Open Networking Consortium

Open Network Systems Layer 1 Interoperability Test Plan [DRAFT]

Rev. 37

University of New Hampshire
InterOperability Laboratory

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Open Networking Consortium
UNH InterOperability Laboratory

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Contents

Modification Record

Revision	Date	Editor(s)	Comments
13	8/6/15	Collin Crowell Daniel Gray David Woolf Greg Roney	
14	8/18/15	David Woolf	Added Test 2.3
15	8/24/15	David Woolf	Added Debug Information Appendix
16	8/31/15	David Woolf	• Corrected Information in Appendix F. • Added Appendix H to describe how many modules or cable assemblies are necessary to complete the testing.
17	9/1/15	David Woolf	• Clarified that MUT/CUT is not required to support DMI (diagnostics) in Test 2.3. • Correction to references in Appendix A • Addition to Appendix H for QSFP+ modules and SFP+/QSFP+ DACs. • Expanded 'Acknowledgements' section
18	9/8/15	David Woolf	•
19	9/15/15	David Woolf	• Fixed typos in Test 2.3
20	9/15/15	David Woolf	• Edited language in Appendix A regarding statements needed from vendors. Edited Appendix B to clarify that all ports of a chassis should be filled, even if there are different port types.
22	11/15/15	Daniel Gray	• Added Test 3.1.3: Insertion Loss for 10G Passive Cables
23	11/17/15	David Woolf	• Removed test 3.1.2 WDP, and renumbered test 3.1.3 to be 3.1.2.
24	1/5/16	David Woolf	• Added new UNH-IOL Address. • Modified Appendix H for proper equipment requirements per expected port counts on current ToR and Spine OCP switches. • Added Appendix I to define test optimization rules. • Added comments to 'Possible

			Problems' section of test 6.4 to allow 'warm up traffic' prior to starting the test. • Added to 'Possible Problems' section of test 6.4 to allow use of a golden module. • Added to 'Possible Problems' section of test 6.1, 6.2, 6.3 to disallow use of a golden module. • Added to 'Possible Problems' section of test 6.4 that although a BER may be determined from test results, only a Pass/Fail indication will be provided in the test results.
25	1/12/16	David Woolf	• Edits to Appendix H to account for 25G DACs and Modules. Improved readability of list, and added length requirements for DACs.
26	1/21/16	Dan Gray	• Additions to Group 4 for LR test cases. Edits to previous titles to define SR test cases. • Additions to Group 3 for future 25G Passive Cable measurements.
27	2/16/16	David Woolf	• Added placeholders for 100G tests in Sections 4.5, 4.6, 5.3. • Renamed document to indicate 'Layer 1' Interoperability, as other work is progressing on proving Layer 2 Interoperability for Open Network Systems. • Add reference to IEEE 802.3bm – 2015
28	4/5/16	David Woolf	• Added info to Appendix B on test setups. Added info to test 6.3 on special handling of LR4 and LR4 Lite trancievers. • Added info to Appendix H on expectations for passive cables. • Added list of interfaces to Abbreviations and Acroynyms page. • Added QSFP28, LR, and 100G products to the requirements page. • Added note at beginning of Group 6 about potential product types for

			testing.
29	4/14/16	Dan Gray	• Sections 4.5, 4.6, 5.3 completed. • Minor edits (typographical, formatting) made throughout Group 4, Group 5.
30	4/29/16	Dan Gray	• Section 3.4 Added. Concens 100GBASE-CR4 return loss and insertion loss testing.
31	6/6/16	David Woolf	• Added 100G AOC quantities to Appendix H. • Added Breakout Cable configurations to Appendix B
32	7/7/16	David Woolf	• Added notes to tests 4.6.3 and 5.3.2 about CTLE support.
33	7/7/16	David Woolf	• Added notes about FEC enablement in the interop tests from Group 6. Added notes in Group 3 about test requirements for x4 breakout cables.
34	7/13/16	David Woolf	• Added notes in Appendix B about special configurations that may be necessary to test with breakout cables. • Added desired quantities of samples for breakout cables in Appendix H.
35	7/25/16	David Woolf	• Added clarification in Possible Problems section of test 6.4 that subtest C is not applicable when using a 1x4 breakout cable, and that in subtest D it may not be possible to fill every port.
36	9/27/16	David Woolf	• Added description to Possible Problems section of test 6.1 of how not all EEPROM values are supported by all NOS. • Added note to Observable Results of test 2.2 for testing QSFP28 modules and reading all 640 bytes of EEPROM. • Added note to Test Optimization rules about not testing at 100% line rate. • Modifed Sections 4.5, 4.6 and 5.3 to show that these measurements should be performed for 25G products as well.

37	2/7/17	David Woolf	• Added description to Possible Problems section of Group 5 allowing alternate test modes to be used if the preferred test mode in not available.

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Introduction

The University of New Hampshire's InterOperability Laboratory (IOL) is an institution designed to improve the interoperability of standards based products by providing an environment where a product can be tested against other implementations of a standard.

This test plan was designed to validate the multi-vendor compatibility of optical transceivers and cables with bare-metal open switches running Networking Operating Systems (NOS) software. The aim is to validate the operation of open network systems, giving end users confidence that the individual components can be combined to create strong alternatives to traditional closed solutions.

The tests do not determine if a product conforms to standards, nor are they purely interoperability tests. Rather, they provide one method to isolate problems within Open Network Systems. Successful completion of all tests contained in this suite does not guarantee that the tested Open Network Module will operate with other Open Network Modules. However, combined with satisfactory operation in the IOL's semi-production environment, these tests provide a reasonable level of confidence that the Device Under Test (DUT) will function well with other Open Network Modules that have been subjected to similar tests.

References

The following documents were referenced in this text:

- IEEE 802.3 - 2012
- IEEE 802.1Q - 2011
- IEEE 802.3bm - 2015
- SFF-8431
- SFF-8432
- SFF-8435
- SFF-8436
- SFF-8472
- SFF-8479
- OCP http://www.opencompute.org/wiki/Networking/SpecsAndDesigns
- ONIE https://github.com/opencomputeproject/onie/wiki
- **100G PSM4 MSA Specification**

Abbreviations and Acronyms

CLI	Command Line Interface
CUT	Cable Assembly Under Test
DOM	Digital Optical Monitoring
DSO	Digital Storage Oscilloscope
DUT	Device Under Test
EEPROM	Electrically Erasable Programmable Read-Only Memory
HTTP	HyperText Transfer Protocol
HUT	Host Under Test
HUT.TS	Port on the HUT connected to Test Station (ex. HUT.TS1 refers to the Port on the HUT connected to Test Station 1)
I^2C	Inter-Integrated Circuit
IPG	Inter-Packet Gap
LP	Link Partner
MUT	Module Under Test
MUT/CUT	Module or Cable Assembly Under Test
NOS	Network Operating System
ONIE	Open Network Install Environment
PHY	Abbreviation for Physical Layer
PVID	Port VLAN ID
QSFP+	Quad Small Form-factor Pluggable, SFF-8679
RMS	Root Mean Square
SFP+	Enhanced Small Form-factor Pluggable, SFF-8431
TS	Test Station (ex. TS1 refers to Test Station 1)
VLAN	Virtual Local Area Network
SFP28	SFF-8402
QSFP28	SFF-8665
LR4	IEEE 802.3ba up to 10 km
SR4	IEEE 802.3ba
LR4 Lite	IEEE 802.3 ba up to 2km
CR4	IEEE 80.2bj

Definition of Terms

Frame:	A unit of data transmission on an IEEE 802 LAN MAC that conveys a PDU between MAC Service users. There are three types of frame; untagged, VLAN-tagged, and priority-tagged.
Host Under Test:	The switch and network operation system subject to the test plan.
Link Partner:	A switch used to connect to the Host Under Test.
Module or Cable Assembly Under Test:	The module or cable assembly subject to the Test Plan. This includes transceivers, passive cables, and active optical cables. This term covers all modules or cable assemblies of the same model that are used in this test plan.
Test Station	A tool that supports the analysis and generation of test traffic, i.e. MAC frames.
Virtual Local Area Network (VLAN):	A subset of the active topology of a Bridged Local Area Network. Associated with each VLAN is a VLAN Identifier (VID).

Test Organization

This document organizes tests by group based on related test methodology or goals. Each group begins with a brief set of comments pertaining to all tests within group. This is followed by a series of description blocks; each block describes a single test. The format of the description block is as follows:

Test Label: The Test Label and title comprise the first line of the test block. The Test Label is the concatenation of the group number, section number and the test number within the group or section, separated by periods.

Purpose: The Purpose is a short statement describing what the test attempts to achieve. It is usually phrased as a simple assertion of the feature or capability to be tested.

Resource Requirements: The Resource Requirements section specifies the software, hardware, and test equipment that will be needed to perform the test.

Discussion: The Discussion is a general discussion of the test and relevant sections of the specification, including any assumptions made in the design or implementation of the test as well as known limitations.

Test Setup: The Test Setup section describes the configuration of the DUT prior to the start of the test. The procedure may involve configuration steps that deviate from what is given in the test setup. If a value is not provided for a protocol parameter, then the protocol's default is used for that parameter.

Test Procedure: This section of the test description contains the step-by-step instructions for carrying out the test. These steps include such things as enabling interfaces, disconnecting links between devices, and sending MAC frames from a Test Station. The test procedure may also instruct the test to make observations, which are interpreted in accordance with the observable results given for that test part.

Observable Results: This section lists observable results that can be examined by the tester to verify that the DUT is operating properly. When multiple observable results are possible, this section provides a short discussion on how to interpret them. The determination of a pass or fail for each test is usually based on how the behavior of the DUT compares to the results described in this section.

Possible Problems: This section contains a description of known issues with the test procedure, which may affect test results in certain situations.

Requirements

Devices covered by this test plan

Pluggable Form Factors
- SFP+ (10G)
- QSFP+ (10G per lane)
- QSFP28 (25G per lane)

Link Technologies (Transceivers and Active Optical Cable assemblies)
- Short Reach (SR) Optics (Multi-mode fiber using 850 nm light)
- Long Reach (LR) Optics (Single-mode fiber using 1310 nm light)

Copper Cables (passive and active)

Host Module Complex
- 10G
- 40G
- 100G

Group 1: Management of NOS through ONIE

Overview: The tests defined in this section verify that the NOS can be uninstalled and reinstalled through ONIE.

Test 1.1 - ONIE Compliance Environment

Purpose: To verify that a host can pass a random sampling of ONIE Compliance Environment tests.

Resource Requirements:

- An HTTP server running on port 80 and hosting the NOS image
- A Linux server with ISC DHCP, tftpd-hpa, nginx, python-pip and python-virtualenv installed
- OCE test script (test-onie.py)
- A hub or switch

Discussion: These tests may be omitted if all of the following apply:

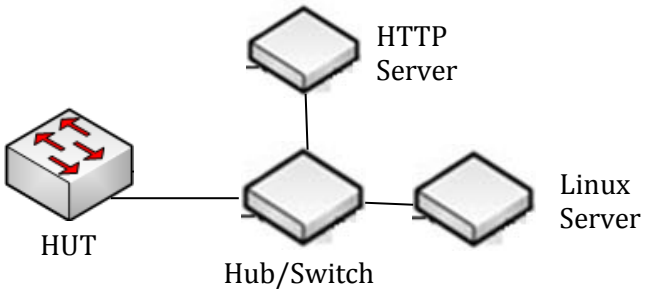
1) The switch has been ONIE HW Certified
2) The NOS has been certified through ONIE NOS Validation with the switch

In the event that the switch has not been through ONIE HW Certification, a random sampling of tests from ONIE Compliance Environment (OCE) will be used. The exact tests will be chosen from one of the following (https://github.com/opencomputeproject/onie/wiki/Testing-OCE):

* Installation: Tests 2 - 37
* Uninstallation: Tests 74 – 76

This test is only applicable if HUT has ONIE pre-installed

Test Setup: The following diagram describes the test layout. The HUT is connected through its Management port. The Linux server is properly configured and the software for OCE testing is installed. ISC DHCP, tftpd-hpa, and nginx are stopped and disabled.



Test Procedure:

Part A: Installation Tests

1. Ensure that the Test Setup is configured.
2. Create a virtual environment on the Linux Server using virtualenv
3. Enter the virtual environment and install the dependencies
4. Power on the HUT and ensure that it boots into ONIE.
5. From the Linux Server, run test-onie.py

Part B: Uninstallation Tests

1. Ensure that the Test Setup is configured and test-onie.py is ready to run
2. From the Linux Server, run test-onie.py

Observable results:

Part A:

- The HUT should pass the random sampling of installation tests.

Part B:

- The HUT should pass the random sampling of uninstallation tests

Possible Problem: None

Test 1.2 - Installing and Uninstalling a NOS through ONIE via HTTP Server

Purpose: To verify that a NOS can be successfully installed through ONIE**.**

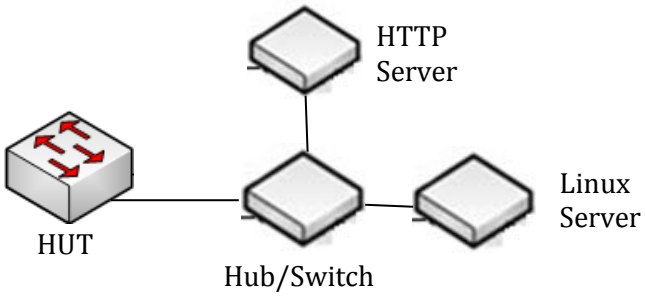
Resource Requirements:

- An HTTP server running on port 80 and hosting the NOS image
- A Linux server running ISC DHCP
- A hub or switch

Discussion: The Open Network Install Environment (ONIE) is a Linux based OS and boot loader which runs on Bare Metal Switches and designed to discover Network Operating Systems (NOS) on a network, transfer the NOS to the switch, then install it. ONIE also provides the means to uninstall the NOS. Once ONIE has installed a NOS, the switch will boot directly into the NOS and not ONIE, but ONIE is still able to be called upon to uninstall or reinstall a NOS.

This test is only applicable if HUT has ONIE pre-installed

Test Setup: The following diagram describes the test layout. The HUT is connected through its Management port.



Test Procedure:

Part A: Installing a NOS

1. Power on the HUT and ensure that it boots into ONIE.
2. Ensure that ONIE has established an IP address from the DHCP server.
3. From ONIE, issue the command " install_url http://<ipAddress>/<fileName>".
4. Wait for ONIE to finish installing the NOS.
5. Reboot the HUT.

Part B: Uninstalling a NOS

1. Power on the HUT and ensure that it boots into the NOS.
2. Reboot the HUT and interrupt the boot process.
3. If the HUT uses the GRUB boot loader, select ONIE from GRUB.
4. From the ONIE list in GRUB, select "uninstall"
5. If the HUT uses the U-Boot boot loader, issue the command “run onie_uninstall”
6. Wait for ONIE to finish uninstalling the NOS.
7. Reboot the HUT

Observable results:

Part A:

- In step 5, the HUT should boot directly into the NOS that was just installed.

Part B:

- In step 7, the Host Under Test should boot directly into ONIE. No NOS should be installed on the Host Under Test.

Possible Problem: None

Group 2: Management of Optical Module

Overview: The tests defined in this section verify that the Modules/Cable Assemblies Under Test are physically compatible with the host under test and that the Module's and Cable Assembly's read-only data is accessible.

Test 2.1 - Physical Compatibility with Supporting Devices

Purpose: To verify that the mechanical form factor is compatible with devices for interoperability purposes

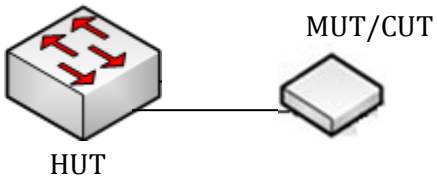
Resource Requirements:

- Known good optical fiber cable with appropriate connector assembly

Discussion: The physical ports on a host must be compatible with Modules or Cable Assemblies of the same form factor. Modules must properly attach to known good optical fiber cable with appropriate connector assembly.

Part B of this test is only applicable to Modules.

Test Setup: The following diagram describes the test layout.



Test Procedure:

Part A: MUT/CUT Insertion

1. Record MUT/CUT part number and serial number.
2. Insert MUT/CUT into port of HUT

Part B: Attaching Fiber

1. Ensure the MUT is inserted in the HUT
2. Attach the known good optical fiber cable with appropriate connectors to the MUT.

Part C: MUT/CUT Removal

1. Remove MUT/CUT from port of HUT

Observable results:

Part A:

- In step 2, the MUT/CUT should insert and mechanically connect to the HUT.

Part B:

- In step 2, the known good optical fiber cable should attach to MUT.

Part C:

- In step 1, the MUT/CUT should remove from the HUT.

Possible Problems: None

Test 2.2 - Host Management of Module or Cable Assembly

Purpose: To verify that the MUT/CUT is manageable via the Host complex.

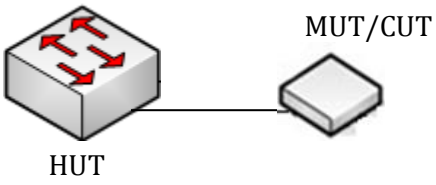
Resource Requirements:

- EEPROM Reader (USB-to-I2C Elite)
- QSFP+ or SFP+ Evaluation board

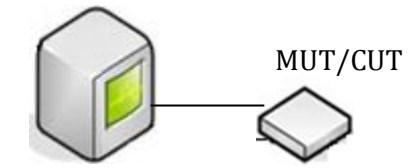
Discussion: Modules and Cable Assemblies alike must present EEPROM data that correctly reflects the information about the device. This information can be extracted though the use of an EEPROM Reader or a host. The Host must be able to recognize the Module or Cable Assembly and display the EEPROM data through the CLI.

Test Setup: The following diagram describes the test layout.

Part A: The MUT/CUT is connected to the HUT.



Part B: The MUT/CUT is inserted into an evaluation board and EEPROM reader.



Test Procedure:

Part A: NOS recognizes MUT/CUT and EEPROM is accessible

1. Record MUT/CUT part number and serial number
2. Insert MUT/CUT into HUT
3. Verify HUT recognizes MUT/CUT type and manufacturer via CLI interface
4. Via CLI interface extract and save EEPROM data (.hex, .txt are acceptable).

Part B: EEPROM is accessible via EEPROM Reader

1. Record MUT/CUT part number and serial number
2. Insert MUT/CUT into evaluation board
3. Connect EEPROM reader to EEPROM via I^2C interface
4. Record *Serial ID* info
    a. For SFP+: Serial ID: A0h – Byte 0-95
    b. For QSFP+: Serial ID: A0h: Page 0 Byte 128-223
5. Record Vendor specific information

   a. For SFP+: Serial ID: A0h – Byte 96-127
   b. For QSFP+: Serial ID: A0h: Page 0 Byte 224-255
6. Extract and save EEPROM data (.hex, .txt are acceptable).

Part C: Compare Results

1. Compare the results obtained in Part A and Part B.

Observable results:

Part A:

- In step 3 and 4, the HUT CLI should recognize the MUT/CUT and accurately reflect the vendor information.
- Ensure that if a QSFP28 module is being tested, that the NOS extracts all 640 bytes of the QSFP28 EEPROM.

Part B:

- In step 6, EEPROM Read Only data shall accurately reflect MUT/CUT information and coincide with CLI.

Part C:

- Ensure that the values obtained in Part A and Part B match, except for the following bytes which are dependent on current status:
  - *TBD*

Possible Problems: Test technician needs to ensure that the correct page of EEPROM data is extracted and observed. This is especially true for QSFP+ Modules and Cable Assemblies.

Test 2.3- Diagnostic Optical Monitor Support

Purpose: To verify that the MUT/CUT (active optical cable only) supports diagnostic functions via the Host complex.

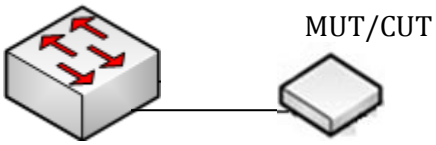
Resource Requirements:

- EEPROM Reader (USB-to-I2C Elite)
- QSFP+ or SFP+ Evaluation board, while for QSFP+ the Pins LPMode and ModSelL need to be in the low state (GND)
- MUT SFP+: OM3 LC simplex patch cord
- MUT QSFP+ SR4: OM3 MPO – 4 x LC-Duplex fanout/breakout cable and 4 x
- LC-Duplex couplers. Alternatively a MPO loop plug (if available)

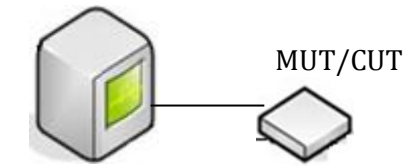
Discussion: Modules and Cable Assemblies alike may support diagnostic functions via the Host complex. Generally these tests can be performed using a Host Complex.

Test Setup: The following diagram describes the test layout.

Part A: The MUT/CUT is connected to the HUT.



Part B: The MUT/CUT is inserted into an evaluation board and EEPROM reader.



Test Procedure:

Part A: NOS recognizes MUT/CUT and EEPROM is accessible

1. Determine if MUT/CUT supports diagnostic capability by probing
    a. For SFP+: I2C Address A0h Byte 92 Bit 6
        i. 0x0 = diagnostic is not implemented
        ii. 0x1 = diagnostic is implemented
    b. For QSFP+: I2C address A0h: Page 0, Byte 220 Bit 3
        i. 0x0 = diagnostic is implemented (received power measurement type OMA)
        ii. 0x1 = diagnostic is implemented (received power measurement type Average Power)
2. Record MUT/CUT part number and serial number

3. Insert MUT/CUT into HUT
4. Verify the following:
    a. SFP+: verify HUT reports Temperature, Supply Voltage (Vcc), RX power, TX bias current, TX power (need to clarify if host OS supports the diagnostic optical monitor reporting)
    b. QSFP+ : verify HUT reports Temperature, Supply Voltage (Vcc), RX power channel 1-4, TX bias current channel 1-4, TX power channel 1 – 4. (need to clarify if host OS supports the diagnostic optical monitor reporting)
5. Via CLI interface extract and save EEPROM data (.hex, .txt are acceptable).

Part B: EEPROM is accessible via EEPROM Reader

1. Record MUT/CUT part number and serial number
2. Insert MUT/CUT into evaluation board
3 MUT/CUT loop
    3.1 SFP+: Loop TX and RX with LC patch cord
    3.2 QSFP+: Loop TX1 with RX1, TX2 with RX2, TX3 with RX3, TX4 with RX4 with fanout/breakout patch cord
    3.3 CUT: loop counterpart transceiver with 2nd eval board with looped high speed lanes

4. Connect EEPROM reader to EEPROM via I2C interface
5. Enable Laser(s). If laser is enabled by default it will be necessary to disable the laser first.
    5.1 SFP+: set Pin TX_Disable to low power state (GND)
    5.2 QSFP+: write at I2C address A0h, Page 0, Byte 86 the value 0x00 to enable all four transmitters/channels

6. Record Alarm and Warning Threshold
6.1 SFP+ (I2C address A2h, Byte 0 - 55)
6.2 QSFP+ (I2C address A0h, Page 3 Byte 128 – 223)

7. Record monitoring values (A/D) information
7.1 SFP+ (I2C address A2h, Byte 96 - 109)
7.2 QSFP+ (I2C address A0h, Page 0 Byte 22 – 81)

2. Extract and save EEPROM data (.hex, .txt are acceptable).

Observable results:

Part A:

- In step 3 and 4, the HUT CLI should recognize the MUT/CUT and accurately reflect the vendor information.
- For SFP+ devices, record if the MUT/CUT supports diagnostic capabilities.
- For QSFP+ devices, record if the MUT/CUT supports diagnostic functions for
    - Received power
    - Bias current
    - Supply voltage
    - Temperature
- If the MUT/CUT supports diagnostic monitoring, record whether the NOS properly reads this diagnostic information. The NOS may or may not support decoding the diagnostic information.

Part B:

- In step 6, EEPROM Read Only data shall accurately reflect MUT/CUT information and coincide with CLI.

Possible Problems: Test technician needs to ensure that the correct page of EEPROM data is extracted and observed. This is especially true for QSFP+ Modules and Cable Assemblies.

Group 3: Passive Cable Testing

Overview: These tests are performed to verify that the return loss characteristics of passive cables are compliant to the appropriate standard, where SFP+ Passive Cables are governed by SFF-8431 and QSFP+ Passive Cables are governed by IEEE Std. 802.3-2012.

A common use case of passive cables in datacenters is 1x4 breakouts. These can be 4x 10G SFP to 1x 40G QSFP cables, or 4x 25G SFP28 to 1x 100G QSFP28 cables. For such breakout cables, its acceptable to perform the testing defined in Group 3 on a single lane of the 10G or 25G breakout.

Section 3.1: 10G Passive Cable Measurements

Test 3.1.1 - Return loss for 10G Passive Cable

Purpose: To verify that the return loss of the Cable under test is within the conformance limits provided by SFF-8431 Appendix E, Table 37.

Resource Requirements:

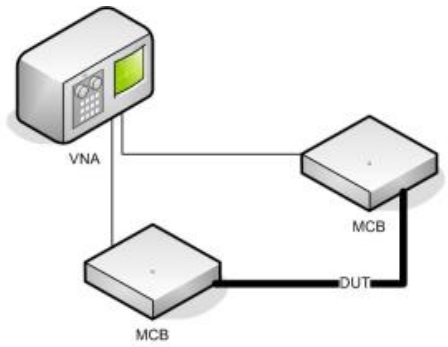
- Network Analyzer
- Module Compliance Boards (2)

Discussion: SFF-8431 Appendix E, Table 37, defines the differential return loss limits for cable assemblies by the following equation:

$$\begin{Bmatrix} -12 + 2\sqrt{f} & 0.01 \le f < 4.1GHz \\ -6.3 + 13log_{10}\left(\frac{f}{5.5}\right) & 4.1GHz < f \le 11.1GHz \end{Bmatrix} (dB)$$

Where *f* is frequency in GHz

Test Setup: The following diagram describes the test layout.



Test Procedure:

Part A: 10G Passive Cable Return Loss

1. Record Cable Assembly part number and serial number
2. Insert the cable under test into the test setup.
3. Measure the return loss of the DUT.

Observable results:

Part A:

- The return loss of the cable under test shall not exceed the values as stated and defined in the equations stated in the discussion for passive cable assemblies.

Possible Results: None.

Test 3.1.2 - Insertion loss for 10G Passive Cable

Purpose: To verify that the insertion loss of the Cable under test is within the conformance limits provided by IEEE Std. 802.3-2012 Annex , Table 37.

Resource Requirements:

- Network Analyzer
- Module Compliance Boards

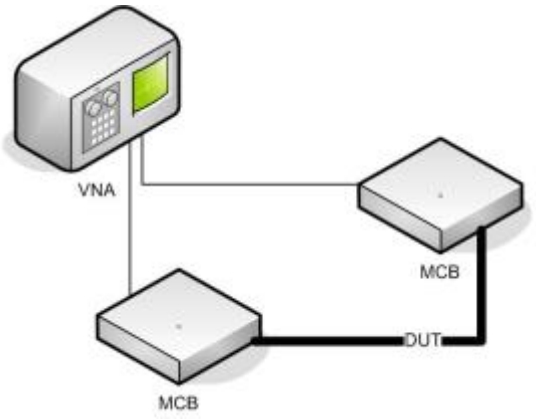
Discussion: The insertion loss characteristics of a passive cable can help to diagnose issues in data transmission. For 10GbE, SFP+ Direct Attach Cables, there is no value for insertion loss limits included in the governing document SFF-8431, Appendix E. Due to the similarities between SFP+ Direct Attach Cables and QSFP+ Direct Attach Cables (40GBASE-CR4), those limits will be used. A certain amount of insertion loss in 40GBASE-CR4 cabling is allowed by IEEE Std. 802.3-2012 Clause 85.10 for compliance.

Insertion loss is to be measured at Nyquist rate. For 40GBASE-CR4 cables, a maximum insertion loss of 17.04 dB can be allowed at 5.15625 GHz. This is provided by IEEE Std. 802.3-2012 Clause 85, Table 85-9. Furthermore, this table provides a value of 3 dB loss as the minimum insertion loss at 5.15625GHz.

Therefore, the insertion loss at 5.15625 GHz must satisfy the following equation.

$$\mathbf{3}\boldsymbol{dB} \leq \boldsymbol{SDD}\mathbf{21}, \boldsymbol{SDD}\mathbf{12} \leq \mathbf{17.04}\boldsymbol{dB}, \qquad \boldsymbol{at}\ \mathbf{5.15625}\ \boldsymbol{GHz}$$

Test Setup: The following diagram describes the test layout.



Test Procedure:

Part A: 10G Passive Cable Insertion Loss

1. Record Cable Assembly part number and serial number
2. Insert the cable under test into the test setup.
3. Measure the insertion loss of the DUT.

Observable results:

Part A:

- The insertion loss of the cable under test shall not violate the values as stated in defined in the equations stated in the discussion for passive cable assemblies.

Possible Problems: None

Section 3.2: 40G Passive Cable Measurements

Test 3.2.1 - Return loss for 40G Passive Cable

Purpose: To verify that the return loss of the cable under test is within the conformance limits provided by IEEE Std. 802.3-2012, subclause 85.10.4

Resource Requirements:

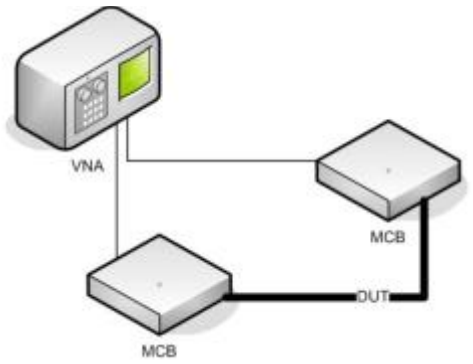
- Network Analyzer
- Module Compliance Boards (2)

Discussion: IEEE Std. 802.3-2012, 85.10.4 states that return loss limits for 40GBASE-CR4 cable assemblies are defined by the following equation:

$$\begin{Bmatrix} -12 + 2\sqrt{f} & 0.01 \le f < 4.1GHz \\ -6.3 + 13log_{10}\left(\frac{f}{5.5}\right) & 4.1GHz < f \le 11.1GHz \end{Bmatrix} (dB)$$

Where f is frequency in GHz.

Test Setup: The following diagram describes the test layout.



Test Procedure:

Part A: 40G Passive Cable Return Loss

1. Record Cable Assembly part number and serial number
2. Insert the cable under test into the Test Setup.
3. Measure the return loss of the cable under test.

Observable results:

Part A:

- The return loss of the cable under test shall not exceed the values as stated in IEEE Std. 802.3-2012, subclause 85.10.4.

Possible Problem: None

Test 3.2.2 - Insertion loss for 40G Passive Cable

Purpose: To verify that the insertion loss of the Cable under test is within the conformance limits provided by IEEE Std. 802.3-2012 Annex , Table 37.

Resource Requirements:

- Network Analyzer
- Module Compliance Boards

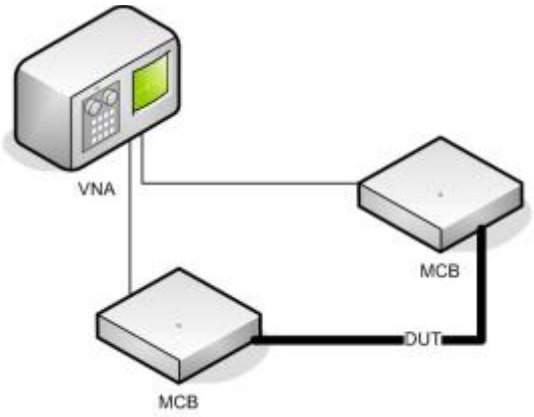
Discussion: The insertion loss characteristics of a passive cable can help to diagnose issues in data transmission. For 40GbE QSFP+ Direct Attach Cables (40GBASE-CR4), a certain amount of insertion loss is allowed by IEEE Std. 802.3-2012 Clause 85.10 for compliance.

Insertion loss is to be measured at Nyquist rate. For 40GBASE-CR4 cables, a maximum insertion loss of 17.04 dB can be allowed at 5.15625 GHz. This is provided by IEEE Std. 802.3-2012 Clause 85, Table 85-9. Furthermore, this table provides a value of 3 dB loss as the minimum insertion loss at 5.15625GHz.

Therefore, the insertion loss at 5.15625 GHz must satisfy the following equation.

$$\boldsymbol{3dB \leq SDD21, SDD12 \leq 17.04dB, \quad at\ 5.15625\ GHz}$$

Test Setup: The following diagram describes the test layout.



Test Procedure:

Part A: 40G Passive Cable Insertion Loss

4. Record Cable Assembly part number and serial number
5. Insert the cable under test into the test setup.
6. Measure the insertion loss of the DUT.

Observable results:

Part A:

- The insertion loss of the cable under test shall not violate the values as stated in defined in the equations stated in the discussion for passive cable assemblies.

Possible Problem: None

Section 3.3: 25G Passive Cable Measurements

Test 3.3.1 - Return loss for 25G Passive Cable

Purpose: To verify that the insertion loss of the Cable under test is within the conformance limits provided by IEEE Std. 802.3by (DRAFT)

Resource Requirements:

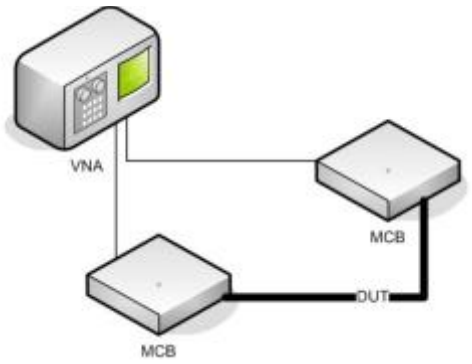
- Network Analyzer
- Module Compliance Boards

Discussion: The return loss characteristics of a passive cable can help to diagnose issues in data transmission. For 25GbE SFP28 Direct Attach Cables, a certain amount of return loss is allowed by IEEE Std. 802.3by Clause 110.10 for compliance. Std. 802.3by refers to Std. 802.3 Clause 92 for return loss characteristics, which are seen below. In addition to this, the minimum return loss at Nyquist – 12.8906 GHz) is also defined as 6dB.

$$\begin{Bmatrix} -16.5 + 2\sqrt{f} & 0.05 \le f < 4.1GHz \\ -10.66 + 14log_{10}\left(\frac{f}{5.5}\right) & 4.1GHz < f \le 19GHz \end{Bmatrix} (dB)$$

Where f is frequency in GHz.

Test Setup: The following diagram describes the test layout.



Test Procedure:

Part A: 25G Passive Cable Return Loss

1. Record Cable Assembly part number and serial number
2. Insert the cable under test into the Test Setup.
3. Measure the return loss of the cable under test.

Observable results:

Part A:

- The return loss of the cable under test shall not exceed the values as stated in IEEE Std. 802.3by.

Possible Problem: None

Test 3.3.2 - Insertion loss for 25G Passive Cable

Purpose: To verify that the insertion loss of the Cable under test is within the conformance limits provided by IEEE Std. 802.3by (DRAFT)

Resource Requirements:

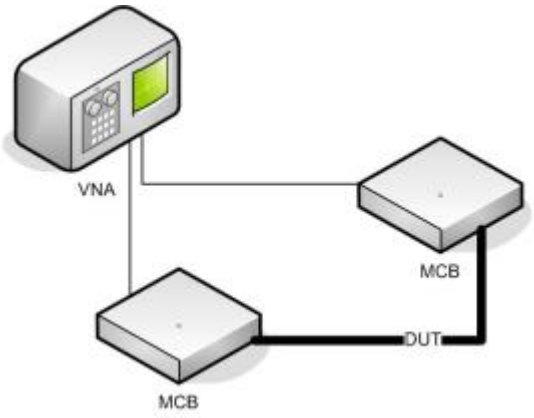
- Network Analyzer
- Module Compliance Boards

Discussion: The insertion loss characteristics of a passive cable can help to diagnose issues in data transmission. For 25GbE SFP28 Direct Attach Cables, a certain amount of insertion loss is allowed by IEEE Std. 802.3by Clause 110.10 for compliance.

Insertion loss is to be measured at Nyquist rate. For 25GbE cables, a minimum insertion loss of 8dB can be allowed at 12.8906 GHz. This is provided by IEEE Std. 802.3by, Table 110-9. Furthermore, this table provides a maximum insertion loss values at 12.8906 GHz for three variants of 25G DACs. These values are as follows:

CA-25G-N	$\boldsymbol{8dB \leq SDD21, SDD12 \leq 15.5dB}$
CA-25G-S	$\boldsymbol{8dB \leq SDD21, SDD12 \leq 16.48\ dB}$
CA-25G-L	$\boldsymbol{8dB \leq SDD21, SDD12 \leq 22.48\ dB}$

Test Setup: The following diagram describes the test layout.



Test Procedure:

Part A: 25G Passive Cable Insertion Loss

1. Record Cable Assembly part number and serial number
2. Insert the cable under test into the test setup.
3. Measure the insertion loss of the DUT.

Observable results:

Part A:

- The insertion loss of the cable under test shall not violate the values as stated in defined in the equations stated in the discussion for passive cable assemblies.

Possible Problem: None

Section 3.4: 100GBASE-CR4 Passive Cable Measurements

Test 3.3.1 - Return loss for 100GBASE-CR4 Passive Cable

Purpose: To verify that the insertion loss of the Cable under test is within the conformance limits provided by IEEE Std. 802.3bj

Resource Requirements:

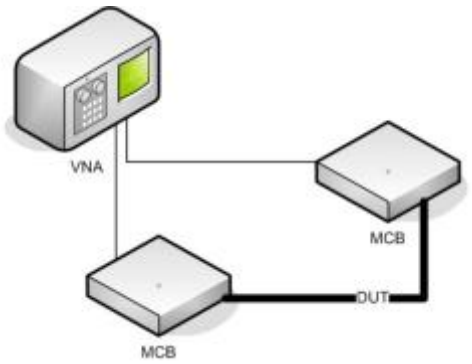
- Network Analyzer
- Module Compliance Boards

Discussion:

IEEE Std. 802.3bj, subclause 92.10.3, define the return loss characteristics for each pair of a 100GBASE-CR4 cable assembly . The return loss characteristics of a passive cable can help to diagnose issues in data transmission. In addition to this, the minimum return loss at Nyquist (12.8906 GHz) is defined at 6dB. The nominal differential reference impedance of the cable assembly is defined as 100Ω.

$$\boldsymbol{SDD11, SDD22} \geq \begin{Bmatrix} \mathbf{16.5 - 2\sqrt{f}} & \mathbf{0.05 \leq f \leq 4.1} \\ \mathbf{10.66 - 14\log_{10}(f/5.5)} & \mathbf{4.1 \leq f \leq 19} \end{Bmatrix} \boldsymbol{(dB)}$$

Test Setup: The following diagram describes the test layout.



Test Procedure:

Part A: 100GBASE-CR4 Passive Cable Return Loss

1. Record Cable Assembly part number and serial number
2. Insert the cable under test into the Test Setup.
3. Measure the return loss of the cable under test.

Observable results:

Part A:

- The return loss of the cable under test shall not violate the governing equation.

Possible Problem: None

Test 3.3.2 - Insertion loss for 100GBASE-CR4 Passive Cable

Purpose: To verify that the insertion loss of the Cable under test is within the conformance limits provided by IEEE Std. 802.3bj

Resource Requirements:

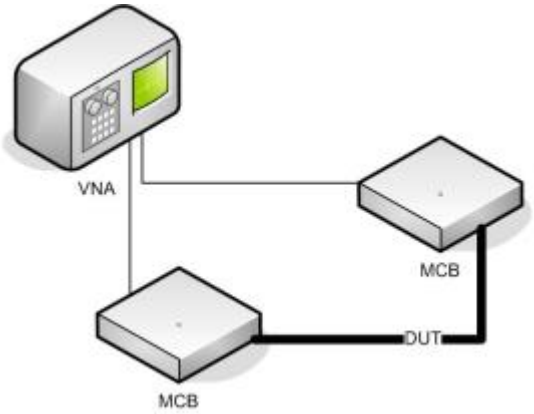
- Network Analyzer
- Module Compliance Boards

Discussion:

The insertion loss characteristics of a passive cable can help to diagnose issues in data transmission. For 100GBASE-CR4 passive cable assemblies, a certain amount of insertion loss is allowed by IEEE Std. 802.3bj, subclause 92.10.2. Insertion loss characteristics of a passive cable can help to diagnose issues in data transmission. In addition to this, the minimum return loss at Nyquist (12.8906 GHz) is defined at 6dB. The nominal differential reference impedance of the cable assembly is defined as 100Ω.

100GBASE-CR4	$8dB \leq SDD21, SDD12 \leq 22.48\ dB$

Test Setup: The following diagram describes the test layout.



Test Procedure:

Part A: 100GBASE-CR4 Passive Cable Insertion Loss

1. Record Cable Assembly part number and serial number
2. Insert the cable under test into the test setup.
3. Measure the insertion loss of the DUT.

Observable results:

Part A:

- The insertion loss of the cable under test shall not violate the values as stated in defined in the equations stated in the discussion for passive cable assemblies.

Possible Problem: None

Group 4: Active Optical Cable and Module Compliance Testing

Overview: These tests verify that Active Optical Cables (AOCs) and Modules are compliant to the standard appropriate for their technologies.

Section 4.1: Test Equipment Calibration for 10GbE SFP+ AOCs and Modules

Test 4.1.1 – Calibration for 10G SFP+ Module and AOC Testing

Purpose: To establish Electrical input baseline of the SFP+ optical modules.

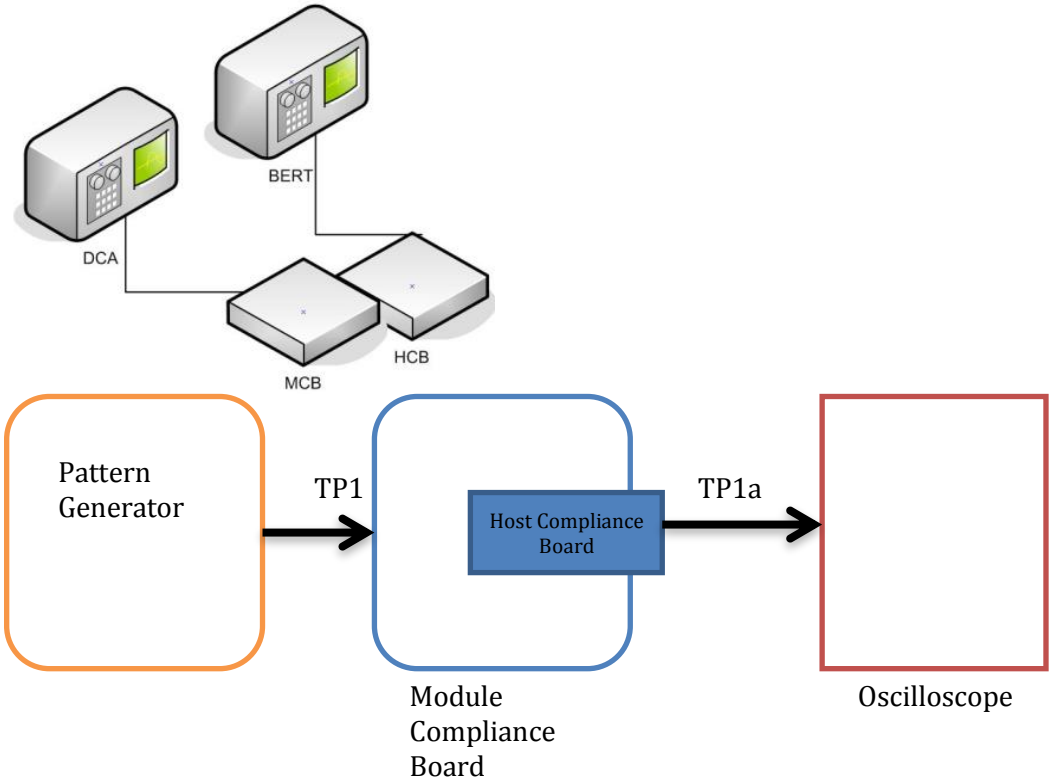
NOTE: This measurement needs to only to be done at the beginning of module testing and not for every DUT.

Resource Requirements:

- Compliance Signal Generator
- Crosstalk Signal Generator
- Module Compliance Boards (2)
- Host Compliance Board
- Digital Storage Oscilloscope

Discussion: Establishing a baseline allows a reference for SFP+ Module measurements.

Test Setup: The first diagram shows the specific setup for the calibration. The second diagram below is derived from IEEE 802.3-2012. The test points provided are as follows: TP1a represents a test point as measured at the output of the Module Compliance Board -> Host Compliance Board combination.



Test Procedure:

Part A: TP1a Calibration of Test Equipment

1. Screen Capture Eye mask
2. Capture 1000 waveforms.
3. Verify Eye Mask Margin. TP1a Electrical Mask specified in SFF-8431 is as follows:

X1, X2, Y1, Y2 = 0.12UI, 0.33UI, 95mV, 350mV
Hit ratio = 5 X 10^{-5}

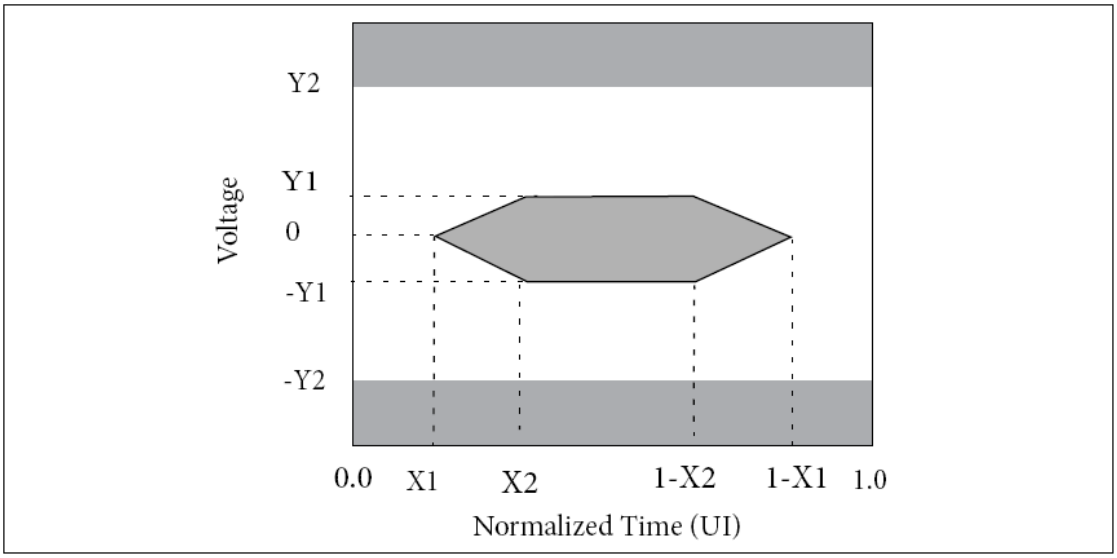


Figure 19 Transmitter Differential Output Compliance Mask at B and B"

Observable Results:

Part A:

- Informational - this is a baseline measurement to reference other SFP+ measurements from. Ensure that the Mask Margin > 0%

Possible Problem: None

Test 4.1.2 - 10G SFP+ Golden Module Verification for SR Variants

Purpose: To record the optical output eye mask margin of the Golden Optical Unit. This unit will be used to test SFP+ Modules at TP4.

NOTE: This measurement needs to only to be done at the beginning of module testing and not for every module under test.

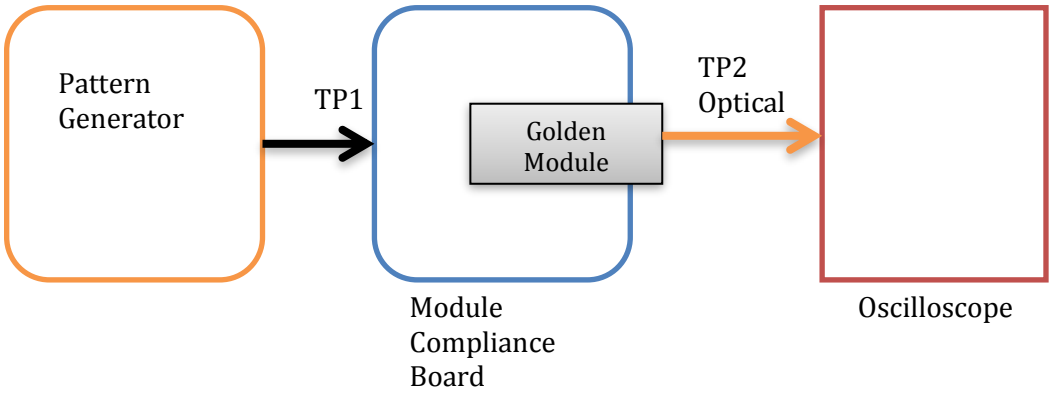
Resource Requirements:

- Compliance Signal Generator
- Crosstalk Signal Generator
- Module Compliance Board
- Digital Storage Oscilloscope capable of Optical Measurements
- 2-5m 50um Optical Patch Cable

Discussion: Establishing a baseline allows a reference for all other optical receiver measurements.

Test Setup: The below block diagram is derived from IEEE 802.3-2012.

The test points provided are as follows.
TP1 represents the electrical input signal to the Golden Module.
TP2 represents the output of this module after a 2m-5m patch cord. It is at this point that the Golden Module is measured.



Test Procedure

Part A: Golden Module Verification

1. Instruct the pattern generator to transmit PRBS31 using settings from 4.1.1.
2. Connect the Golden Module to the scope using the 2m-5m patch cord.
3. Capture 1000 waveforms.

4. Verify that the eye diagram at TP2 is compliant to an eye mask defined by the following points: X1, X2, X3, Y1, Y2, Y3 = 0.235, 0.395, 0.45, 0.235, 0.265, 0.4
    a. Hit ratio = 5 X 10^{-5}

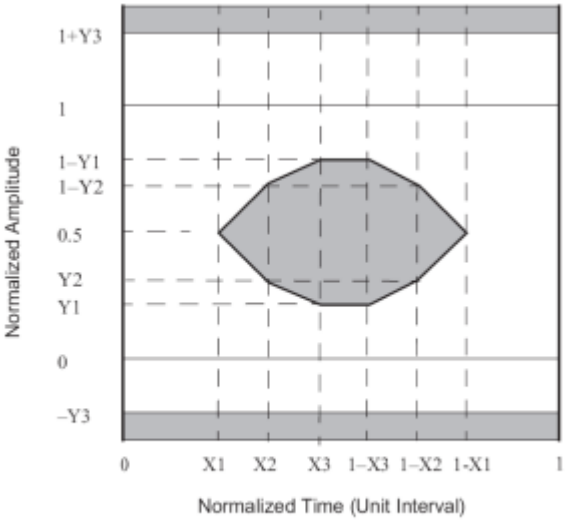


Figure 52–8—Transmitter eye mask definition

Observable results:

Part A:

- Informational - to establish baseline of test equipment as reference for additional tests. Ensure the Mask Margin > 0%

Possible Problem: None

Test 4.1.3 - 10G SFP+ Golden Module Verification for LR Variants

Purpose: To record the optical output eye mask margin of the Golden Optical Unit. This unit will be used to test SFP+ Modules at TP4.

NOTE: This measurement needs to only to be done at the beginning of module testing and not for every module under test.

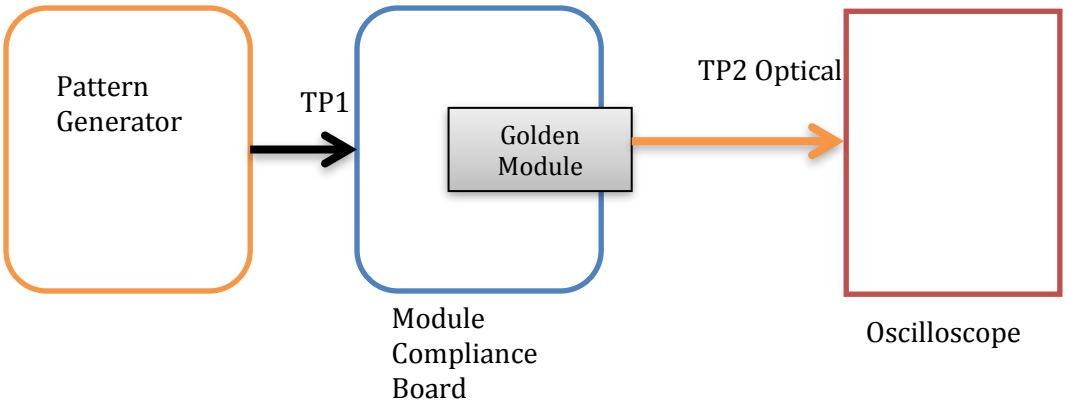
Resource Requirements:

- Compliance Signal Generator
- Crosstalk Signal Generator
- Module Compliance Board
- Digital Storage Oscilloscope capable of Optical Measurements
- 2-5m SMF Optical Patch Cable

Discussion: Establishing a baseline allows a reference for all other optical receiver measurements.

Test Setup: The below block diagram is derived from IEEE 802.3-2012.

The test points provided are as follows.
TP1 represents the electrical input signal to the Golden Module.
TP2 represents the output of this module after a 2m-5m patch cord. It is at this point that the Golden Module is measured.



Test Procedure

Part A: Golden Module Verification

1. Instruct the pattern generator to transmit PRBS31 using settings from 4.1.1.
2. Connect the Golden Module to the scope using the 2m-5m patch cord.
3. Capture 1000 waveforms.

4. Verify that the eye diagram at TP2 is compliant to an eye mask defined by the following points: X1, X2, X3, Y1, Y2, Y3 = 0.235, 0.395, 0.45, 0.235, 0.265, 0.4
    b. Hit ratio = 5 X 10^{-5}

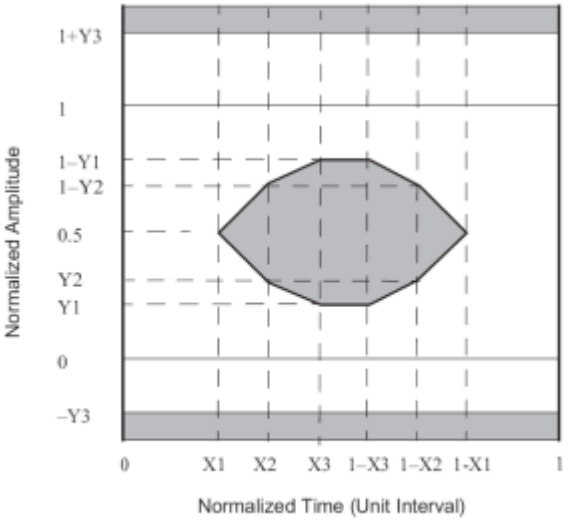


Figure 52–8—Transmitter eye mask definition

Observable results:

Part A:

- Informational - to establish baseline of test equipment as reference for additional tests. Ensure the Mask Margin > 0%

Possible Problem: None

Section 4.2: 10GbE SFP+ Testing for AOCs and Modules

Test 4.2.1 - Transmitter eye mask for 10G SFP+ (Modules Only) (SR Variants)

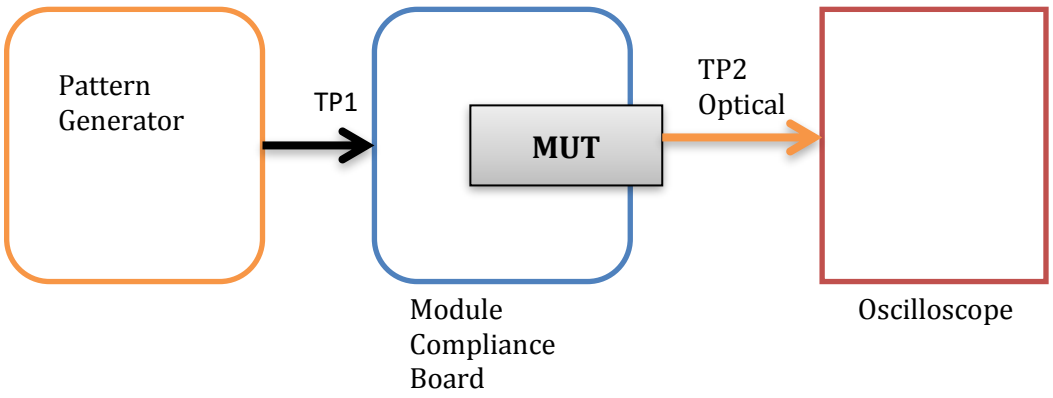
Purpose: To verify that the optical transmitter of the module under test (MUT) meets the specified requirements.

Resource Requirements:

- Compliance Signal Generator
- Crosstalk Signal Generator
- Module Compliance Board
- Digital Storage Oscilloscope capable of Optical Measurements
- 2-5m 50um Optical Patch Cable

Discussion: A transmitter Eye mask can indicate significant information about the health of a transmitter.

Test Setup: TP1 represents the electrical input signal to the module through the MCB. TP2 represents the output of this module after a 2m-5m patch cord.



Test Procedure

Part A: TP2 Module Validation

1. Record Optical Module part number and serial number
2. Use the board setup and input signal measured in section 4.1.1.
3. Configure the scope to capture 1000 waveforms.
4. Insert module under test into the Evaluation Board, connect the optical fiber to the DCA and capture the following information:
   a. Optical Eye (screen capture).
   b. Transmitter Eye Mask definition X1, X2, X3, Y1, Y2, Y3 = 0.235, 0.395, 0.45, 0.235, 0.265, 0.40 10.3125Gbps. IEEE 802.3-2012 Clause 52 compliant

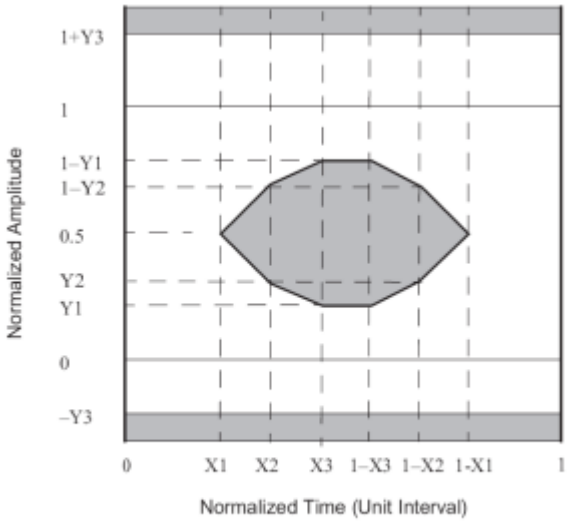


Figure 52–8—Transmitter eye mask definition

Observable results:

Part A:

- Hit ratio shall not exceed 5 x 10^{-5} per sample. Ensure the Mask Margin > 0%

Possible Problems: None

Test 4.2.2 - Transmitter eye mask for 10G SFP+ (Modules Only) (LR Variants)

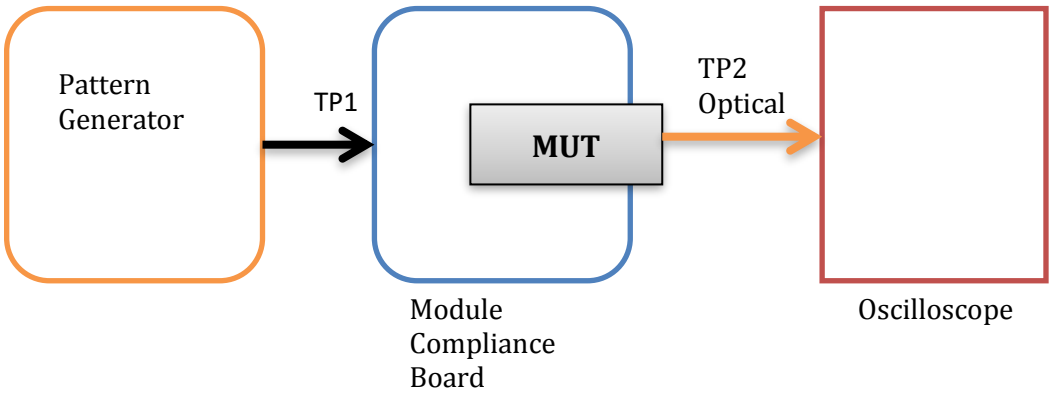
Purpose: To verify that the optical transmitter of the module under test (MUT) meets the specified requirements.

Resource Requirements:

- Compliance Signal Generator
- Crosstalk Signal Generator
- Module Compliance Board
- Digital Storage Oscilloscope capable of Optical Measurements
- 2-5m SMF Optical Patch Cable

Discussion: A transmitter Eye mask can indicate significant information about the health of a transmitter.

Test Setup: TP1 represents the electrical input signal to the module through the MCB. TP2 represents the output of this module after a 2m-5m patch cord.



Test Procedure

Part A: TP2 Module Validation

1. Record Optical Module part number and serial number
2. Use the board setup and input signal measured in section 4.1.1.
3. Configure the scope to capture 1000 waveforms.
4. Insert module under test into the Evaluation Board, connect the optical fiber to the DCA and capture the following information:
   a. Optical Eye (screen capture).
   b. Transmitter Eye Mask definition X1, X2, X3, Y1, Y2, Y3 = 0.235, 0.395, 0.45, 0.235, 0.265, 0.40 10.3125Gbps. IEEE 802.3-2012 Clause 52 compliant

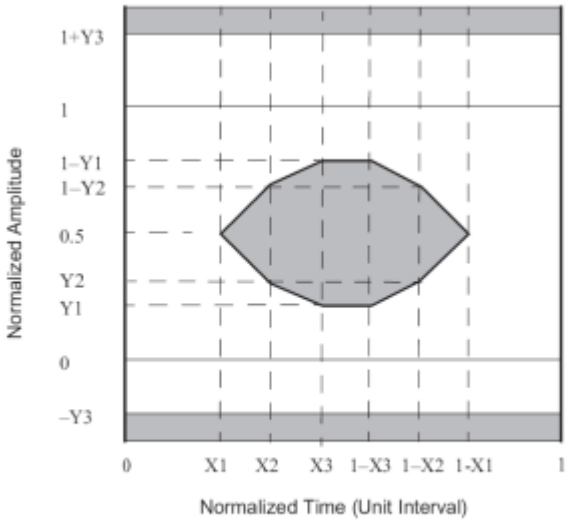


Figure 52–8—Transmitter eye mask definition

Observable results:

Part A:

- Hit ratio shall not exceed 5 x 10^{-5} per sample. Ensure the Mask Margin > 0%

Possible Problems: None

Test 4.2.3 - Output eye mask for 10G SFP+

Purpose: To verify that the device (Module or Cable Assembly) under test (DUT) demonstrates electrical output characteristics that meets the specified requirements.

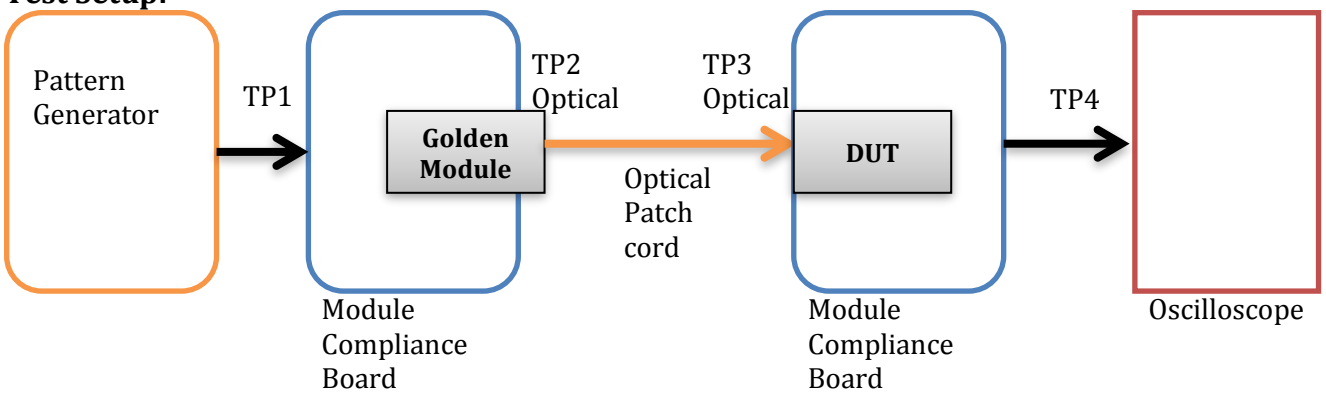
Resource Requirements:

- Compliance Signal Generator
- Crosstalk Signal Generator
- Module Compliance Boards (2)
- Host Compliance Board
- Digital Storage Oscilloscope
- Golden Module verified by test 4.1.2 (Module Testing Only)

Discussion: An eye mask of the electrical output can indicate significant information about the health of a module's receiver.

Part A of this test is only applicable to modules. Part B of this test is only applicable to active optical cables.

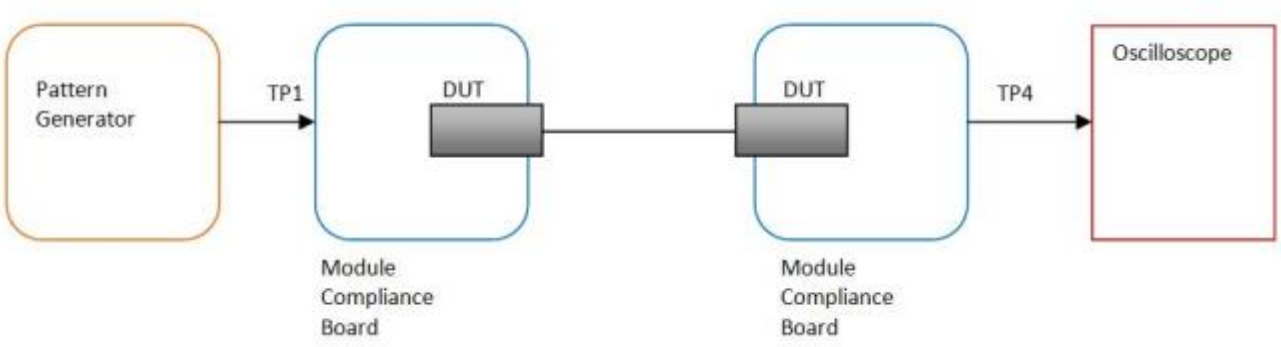
Test Setup:



This test encompasses electrical output eye mask verification for both Modules and AOCs. Because of this, please note the two setups below describing this test for Modules (top) and AOCs (below).

The above setup describes the physical setup and the test points at various locations in the setup for Modules. For this test, the electrical eye mask will be measured at TP4 (TP4 defined in IEEE 802.3-2012). The electrical output of the DUT is measured through an IEEE Std. 802.3-2012 compliant Module Compliance Board.

The setup below describes the physical setup and the test points at various locations in the setup for AOCs. Notice that TP2 and TP3 are hidden when evaluating AOCs. For this test, the electrical eye mask will be measured at TP4 (TP4 defined in IEEE 802.3 – 2012). The electrical output of the Cable under test is measured through a IEEE Std. 802.3 – 2012 compliant Module Compliance Board.



Test Procedure:

Part A: Module TP4 Verification

1. Record Optical Module part number and serial number
2. Use the board setup with the golden optical module results from test 4.1.2 (SR) or 4.1.3 (LR).
3. Insert Module under test into the MCB, and capture the following information using test pattern PRBS31, transmitted using the settings calibrated in test 4.1.1:
    a. Electrical Eye (screen capture).
    b. Capture 1000 waveforms.
    c. Verify that the eye diagram at TP4 is compliant to an eye mask defined by the following points: X1, Y1, Y2 = 0.35UI, 150mV, 425mV (Figure below)
    c. Hit ratio = 5 X 10^{-5}

Part B: Active Optical Cable TP4 Verification

1. Record Optical Module part number and serial number
2. Insert Cable under test into the setup, capture the following information using test pattern PRBS31, transmitted using the settings calibrated in test 4.1.1:
    a. Electrical Eye (screen capture).
    b. Capture 1000 waveforms.
    c. Verify that the eye diagram at TP4 is compliant to an eye mask defined by the following points: X1, Y1, Y2 = 0.35UI, 150mV, 425mV (Figure below)
    d. Hit ratio = 5 X 10^{-5}

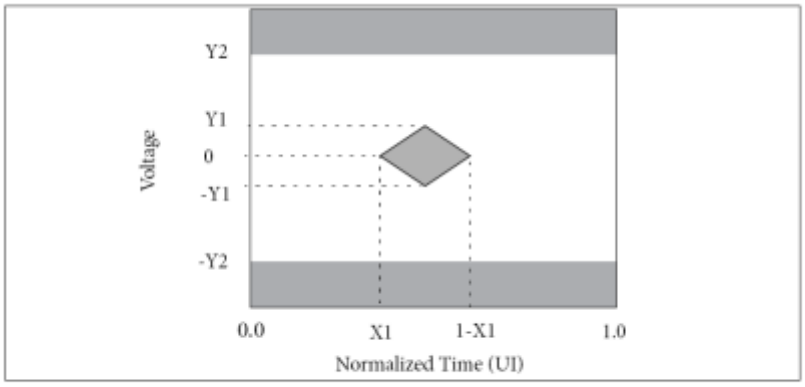


Figure 20 Host Receiver Input Compliance Mask at C" Supporting Limiting Module

Observable results:

Part A:

- Hit ratio shall not exceed 5 x 10^{-5} per sample. Ensure the Mask Margin > 0%.

Part B:

- Hit ratio shall not exceed 5 x 10^{-5} per sample. Ensure the Mask Margin > 0%.

Possible Problems: None

Section 4.3: Test Equipment Calibration for 40GbE QSFP+ AOCs and Modules

Test 4.3.1 – Calibration for 40G QSFP+ Module and AOC Testing

Purpose: To establish Electrical TP1a input baseline to the QSFP+ optical cables, optical modules and copper cables.

NOTE: This measurement needs to only to be done at the beginning of module testing and not for every module or cable under test.

Resource Requirements:

- Compliance Signal Generator
- Crosstalk Signal Generator
- Module Compliance Boards (2)
- Host Compliance Board
- Digital Storage Oscilloscope

Discussion: Establishing a baseline allows a reference for all other optical measurements.

Test Setup: The following diagram is borrowed from IEEE 802.3-2012, and defines test points for QSFP+ testing.

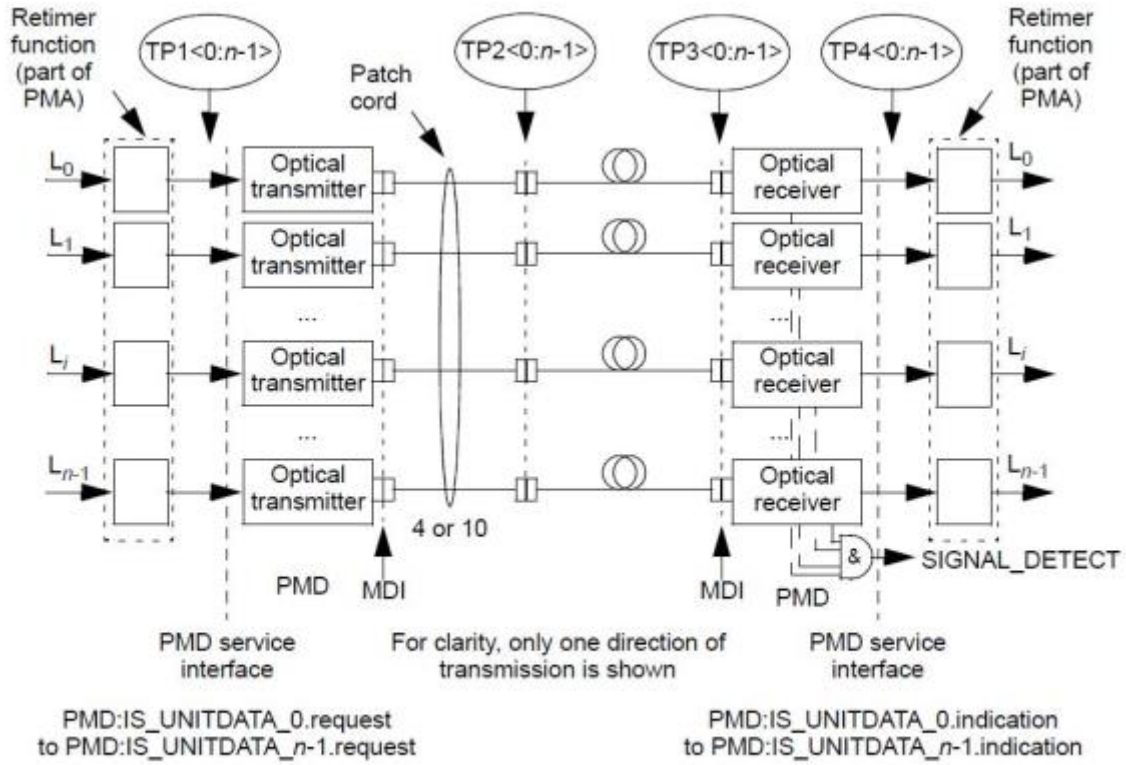
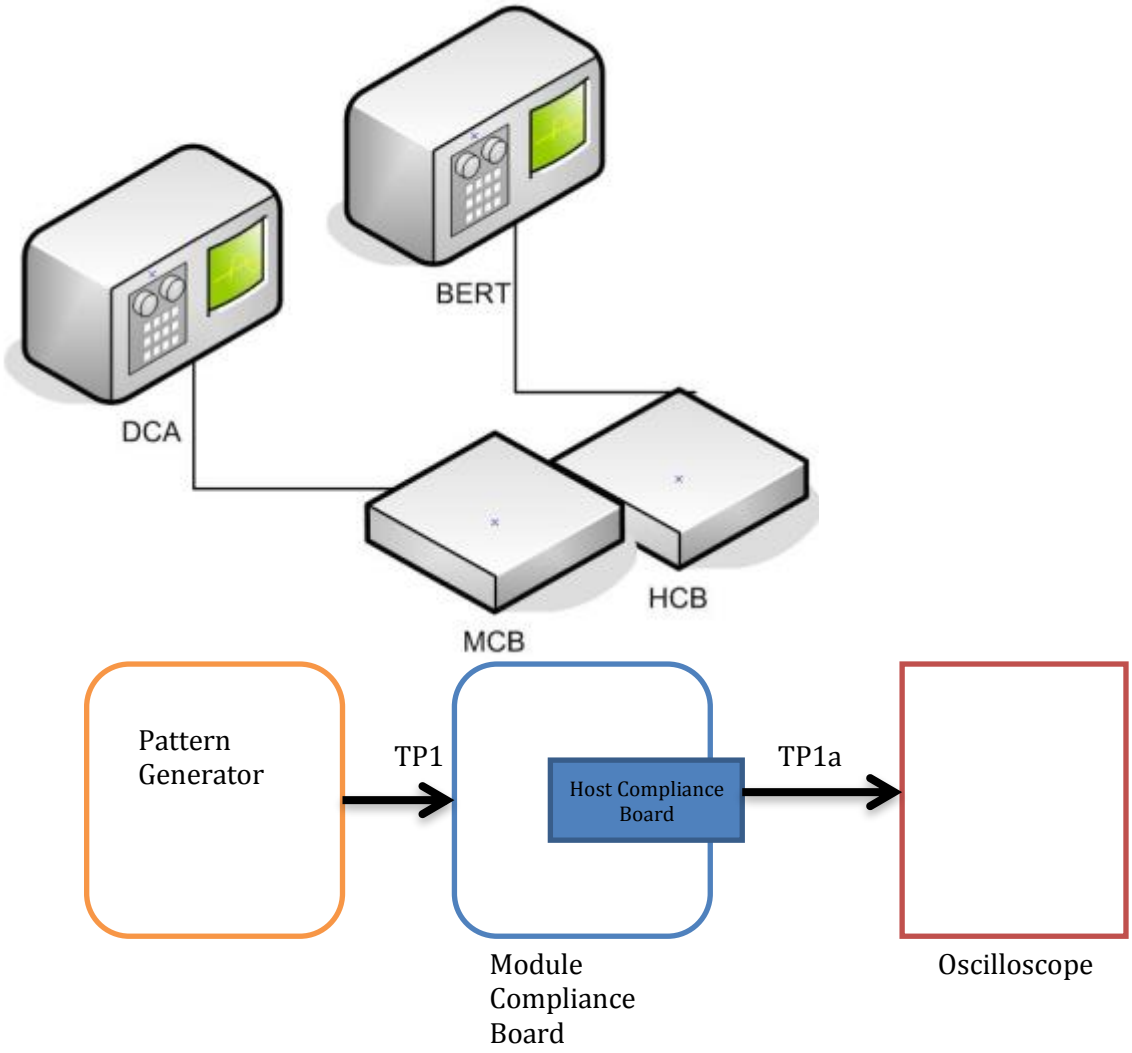


Figure 86–2—Block diagram for 40GBASE–SR4 and 100GBASE–SR10 transmit/receive paths

Throughout the test plan, lane two [of lanes 1, 2, 3, 4] shall be used for evaluation, while other lanes will be active and terminated. Below is a simplified diagram describing calibration points for our test plan.

The below block diagram is derived from IEEE 802.3-2012. The test points provided are as follows: TP1 represents a test point before the electrical input of the MCB. TP1a represents the point of calibration for the pattern generator. This setup is used to calibrate the pattern generator's output in order to ensure that a compliant eye diagram is recovered at TP1a. Note that the lane tested shall be lane two, while all other lanes will be active and terminated.

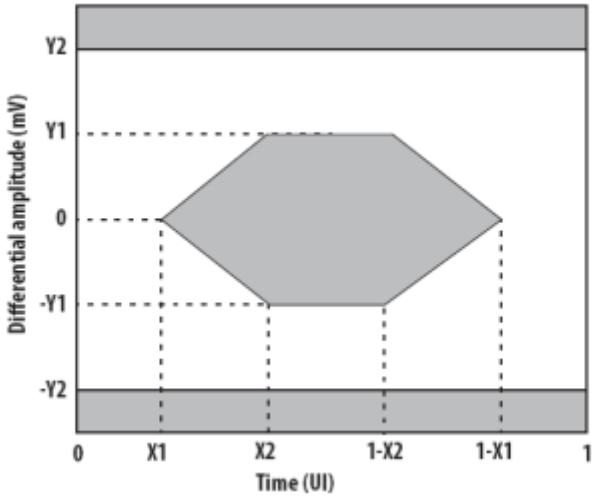


Test Procedure:

Part A: TP1a Calibration of Test Equipment

1. Screen Capture Eye mask
2. Capture 1000 waveforms.
3. Verify Eye Mask Margin: Ensure that the TP1a measurement passes the IEEE 802.3-2012 specification.

X1, X2, Y1, Y2 = 0.11UI, 0.31UI, 95mV, 350mV



4. Repeat this process for all four lanes. In the event of a DUT exhibiting unexpected behavior during other testing, these values may be used to further evaluate issues. Note that only Lane 2 will be used initially for further tests in section 4.2.

Observable results:

Part A:

- Informational - Establish baseline of test equipment as reference for additional tests. Verify the Mask Margin > 0%.

Possible Problems: None

Test 4.3.2 - 40G QSFP+ Golden Module Verification for SR Variants

Purpose: To record the optical output eye mask margin of the Golden Optical Unit

NOTE: This measurement needs to only to be done at the beginning of module testing and not for every module under test.

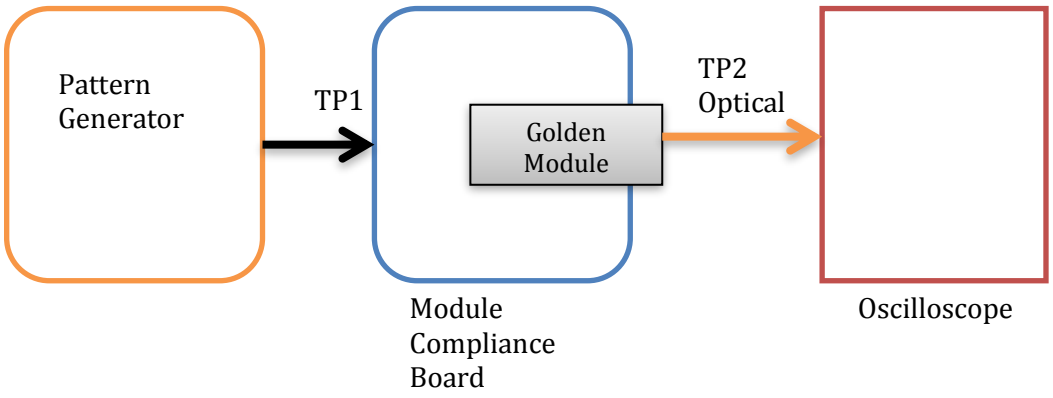
Resource Requirements:

- Compliance Signal Generator
- Crosstalk Signal Generator
- Module Compliance Board
- Digital Storage Oscilloscope capable of Optical Measurements
- 2-5m 50um Optical Patch Cable

Discussion: Establishing a baseline allows a reference for all other optical receiver measurements.

Test Setup: The below block diagram is derived from IEEE 802.3-2012.

The test points provided are as follows.
TP1 represents the electrical input signal to the Golden Module.
TP2 represents the output of this module after a 2m-5m patch cord.



Test Procedure:

Part A: Golden Module Verification

1. Instruct the pattern generator to transmit PRBS31.
2. Connect the Golden Module to a 2m-5m patch cord.
3. Connect the Golden Module to the oscilloscope.
4. Capture 1000 waveforms
5. Verify that the eye diagram at TP2 is compliant to an eye mask defined by the following points: X1, X2, X3, Y1, Y2, Y3 = 0.23, 0.34, 0.43, 0.27, 0.35, 0.40.
    e. Hit ratio = 5×10^{-5}

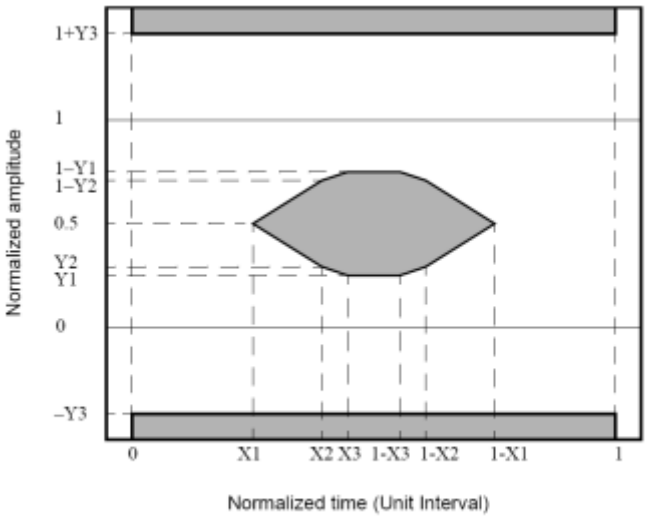


Figure 86–4—Transmitter eye mask definition

6. Repeat this process for all four lanes. In the event of a module under test exhibiting unexpected behavior during other testing, these values may be used to further evaluate issues. Note that only Lane 2 will be used initially for further tests in section 4.2.

Observable results:

Part A:

- Informational - Establish baseline of test equipment as reference for additional tests. Ensure a hit ratio of 5 X 10^{-5}. Verify that the Mask Margin > 0%.

Possible Problems: None

Test 4.3.3 - 40G QSFP+ Golden Module Verification for LR Variants

Purpose: To record the optical output eye mask margin of the Golden Optical Unit

NOTE: This measurement needs to only to be done at the beginning of module testing and not for every module under test.

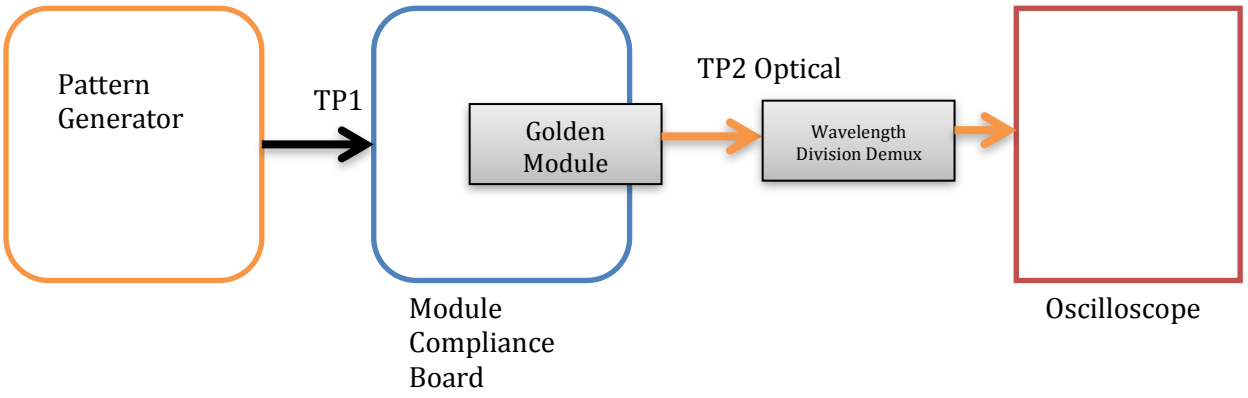
Resource Requirements:

- Compliance Signal Generator
- Crosstalk Signal Generator
- Module Compliance Board
- Digital Storage Oscilloscope capable of Optical Measurements
- Optical Demultiplexer
- 2-5m SMF Optical Patch Cable

Discussion: Establishing a baseline allows a reference for all other optical receiver measurements.

Test Setup: The below block diagram is derived from IEEE 802.3-2012.

The test points provided are as follows.
TP1 represents the electrical input signal to the Golden Module.
TP2 represents the output of this module after a 2m-5m patch cord.



Test Procedure:

Part A: Golden Module Verification

1. Instruct the pattern generator to transmit PRBS31.
2. Connect the Golden Module to a 2m-5m patch cord.
3. Connect the Golden Module to the oscilloscope through a demux.
4. Capture 1000 waveforms
5. Verify that the eye diagram at TP2 is compliant to an eye mask defined by the following points: X1, X2, X3, Y1, Y2, Y3 = 0.25, 0.4, 0.45, 0.25, 0.28, 0.4.

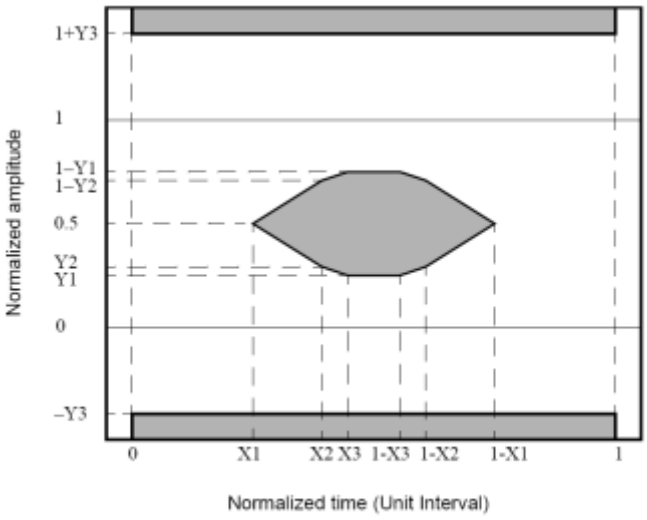


Figure 86–4—Transmitter eye mask definition

6. Repeat this process for all four wavelengths. In the event of a module under test exhibiting unexpected behavior during other testing, these values may be used to further evaluate issues. Note that only L_1 will be used initially (as defined by IEEE Std. 802.3-2012, Table 87-5) for further tests in section 4.4.

Observable results:
Part A:

- There shall be no violations of the eye mask at any point.

Possible Problems: None

Section 4.4: 40GbE QSFP+ Testing for AOCs and Modules

Test 4.4.1 - Transmitter Eye mask for 40G QSFP+ (Modules Only) (SR Variants)

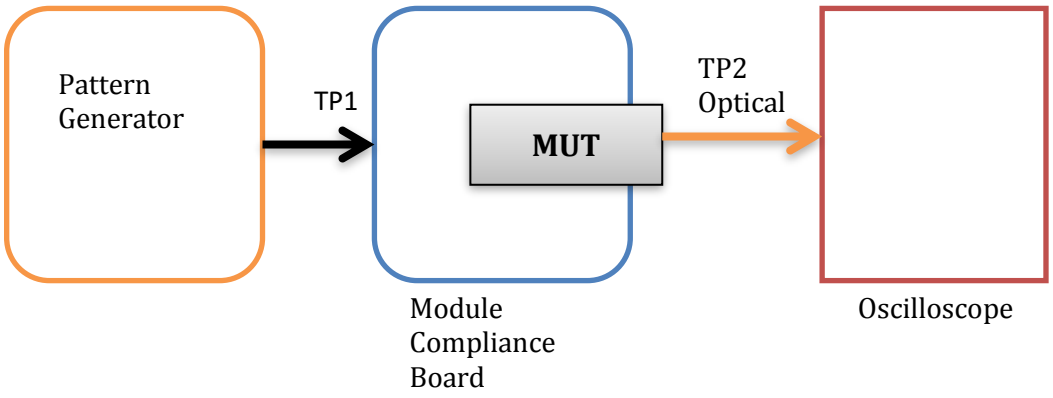
Purpose: To verify that the optical transmitter of the Module under test (MUT) meets the specified requirements.

Resource Requirements:

- Compliance Signal Generator
- Crosstalk Signal Generator
- Module Compliance Board
- Digital Storage Oscilloscope capable of Optical Measurements
- 2-5m 50um Optical Patch Cable

Discussion: A transmitter Eye mask can indicate significant information about the health of a transmitter.

Test Setup: The next block diagram is also derived from IEEE Std. 802.3-2012. TP1 represents the electrical input signal to the DUT. TP2 represents the output of this module after a 2m-5m patch cord.



Test Procedure:

Part A: TP2 Module Verification

1. Record Optical Module part number and serial number
2. Use the board setup and input signals measured in Test 4.2.1.
3. Test lane #2 out of four lanes.
    a. Note: If there is an issue during Link Functionality or Interoperability testing, re-run this test with all four channels using values found in Test 4.2.1.
4. Configure the oscilloscope to capture 1000 waveforms.
5. Insert module under test into the Evaluation Board, connect the optical fiber (breakout cable) to the DCA and capture the following information using test pattern PRBS31:
    a. Optical Eye (screen capture)

b. Optical Mask Margin: PRBS31, 10.3125Gbps, TP2: X1, X2, X3, Y1, Y2, Y3 = 0.23, 0.34, 0.43, 0.27, 0.35, 0.4 UI.
c. Hit Ratio = 5e-5.

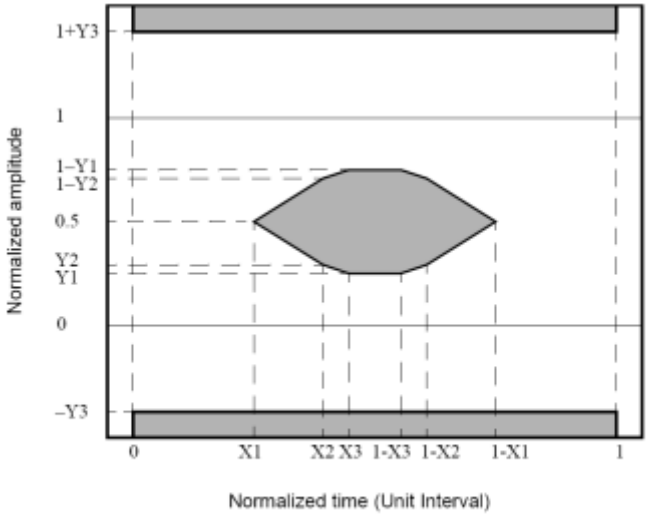


Figure 86–4—Transmitter eye mask definition

Observable results:

Part A:

- Hit ratio shall not exceed 5 x 10^{-5} per sample. Ensure the Mask Margin > 0%

Possible Problems: None

Test 4.4.2 - Transmitter Eye mask for 40G QSFP+ (Modules Only) (LR Variants)

Purpose: To record the optical output eye mask margin of the Golden Optical Unit

NOTE: This measurement needs to only to be done at the beginning of module testing and not for every module under test.

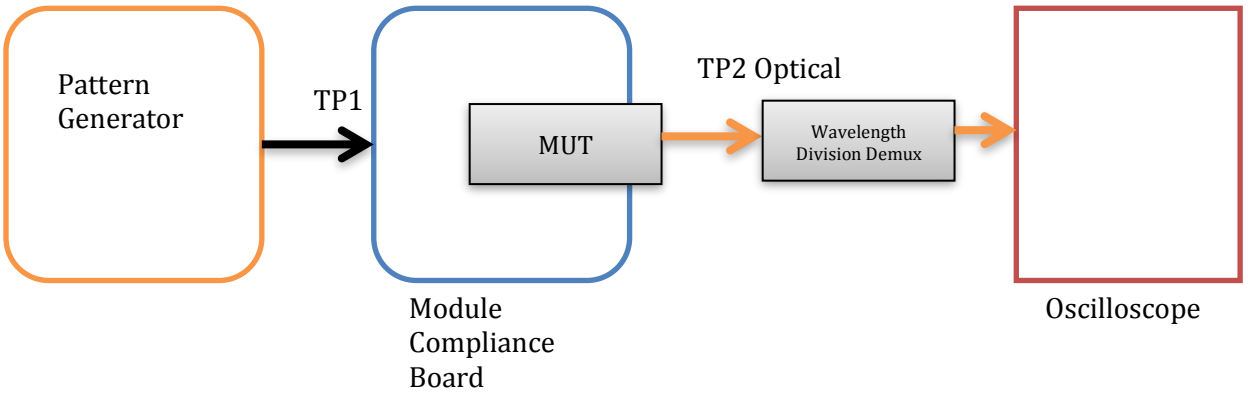
Resource Requirements:

- Compliance Signal Generator
- Crosstalk Signal Generator
- Module Compliance Board
- Digital Storage Oscilloscope capable of Optical Measurements
- Optical Demultiplexer
- 2-5m SMF Optical Patch Cable

Discussion: Establishing a baseline allows a reference for all other optical receiver measurements.

Test Setup: The below block diagram is derived from IEEE 802.3-2012.

The test points provided are as follows.
TP1 represents the electrical input signal to the Golden Module.
TP2 represents the output of this module after a 2m-5m patch cord.



Test Procedure:

Part A: Golden Module Verification

1. Instruct the pattern generator to transmit PRBS31.
2. Connect the Golden Module to a 2m-5m patch cord.
3. Connect the Golden Module to the oscilloscope through a demux.
4. Capture 1000 waveforms
5. Verify that the eye diagram at TP2 is compliant to an eye mask defined by the following points: X1, X2, X3, Y1, Y2, Y3 = 0.25, 0.4, 0.45, 0.25, 0.28, 0.4.

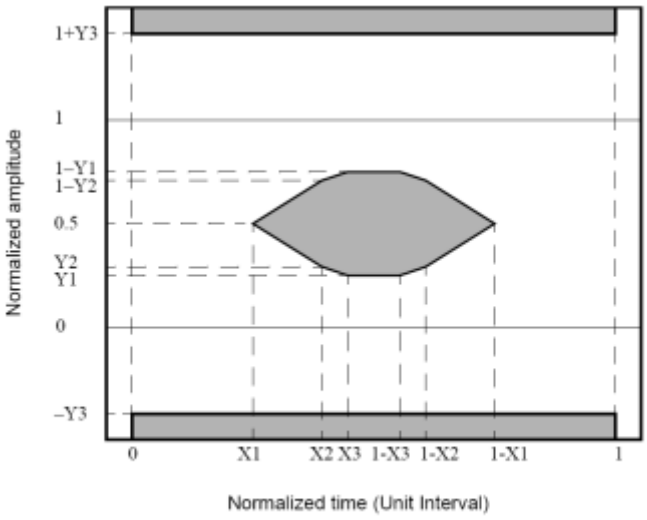


Figure 86–4—Transmitter eye mask definition

6. Repeat this process for all four wavelengths. In the event of a module under test exhibiting unexpected behavior during other testing, these values may be used to further evaluate issues. Note that only L_1 will be used initially (as defined by IEEE Std. 802.3-2012, Table 87-5) for further tests in section 4.4.

Observable results:
Part A:

- There shall be no violations of the eye mask at any point.

Possible Problems: None

Test 4.4.3 - Output eye mask for 40G QSFP+

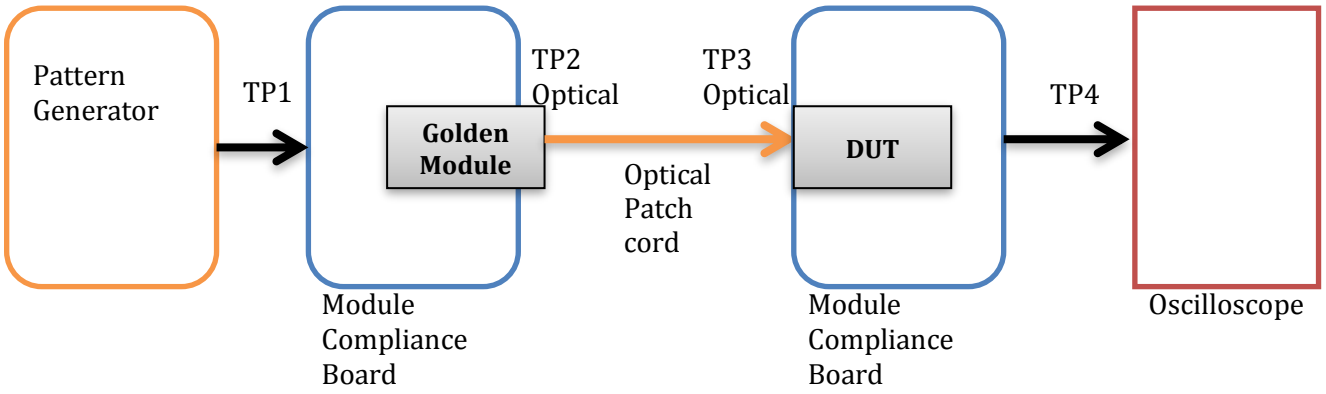
Purpose: To verify that the Device (Module or Cable Assembly) under test (DUT) demonstrates electrical output characteristics that meets the specified requirements.

Resource Requirements:

- Compliance Signal Generator
- Crosstalk Signal Generator
- Module Compliance Boards (2)
- Host Compliance Board
- Digital Storage Oscilloscope
- Golden Module verified by test 4.3.2 or 4.3.3, for either SR or LR variant, respectively (Module Testing Only)

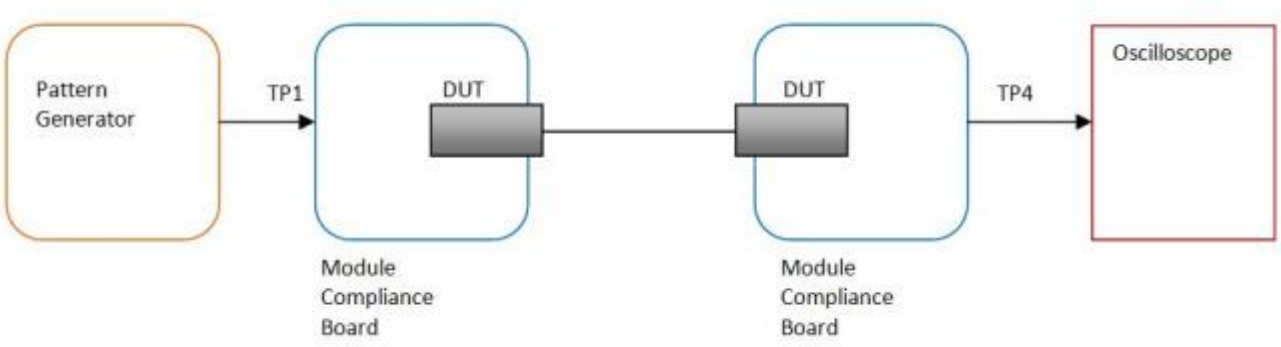
Discussion: An eye mask of the electrical output can indicate significant information about the health of a module's receiver.

Test Setup: This test encompasses electrical output eye mask verification for both Modules and AOCs. Because of this, please note the two setups below describing this test for Modules (top) and AOCs (below).



The above setup describes the physical setup and the test points at various locations in the setup for Modules. For this test, the electrical eye mask will be measured at TP4 (TP4 defined in IEEE 802.3-2012). The electrical output of the DUT is measured through an IEEE Std. 802.3-2012 compliant Module Compliance Board.

The setup below describes the physical setup and the test points at various locations in the setup for AOCs. Notice that TP2 and TP3 are hidden when evaluating AOCs. For this test, the electrical eye mask will be measured at TP4 (TP4 defined in IEEE 802.3 – 2012). The electrical output of the Cable under test is measured through a IEEE Std. 802.3 – 2012 compliant Module Compliance Board.



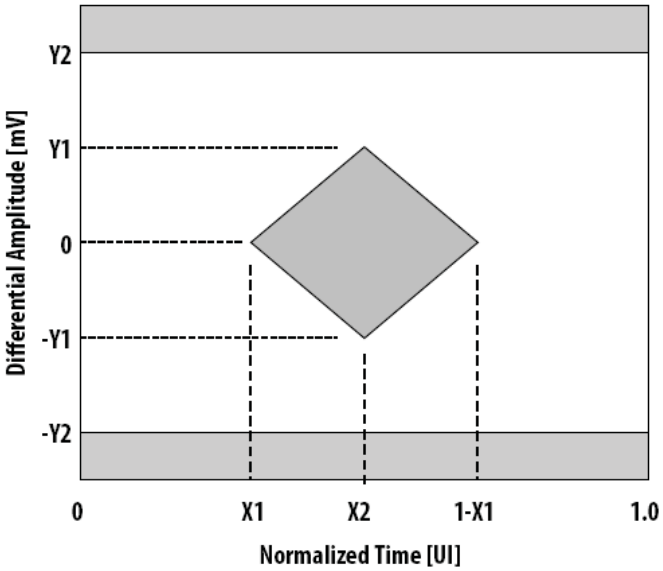
Test Procedure:

Part A: Module TP4 Verification

1. Record Optical Module part number and serial number
2. Use the board setup with the golden optical module results from test 4.3.2 (SR) or 4.3.3 (LR).
3. Test lane #2 out of four lanes.
    a. Note: If there is an issue during Link Functionality or Interoperability testing, re-run this test with all four channels using values found in Test 4.3.1.
4. Insert Module under test into the MCB, and capture the following information using test pattern PRBS31, transmitted using the settings calibrated in test 4.3.1:
    a. Electrical Eye (screen capture).
    b. Capture 1000 waveforms.
    c. Verify that the eye diagram at TP4 is compliant to an eye mask defined by the following points: X1, X2, Y1, Y2 = 0.29UI, 0.5UI, 150mV, 425mV (Figure Below)
    d. Hit ratio = 5×10^{-5}

Part B: Active Optical Cable TP4 Verification

1. Record Optical Cable part number and serial number
2. Test lane #2 out of four lanes.
    a. Note: If there is an issue during Link Functionality or Interoperability testing, re-run this test with all four channels using values found in Test 4.3.1.
3. Insert Cable under test into the setup, capture the following information using test pattern PRBS31, transmitted using the settings calibrated in test 4.3.1:
    a. Electrical Eye (screen capture).
    b. Capture 1000 waveforms.
    c. Verify that the eye diagram at TP4 is compliant to an eye mask defined by the following points: X1, Y1, Y2 = 0.29UI, 0.5UI, 150mV, 425mV (Figure Below)
    d. Hit ratio = 5×10^{-5}



Observable results:

Part A:

- Hit ratio shall not exceed 5 x 10^{-5} per sample. Ensure the Mask Margin > 0%.

Part B:

- Hit ratio shall not exceed 5 x 10^{-5} per sample. Ensure the Mask Margin > 0%.

Possible Problems: None

Section 4.5: Test Equipment Calibration for 25G SFP28 or 100G QSFP28 AOCs and Modules

Test 4.5.1 – Calibration for 25G SFP28 or 100G QSFP28 Module and AOC Testing

Purpose: To establish Electrical TP1a input baseline to the QSFP+ optical cables, optical modules and copper cables.

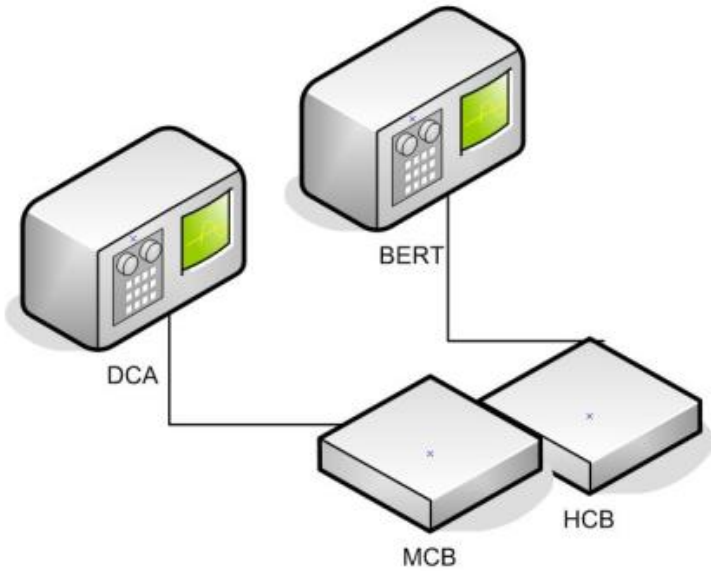
NOTE: This measurement needs to only to be done at the beginning of module testing and not for every module or cable under test.

Resource Requirements:

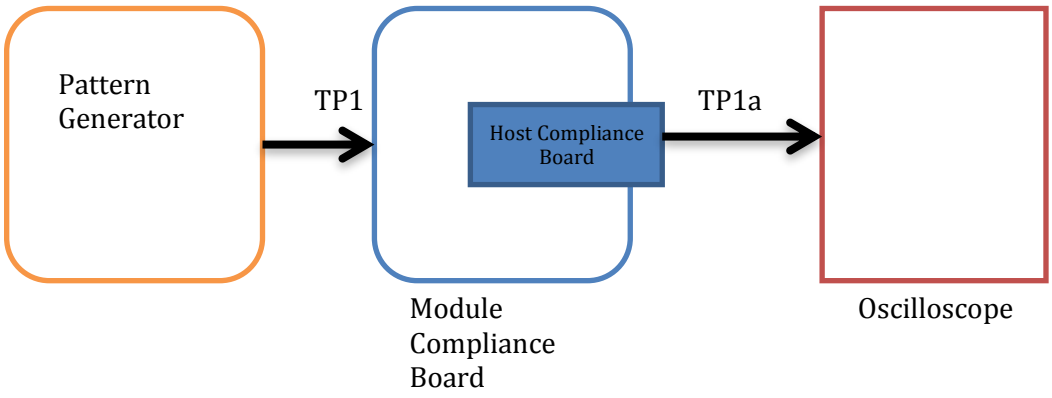
- Compliance Signal Generator
- Crosstalk Signal Generator
- Module Compliance Boards (2)
- Host Compliance Board
- Digital Storage Oscilloscope

Discussion: Establishing a baseline allows a reference for all other optical measurements.

Test Setup: Throughout the test plan, lane two [of lanes 1, 2, 3, 4] shall be used for evaluation, while other lanes will be active and terminated. Below is a simplified diagram describing calibration points for our test plan. Specifically, setups defined in IEEE Std. 802.3bm, Annex 83E are used to produce a compliant test signal from the pattern generator.



The below block diagram is derived from IEEE 802.3-2012. The test points provided are as follows: TP1 represents a test point before the electrical input of the MCB. TP1a represents the point of calibration for the pattern generator. This setup is used to calibrate the pattern generator's output in order to ensure that a compliant eye diagram is recovered at TP1a. Note that the lane tested shall be lane two, while all other lanes will be active and terminated.



The measurements taken differ from those in Sections 4.1 through 4.4.

In this test, the transmitter eye width is measured by leveraging the Dual-Dirac jitter model to estimate random jitter on a cumulative density function (CDF) created from a differential equalized signal. The DUT is instructed to transmit Pattern 4, and there should be sufficient samples to allow for a CDF to a probability of $\mathbf{10^{-6}}$ without extrapolation. The CDF for the left and right edges of the eye diagram are linear fit to yield the random jitter for the left and right edges (RJR, RJL), which then uses equation 83E-7 to extrapolate the eye width from $\mathbf{10^{-6}}$ probability to the desired $\mathbf{10^{-15}}$ probability:

$$EW15 = EW6 - 3.19 * (RJR + RJL) \ (83E-7)$$

The transmitter eye height is found by finding the central 5% of the signal at both logic 1 and logic 0. A CDF is created for each level, which are linear fit in Q-scale over the range of probabilities of 10-4 and 10-6 which yield relative noise 1 (RN1) and relative noise 0 (RN0). Equation 83E-8 is used to extrapolate the eye height from 10-6 probability to the desired 10-15 probability:

$$EH15 = EH6 - 3.19 * (RN0 + RN1) \ (83E-8)$$

Test Procedure:

Part A: TP1a Calibration of Test Equipment

1. Screen Capture Eye
2. Capture 1000 waveforms.
3. Repeat this process for all four lanes. In the event of a DUT exhibiting unexpected behavior during other testing, these values may be used to further evaluate issues. Note that only Lane 2 will be used initially for further tests in section 4.2.
4. Calculate EW15 and EH15.

Observable results:

Part A:

- EW15 shall be less than 0.46UI
- EH15 shall be at least 95 mV at the CTLE configuration which provides the best result.

Possible Problems: None

Test 4.5.2 – 25G SFP28 or 100G QSFP28 Golden Module Verification for SR Variants

Purpose: To record the optical output eye mask margin of the Golden Optical Unit

NOTE: This measurement needs to only to be done at the beginning of module testing and not for every module under test.

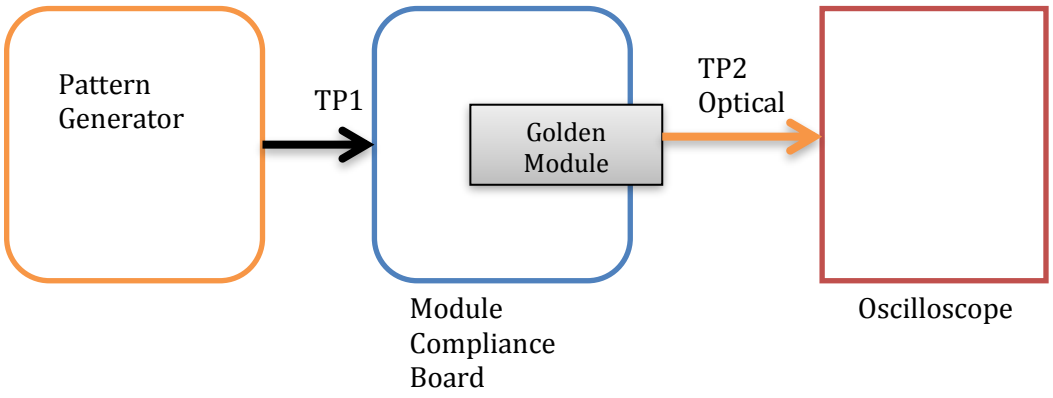
Resource Requirements:

- Compliance Signal Generator
- Crosstalk Signal Generator
- Module Compliance Board
- Digital Storage Oscilloscope capable of Optical Measurements
- 2-5m 50um Optical Patch Cable

Discussion: Establishing a baseline allows a reference for all other optical receiver measurements.

Test Setup: : The below block diagram is derived from IEEE 802.3-2012.

The test points provided are as follows.
TP1 represents the electrical input signal to the Golden Module.
TP2 represents the output of this module after a 2m-5m patch cord.



Test Procedure:

Part A: Golden Module Verification

1. Instruct the pattern generator to transmit PRBS31.
2. Connect the Golden Module to a 2m-5m patch cord.
3. Connect the Golden Module to the oscilloscope.
4. Capture 1000 waveforms
5. Verify that the eye diagram at TP2 is compliant to an eye mask defined by the following points: X1, X2, X3, Y1, Y2, Y3 = 0.3, 0.38, 0.45, 0.35, 0.41, 0.5
    f. Hit ratio = 1.5×10^{-3}

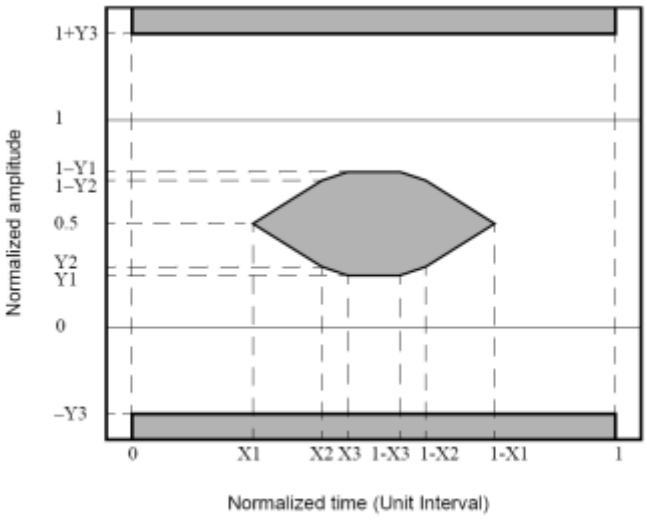


Figure 86–4—Transmitter eye mask definition

6. Repeat this process for all four lanes. In the event of a module under test exhibiting unexpected behavior during other testing, these values may be used to further evaluate issues. Note that only Lane 2 will be used initially for further tests in section 4.2.

Observable results:

Part A:

- Informational - Establish baseline of test equipment as reference for additional tests. Ensure a hit ratio of 1.5 X 10^{-3}. Verify that the Mask Margin > 0%.

Possible Problems: None

Test 4.5.3 – 25G SFP28 or 100G QSFP28 Golden Module Verification for LR Variants

Purpose: To record the optical output eye mask margin of the Golden Optical Unit

NOTE: This measurement needs to only to be done at the beginning of module testing and not for every module under test.

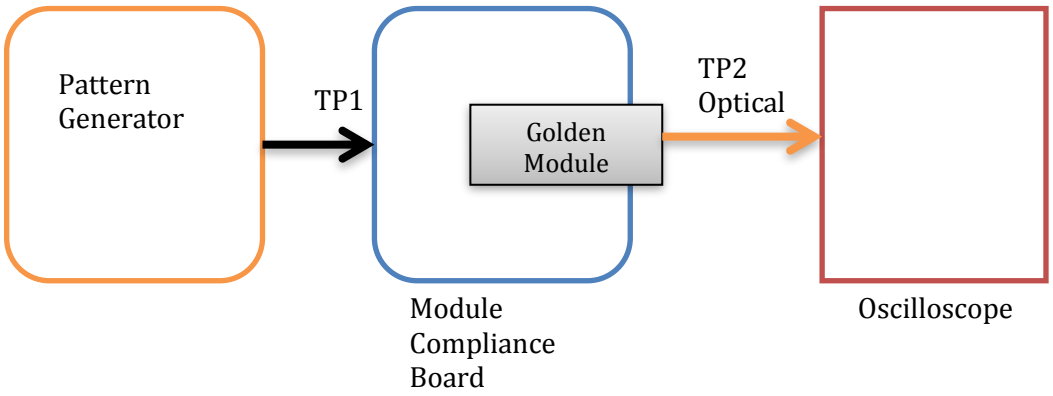
Resource Requirements:

- Compliance Signal Generator
- Crosstalk Signal Generator
- Module Compliance Board
- Digital Storage Oscilloscope capable of Optical Measurements
- Optical Demultiplexer
- 2-5m SMF Optical Patch Cable

Discussion: Establishing a baseline allows a reference for all other optical receiver measurements.

Test Setup: : The below block diagram is derived from IEEE 802.3-2012.

The test points provided are as follows.
TP1 represents the electrical input signal to the Golden Module.
TP2 represents the output of this module after a 2m-5m patch cord.



Test Procedure:

Part A: Golden Module Verification

1. Instruct the pattern generator to transmit PRBS31.
2. Connect the Golden Module to a 2m-5m patch cord.
3. Connect the Golden Module to the oscilloscope.
4. Capture 1000 waveforms
5. Verify that the eye diagram at TP2 is compliant to an eye mask defined by the following points: X1, X2, X3, Y1, Y2, Y3 = 0.25, 0.4, 0.45, 0.25, 0.28, 0.4

Observable results:
Part A:

- Informational - Establish baseline of test equipment as reference for additional tests. The eye mask may not be violated at any point.

Possible Problems: None

Section 4.6: 25G SFP28 or 100G QSFP28 Testing for AOCs and Modules

Test 4.6.1 - Transmitter Eye Verification for 25G SFP28 or 100G QSFP28 (Modules Only) (SR Variants)

Purpose: To verify that the optical transmitter of the Module under test (MUT) meets the specified requirements.

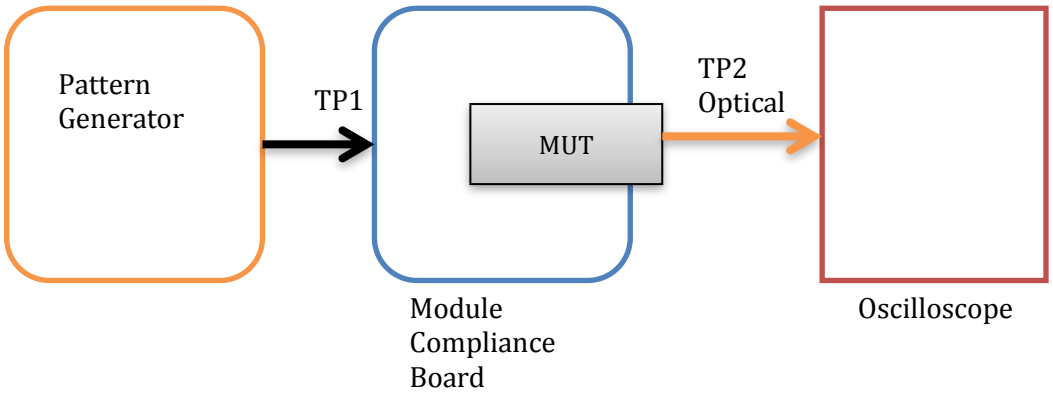
Resource Requirements:

- Compliance Signal Generator
- Crosstalk Signal Generator
- Module Compliance Board
- Digital Storage Oscilloscope capable of Optical Measurements
- 2-5m 50um Optical Patch Cable

Discussion: A transmitter Eye mask can indicate significant information about the health of a transmitter.

Test Setup: : The below block diagram is derived from IEEE 802.3-2012.

The test points provided are as follows.
TP1 represents the electrical input signal to the Golden Module.
TP2 represents the output of this module after a 2m-5m patch cord.



Test Procedure:

Part A: MUT Verification

1. Instruct the pattern generator to transmit PRBS31.
2. Connect the Module to the oscilloscope.
3. Capture 1000 waveforms
4. Verify that the eye diagram at TP2 is compliant to an eye mask defined by the following points: X1, X2, X3, Y1, Y2, Y3 = 0.3, 0.38, 0.45, 0.35, 0.41, 0.5

a. Hit ratio = 1.5 X 10^{-3}

Observable results:
Part A:

- Ensure a hit ratio of 1.5 X 10^{-3}. Verify that the Mask Margin > 0%.

Possible Problems: None

Test 4.6.2 - Transmitter Eye Verification for 25G SFP28 or 100G QSFP28 (Modules Only) (LR Variants)

Purpose: To record the optical output eye mask margin of the Golden Optical Unit

NOTE: This measurement needs to only to be done at the beginning of module testing and not for every module under test.

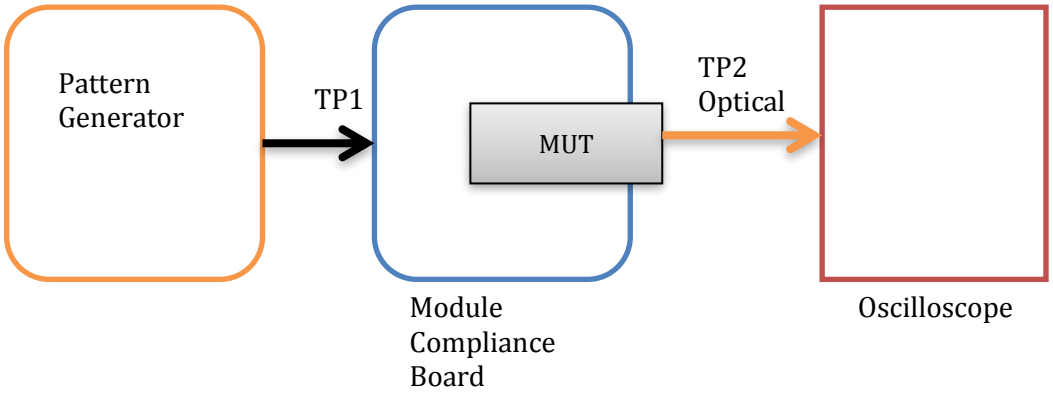
Resource Requirements:

- Compliance Signal Generator
- Crosstalk Signal Generator
- Module Compliance Board
- Digital Storage Oscilloscope capable of Optical Measurements
- Optical Demultiplexer
- 2-5m SMF Optical Patch Cable

Discussion: Establishing a baseline allows a reference for all other optical receiver measurements.

Test Setup: : The below block diagram is derived from IEEE 802.3-2012.

The test points provided are as follows.
TP1 represents the electrical input signal to the Golden Module.
TP2 represents the output of this module after a 2m-5m patch cord.



Test Procedure:

Part A: MUT Verification

1. Instruct the pattern generator to transmit PRBS31.
2. Connect the Module to the oscilloscope.
3. Capture 1000 waveforms
4. Verify that the eye diagram at TP2 is compliant to an eye mask defined by the following points: X1, X2, X3, Y1, Y2, Y3 = 0.25, 0.4, 0.45, 0.25, 0.28, 0.4

Observable results:
Part A:

- The DUT's transmitter shall not be violate the eye mask at any point.

Possible Problems: None

Test 4.6.3 - Output eye mask for 25G SFP28 or 100G QSFP28

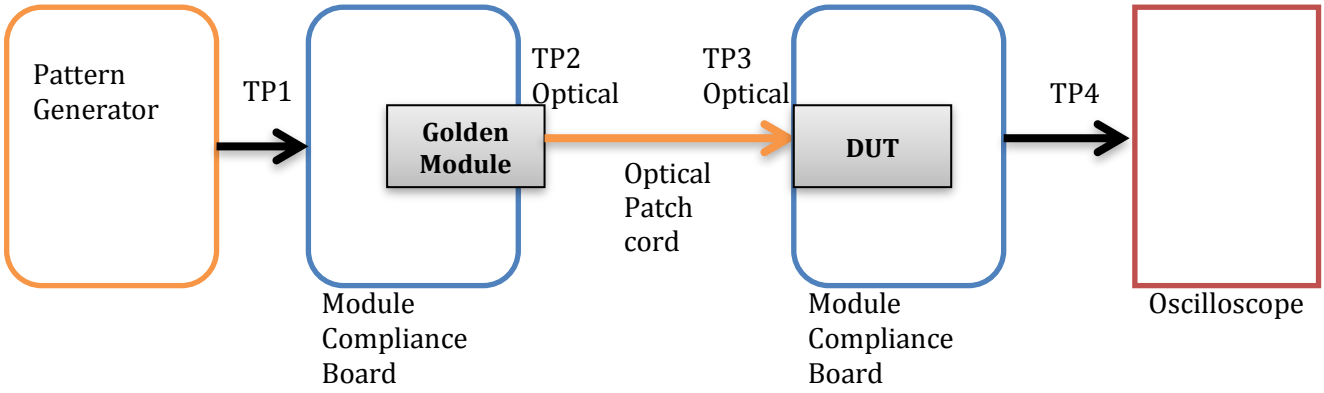
Purpose: To verify that the Device (Module or Cable Assembly) under test (DUT) demonstrates electrical output characteristics that meets the specified requirements.

Resource Requirements:

- Compliance Signal Generator
- Crosstalk Signal Generator
- Module Compliance Boards (2)
- Host Compliance Board
- Digital Storage Oscilloscope
- Golden Module verified by test 4.5.2 or 4.5.3, for either SR or LR variant, respectively (Module Testing Only)

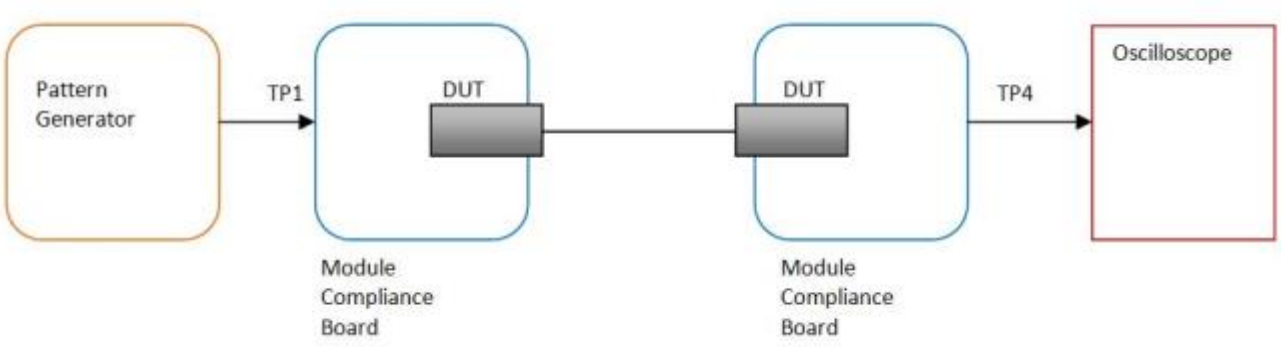
Discussion: An eye mask of the electrical output can indicate significant information about the health of a module's receiver.

Test Setup: This test encompasses electrical output eye mask verification for both Modules and AOCs. Because of this, please note the two setups below describing this test for Modules (top) and AOCs (below).



The above setup describes the physical setup and the test points at various locations in the setup for Modules.

The setup below describes the physical setup and the test points at various locations in the setup for AOCs. Notice that TP2 and TP3 are hidden when evaluating AOCs.



The measurements taken differ from those in Sections 4.1 through 4.4.

In this test, the transmitter eye width is measured by leveraging the Dual-Dirac jitter model to estimate random jitter on a cumulative density function (CDF) created from a differential equalized signal. The DUT is instructed to transmit Pattern 4, and there should be sufficient samples to allow for a CDF to a probability of $\mathbf{10^{-6}}$ without extrapolation. The CDF for the left and right edges of the eye diagram are linear fit to yield the random jitter for the left and right edges (RJR, RJL), which then uses equation 83E-7 to extrapolate the eye width from $\mathbf{10^{-6}}$ probability to the desired $\mathbf{10^{-15}}$ probability:

$$EW15 = EW6 - 3.19 * (RJR + RJL) \ (83E-7)$$

The transmitter eye height is found by finding the central 5% of the signal at both logic 1 and logic 0. A CDF is created for each level, which are linear fit in Q-scale over the range of probabilities of 10-4 and 10-6 which yield relative noise 1 (RN1) and relative noise 0 (RN0). Equation 83E-8 is used to extrapolate the eye height from 10-6 probability to the desired 10-15 probability:

$$EH15 = EH6 - 3.19 * (RN0 + RN1) \ (83E-8)$$

Test Procedure:

Part A: Module TP4 Verification

1. Record Optical Module part number and serial number
2. Use the board setup with the golden optical module results from test 4.6.2 (SR) or 4.6.3 (LR).
3. Test lane #2 out of four lanes.
    a. Note: If there is an issue during Link Functionality or Interoperability testing, re-run this test with all four channels using values found in Test 4.6.1.
4. Insert Module under test into the MCB, and capture the following information using test pattern PRBS31, transmitted using the settings calibrated in test 4.6.1:
    a. Electrical Eye (screen capture).
    b. Capture 1000 waveforms.
    c. Verify that the EH15 measurement is at least 228 mV
    d. Verify that the EW15 measurement is at least 0.57 UI

Part B: Active Optical Cable TP4 Verification

1. Record Optical Cable part number and serial number
2. Test lane #2 out of four lanes.

   a. Note: If there is an issue during Link Functionality or Interoperability testing, re-run this test with all four channels using values found in Test 4.6.1.
3. Insert Cable under test into the setup, capture the following information using test pattern PRBS31, transmitted using the settings calibrated in test 4.5.1:
   a. Electrical Eye (screen capture).
   b. Capture 1000 waveforms.
   c. Verify that the EH15 Measurement is at least 228 mV
   d. Verify that the EW15 Measurement is at least 0.57 UI

Observable results:

Part A & B:

- EH15 shall be at least 228 mV at the CTLE configuration that provides the best result.
- EW15 shall be at least 0.57 UI

Possible Problems: Please note that hardware and software capable of continuous time-linear equalization (CTLE) is necessary for performing the EH51 and EW15 measurements.

Group 5: Host Module Electrical Verification

Overview: The tests defined in this section verify the electrical signaling characteristics of the host module. These tests are distinguished based on speed and are represented as sections of such.

For all tests in this section, if the tests have been previously performed on the hardware, and the firmware has not been changed, there is no need to perform the tests again if the hardware is being testing with a new or updated NOS in Group 6. Results previously obtained can be used.

Further, if a preferred test mode described in the test procedure is not available in the HUT, an alternate test mode may be used at the discretion of the test technician.

Section 5.1: Electrical Verification of 10G Host

Test 5.1.1 - Output Rise and Fall Times for 10G Host

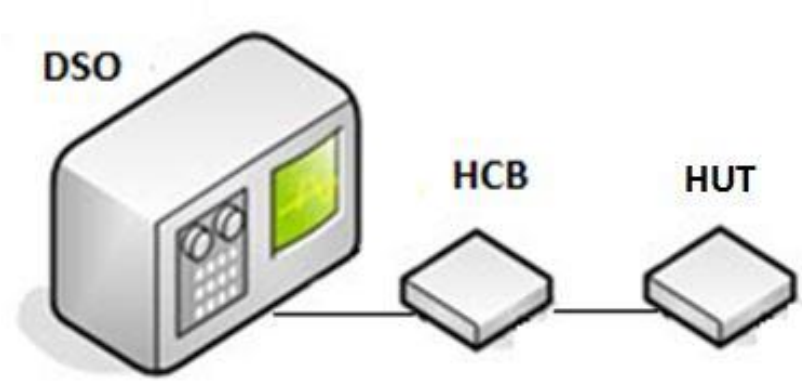
Purpose: To verify that the Output Rise and Fall Times are within the conformance limits.

Resource Requirements:

- Digital Storage Oscilloscope
- Host Compliance Board

Discussion: In this test, the transition time is measured while the host under test is connected to the DSO. The transition times are to be measured at the 20% and 80% levels. The measurement is done using the square wave test pattern defined.

Test Setup: The host's output is connected to the host compliance board which is then connected to the DSO. The DSO should be properly calibrated before use.



Test Procedure:

Part A: Transition Time Verification

1. Configure the host under test so that it is sourcing a square wave with no equalization.
2. Connect the host under test's transmitter to the DSO.
3. Measure the rising and falling edge transition times.

Observable Results:

Part A:

- The rising and falling edge transition times should not be less than 34ps.

Possible Problems: None

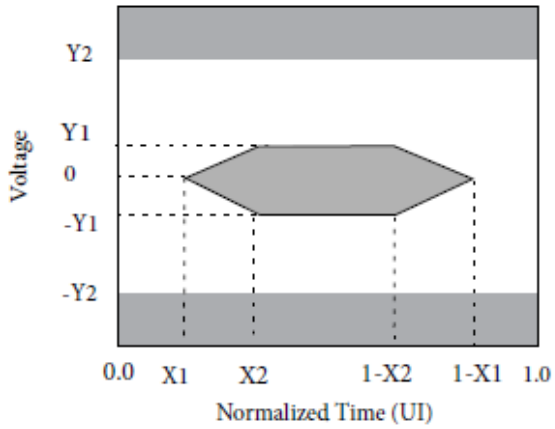
Test 5.1.2 - Transmitter Eye Mask for 10G Host

Purpose: To verify that the Eye Mask Hit Ratio is within the conformance limits.

Resource Requirements:

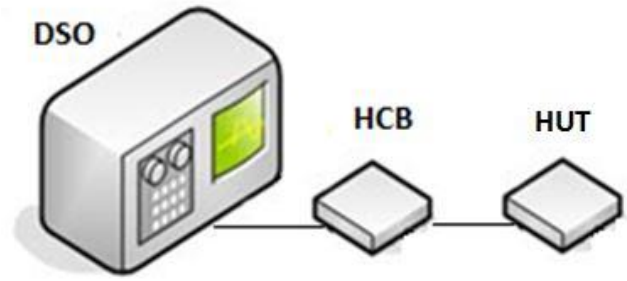
- Digital Storage Oscilloscope
- Host Compliance Board

Discussion: In this test, the eye mask is measured while the host under test is connected to DSO. The host will transmit PRBS31.



X1=0.12 UI X2=0.33 UI Y1=95 mV Y2=350 mV

Test Setup: The host's output is connected to the host compliance board which is then connected to the DSO. The DSO should be properly calibrated before use.



Test Procedure:

Part A: Eye Mask Margin Verification

1. Configure the host under test so that it is sourcing PRBS31.
2. Connect the host under test's transmitter to DSO.
3. Capture the eye mask.

Observable Results:

Part A:

- Hit ratio shall not exceed 5 x 10^{-5} per sample. Ensure the Mask Margin > 0%

Possible Problems: None

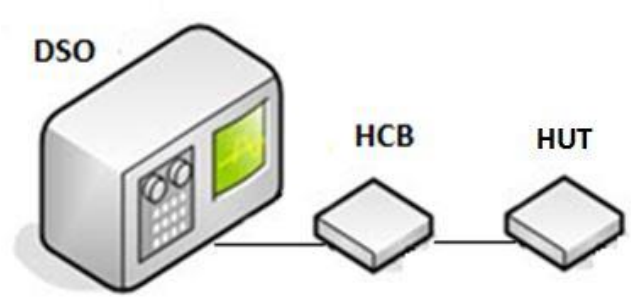
Test 5.1.3 - Total Jitter for 10G Host

Purpose: To verify that the Total Jitter (TJ) is within the conformance limits.

Resource Requirements:
- Digital Storage Oscilloscope
- Host Compliance Board

Discussion: Total jitter is defined as the sum of the deterministic jitter and random jitter. Test pattern PRBS31 will be used.

Test Setup: The DUT output is connected to the host compliance board which is then connected to the DSO. The DSO should be properly calibrated before use.



Test Procedure:
Part A: Jitter Compliance
1. Set the host under test to transmit PRBS31.
2. Connect the host under test's transmitter to DSO.
3. Measure the total jitter.

Observable Results:
Part A:
- The total jitter should not exceed 0.28 UI(p-p)

Possible Problems: None

Test 5.1.4 - Input and Output Return Loss on 10G Host

Purpose: To verify that the differential input and output return loss of the Host under test is within the conformance limits.

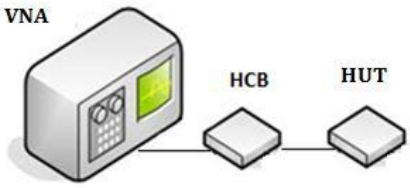
Resource Requirements:

- Network Analyzer
- Host Compliance Board

Discussion: For the purpose of this test, the differential output return loss is defined as the magnitude of the reflection coefficient expressed in decibels. The reflection coefficient is the ratio of the voltage in the reflected wave to the voltage in the incident wave. Note that this is also known as the SDDxx scattering parameter (s-parameter). SDD11 shall be considered the Differential Input Return Loss, and SDD22 shall be considered the Differential Output Return Loss for frequencies from 10MHz to 11.1GHz, the limiting equation from SFF-8431 is provided below:

$$SDD11, SDD22 = \begin{cases} -12, & 10MHz \leq f < 2GHz \\ -6.68 + 12.1 \log_{10} \frac{f}{5.5}, & 2GHz \leq f \leq 11.1GHz \end{cases}$$

Test Setup: The following diagram describes the test layout.



Test Procedure:

Part A: Input and Output Return Loss Verification

1. Calibrate the VNA to remove the effects of the coaxial cables.
2. Configure the DUT so that it is sourcing normal IDLE signaling.
3. Connect the DUT's transmitter to the VNA.
4. Measure the reflection coefficient at the DUT transmitter from 10 MHz to 11.1 GHz.
5. Compute the return loss from the reflection coefficient values.

Observable Results:

Part A:

- The differential return loss shall not violates the limits designated by the governing equations.

Possible Problems: None.

Section 5.2: Electrical Analysis of 40G Host

Test 5.2.1 - Output Rise and Fall Times for 40G Host

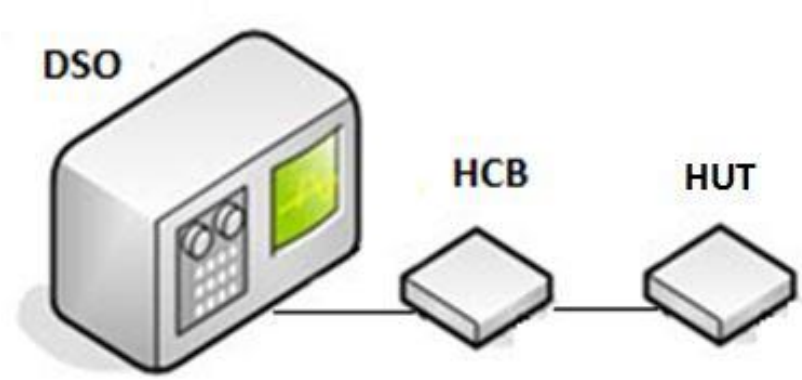
Purpose: To verify that the Output Rise and Fall Times are within the conformance limits.

Resource Requirements:

- Digital Storage Oscilloscope
- Host Compliance Board

Discussion: In this test, the transition time is measured while the host under test is connected to the DSO. The transition times are to be measured at the 20% and 80% levels. The measurement is done using the square wave test pattern defined.

Test Setup: The host's output is connected to the host compliance board which is then connected to the DSO. The DSO should be properly calibrated before use.



Test Procedure:

Part A: Transition Time Verification

1. Configure the host under test so that it is sourcing a square wave with no equalization.
2. Connect the host under test's transmitter to the DSO.
3. Measure the rising and falling edge transition times.

Observable Results:

Part A:

- The rising and falling edge transition times should not be less than 28ps.

Possible Problems: None

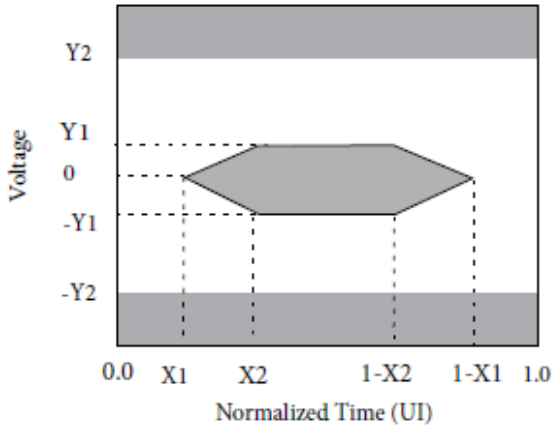
Test 5.2.2 - Transmitter Eye Mask on 40G Host

Purpose: To verify that the UI and amplitude values of the eye mask are within the conformance limits.

Resource Requirements:

- Digital Storage Oscilloscope
- Host Compliance Board

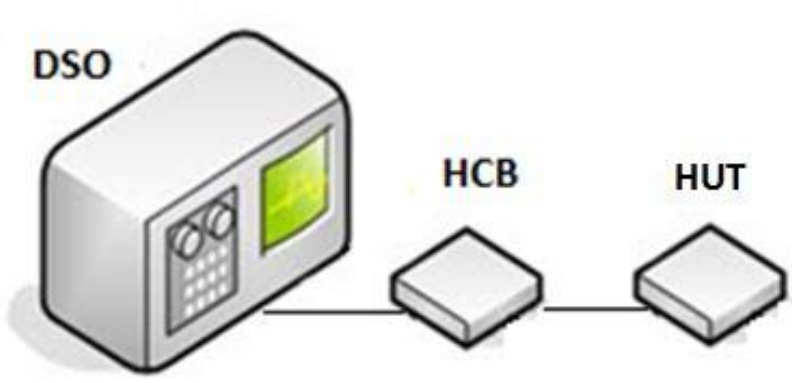
Discussion: IEEE Std. 802.3-2012 Clause 86 specifies the transmitter characteristics for 40GBASE-SR4 devices. This includes conformance requirements for the eye mask defined at the following points:



X1 = 0.11 UI X2 = 0.31 UI Y1 = 95mV Y2 = 350mV

The host under test shall transmit PRBS31 as defined by this standard. If the host under test is incapable of transmitting PRBS31, then Scrambled Idle may be used.

Test Setup: The host under test's output is connected to the host compliance board which is then connected to the DSO. The DSO should be properly calibrated before use.



Test Procedure:

Part A: Eye Mask Margin Verification

1. Configure the host under test so that it is sourcing PRBS31.
2. Connect the host under test's transmitter to DSO.
3. Capture the eye mask.

Observable Results:

Part A:

- Hit ratio shall not exceed 5×10^{-5} per sample. Ensure the Mask Margin > 0%

Possible Problems: None

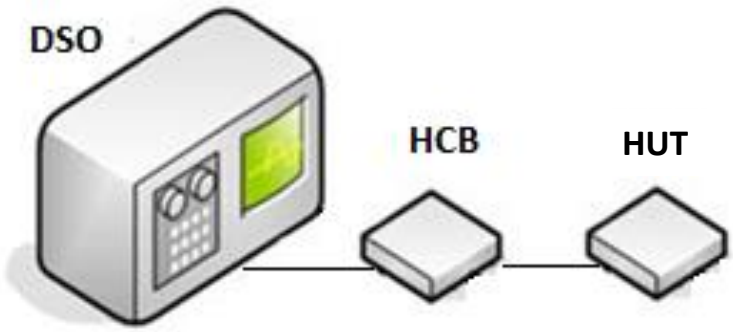
Test 5.2.3 - Jitter Output for 40G Host

Purpose: To verify that the Total Jitter (TJ) is within the conformance limits.

Resource Requirements:
- Digital Storage Oscilloscope
- Host Compliance Board

Discussion: IEEE Std. 802.3-2012 Clause 86 defines the characteristics of 40G devices. Included are requirements for J2 and J9 values for conformance. This test will verify that a host's jitter output is compliant to the standard. During the test, the host must be transmitting PRBS31 with the operating system active.

Test Setup: The following diagram describes the test layout.



Test Procedure:
Part A: Jitter Compliance
1. Configure the host under test to transmit PRBS31 continuously.
2. Connect the host under test's transmitter to the DSO.
3. Measure the J2 and J9 jitter.

Observable Results:
Part A:
1. J2 must be less than or equal to 0.17UI
2. J9 must be less than or equal to 0.29UI

Possible Problems: None

Test 5.2.4 - Input and Output Return Loss on 40G Host

Purpose: To verify that the differential input and output return loss of the host under test is within the conformance limits.

Resource Requirements:

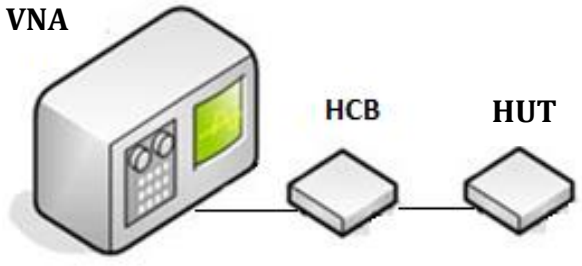
- Network Analyzer
- Host Compliance Board

Discussion: IEEE Std. 802.3-2012, sub clause 86A.4.1.1 specifies the transmitter characteristics for 40GBASE-SR4 and 100GBASE-SR10 devices. This specification includes conformance requirements for the differential input and output return loss. For the purpose of this test, the differential return loss is defined as the magnitude of the reflection coefficient expressed in decibels. The reflection coefficient is the ratio of the voltage in the reflected wave to the voltage in the incident wave. For frequencies from 10 MHz to 11.1 GHz, the differential return loss of the driver shall not exceed the limit given in Equation 86A-1 and Equation 86A-2 (same):

$$\boldsymbol{SDD11, SDD22} = \begin{cases} \boldsymbol{-12 + 2\sqrt{f},\ 10MHz \leq f < 4.11GHz} \\ \boldsymbol{-6.3 + 13\log_{10}\frac{f}{5.5},\ 4.11GHz \leq f \leq 11.1GHz} \end{cases}$$

This value is to be verified for each of the four lanes, which are identified as Lane 0, Lane1, Lane 2 and Lane 3.

Test Setup: The following diagram describes the test layout.



Test Procedure:

Part A: Input and Output Return Loss Verification

1. Calibrate the VNA to remove the effects of the coaxial cables.
2. Configure the host under test so that it is sourcing normal IDLE signaling.
3. Connect the host under test's transmitter to the VNA.
4. Measure the reflection coefficient at the DUT transmitter from 10 MHz to 11.1 GHz.
5. Compute the return loss from the reflection coefficient values.
6. Repeat steps 3 through 5 for all lanes.

Observable Results:

Part A:

- The differential input return loss shall exceed the limits described by Equation 86A-2.

Section 5.3: Electrical Analysis of 25G or 100G Host

Test 5.3.1 - Output Rise and Fall Times for 25G or 100G Host

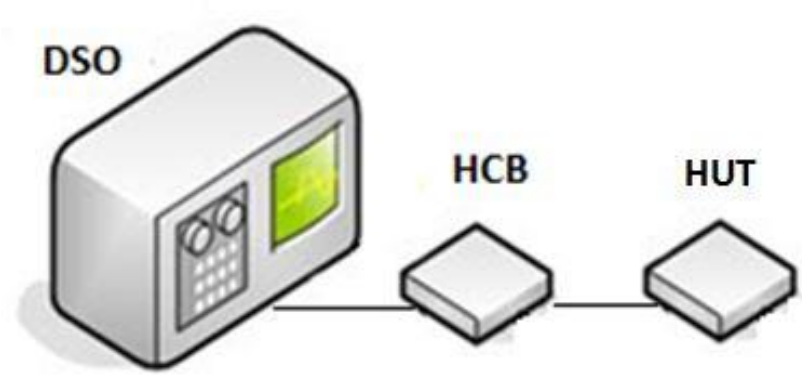
Purpose: To verify that the Output Rise and Fall Times are within the conformance limits.

Resource Requirements:

- Digital Storage Oscilloscope
- Host Compliance Board

Discussion: In this test, the transition time is measured while the host under test is connected to the DSO. The transition times are to be measured at the 20% and 80% levels. The measurement is done using the square wave test pattern defined.

Test Setup: The host's output is connected to the host compliance board which is then connected to the DSO. The DSO should be properly calibrated before use.



Test Procedure:

Part A: Transition Time Verification

1. Configure the host under test so that it is sourcing a square wave with no equalization.
2. Connect the host under test's transmitter to the DSO.
3. Measure the rising and falling edge transition times.

Observable Results:

Part A:

- The rising and falling edge transition times should not be less than 10ps.

Possible Problems: None

Test 5.3.2 - Transmitter Eye Height and Eye Width Verification

Purpose: To verify that the UI and amplitude values of the eye mask are within the conformance limits.

Resource Requirements:

- Digital Storage Oscilloscope
- Host Compliance Board

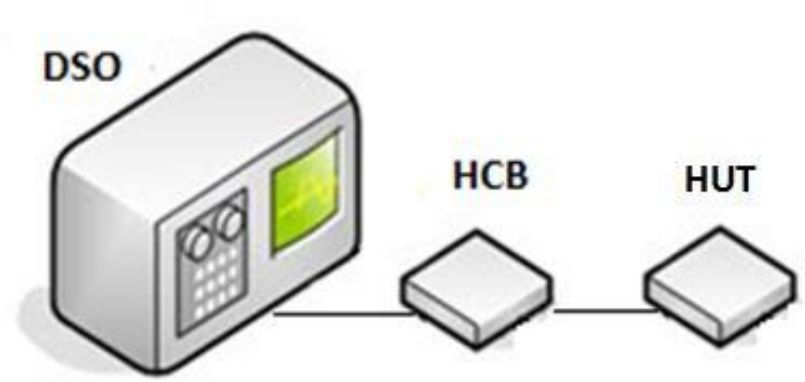
Discussion: In this test, the transmitter eye width is measured by leveraging the Dual-Dirac jitter model to estimate random jitter on a cumulative density function (CDF) created from a differential equalized signal. The DUT is instructed to transmit Pattern 4, and there should be sufficient samples to allow for a CDF to a probability of $\mathbf{10^{-6}}$ without extrapolation. The CDF for the left and right edges of the eye diagram are linear fit to yield the random jitter for the left and right edges (RJR, RJL), which then uses equation 83E-7 to extrapolate the eye width from $\mathbf{10^{-6}}$ probability to the desired $\mathbf{10^{-15}}$ probability:

$$EW15 = EW6 - 3.19 * (RJR + RJL) \ (83E-7)$$

The transmitter eye height is found by finding the central 5% of the signal at both logic 1 and logic 0. A CDF is created for each level, which are linear fit in Q-scale over the range of probabilities of 10-4 and 10-6 which yield relative noise 1 (RN1) and relative noise 0 (RN0). Equation 83E-8 is used to extrapolate the eye height from 10-6 probability to the desired 10-15 probability:

$$EH15 = EH6 - 3.19 * (RN0 + RN1) \ (83E-8)$$

Test Setup: The host under test's output is connected to the host compliance board which is then connected to the DSO. The DSO should be properly calibrated before use.



Test Procedure:

Part A: Eye Height and Width Verification

1. Setup to Capture Eye Diagram

2. Configure the DUT to transmit PRBS31.
3. Capture 1000 waveforms
4. Calculate EH15, ensure that it is at least 95 mV.
5. Calculate EW15, ensure that it is at least 0.46 UI

Observable Results:

Part A:

- EH15 Measurements must be at least 95 mV.
- EW15 Measurements must be at least 0.46 UI.

Possible Problems: Please note that hardware and software capable of continuous time-linear equalization (CTLE) is necessary for performing the EH51 and EW15 measurements.

Test 5.3.3 - Input and Output Return Loss on 25G or 100G Host

Purpose: To verify that the differential input and output return loss of the host under test is within the conformance limits.

Resource Requirements:

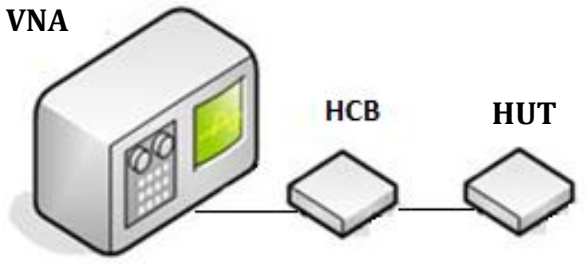
- Network Analyzer
- Host Compliance Board

Discussion: IEEE Std. 802.3bm-2015 specifies the characteristics for 100 CAUI-4 devices. This specification includes conformance requirements for the differential input and output return loss. For the purpose of this test, the differential return loss is defined as the magnitude of the reflection coefficient expressed in decibels. The reflection coefficient is the ratio of the voltage in the reflected wave to the voltage in the incident wave. For frequencies from 10 MHz to 19 GHz, the differential return loss of the driver shall not exceed the limit given in Equation 83E-5:

$$SDD11, SDD22 = \begin{cases} 9.5 - 0.37f & 10MHz \le f < 8GHz \\ 4.75 - 7.4 \log_{10} \frac{f}{14} & 8GHz \le f \le 19GHz \end{cases}$$

This value is to be verified for each of the four lanes, which are identified as Lane 0, Lane1, Lane 2 and Lane 3.

Test Setup: The following diagram describes the test layout.



Test Procedure:

Part A: Input and Output Return Loss Verification

1. Calibrate the VNA to remove the effects of the coaxial cables.
2. Configure the host under test so that it is sourcing normal IDLE signaling.
3. Connect the host under test's transmitter to the VNA.
4. Measure the differential input and output return loss of the DUT.
5. Repeat steps 3 through 5 for all lanes.

Observable Results:

Part A:

1. The differential input return loss shall exceed the limits described by Equation 83E-5

Group 6: Link Functionality

Overview: The following tests cover baseline performance of the host, link detection on power up, BER and the ability for a system to remain functional when receiving packets for an extended period of time. The test described in Group 6 can be applied to 10/40/100G Ethernet links using Mulitmode Fiber, Singlemode Fiber, or copper cables.

Test 6.1 - Establish Baseline Performance Analysis

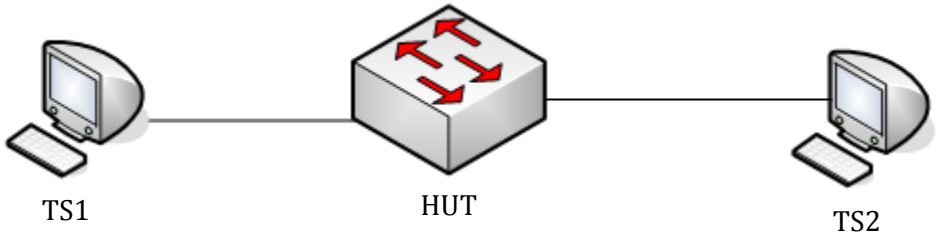
Purpose: To establish a baseline performance analysis of the HUT.

Resource Requirements:

- Four Golden Modules or two Golden Cable Assemblies of the appropriate form factor and type
- Link monitoring and traffic generating capabilities.
- Known good optical fiber cable with appropriate connector assembly

Discussion: This baseline assessment will be performed using known compliant, anonymous Modules or Cable Assemblies to establish a baseline performance of the HUT. The test is designed to create an understanding of performance that can translate through the remaining tests in this section.

Test Setup: The frames transmitted in these tests are defined in Appendix C. The Default Test Setup for the HUT is defined in Appendix D. The following diagram describes the test layout. The Golden Modules or Golden Cable Assemblies are used for all connections.



Test Procedure:

Part A. Link Check

1. Ensure that the Test Setup is configured using the Golden Modules or Golden Cable Assemblies.
2. Transmit Traffic Stream 6.1 A at 1% line rate in order to verify that the link was properly established.

Part B. Baseline the HUT

1. Ensure that the Test Setup is configured using the Golden Modules or Golden Cable Assemblies.
2. Reset all counters that will be used to measure or monitor the exchange of packets
3. Transmit Traffic Stream 6.1 B at 90% line rate.
4. Using the available counters, identify the number of packets received and transmitted.
5. If frame loss occurs, throttle traffic rate to 85% and repeat.
6. Repeat reduction of 5% traffic until all frames are received.
7. Record this baseline percent and use throughout tests in this section.
8. Reboot the HUT.

Observable results:

Part A:

- In step 2, the Golden Modules or Golden Cable Assemblies should create link with the HUT and TS2 should receive all of the frames transmitted by TS1.

Part B:

- In step 4, a baseline percentage should be found for the HUT.

Possible Problems: Due to known issues with some types of test equipment and Direct Attached Copper cables, it may be desirable to use a 'golden module' to attach the HUT to the Testing Station, however a golden module should not be used for this test. If a golden module is used for this test it would eliminate the use of the pluggable module / Cable under test and invalidate the results of testing the Pluggable Module/ Cable/ NOS/ OCP Switch combination. If problems are encountered that appear to be due to incompatibilities between the Testing Station and DAC, a different type of Testing Station should be used, such as another test equipment manufacturer, or a Server with NIC and traffic generation software.

If the link under test is implementing a 100GBASE-SR4 phy, the test herein should be performed with FEC enabled per IEEE 802.3bm Clause 91.

If the link under test is implementing a 25GBASE-CR phy, the test herein should be performed with FEC enabled per IEEE 802.3by Clause 110.

If the link under test is implementing a 100GBASE-CR phy breakout to 25GBASE-CR phy, the test herein should be performed with FEC disabled.

Interoperability problems have been observed between NOS and cable providers. Certain cables supporting 100G operation may indicate support for "0x11 QSFP28" in their EEPROM. Others may indicated support for "0x0D QSFP+ or Later". According to SFF specifications both values are conformant to specifications, however some NOS have been observed not accept both values. Technicians should be aware of this potential issue when performing interoperability testing. If such an issue is observed when testing a particular configuration, that configuration would be considered as failing the requirements outlined in this document. A solution to this issue is for a NOS to accept either value, "0x11 QSFP28" or "0x0D QSFP+ or Later".

Test 6.2 - Link Detection on Power Up

Purpose: To determine if the MUT/CUT, HUT and LP establish a link while varying the power up sequence.

Resource Requirements:

- Link monitoring and traffic generating capabilities.
- Local management indicators on the HUT and LP that indicate the state of the link.
- Known good optical fiber cable with appropriate connector assembly

Discussion: The ability to detect and establish a link is dependent on the two devices that make up the link segment and the channel used to connect the two devices. This test procedure addresses several conditions in which link detection should work when a Module or Cable Assembly is used in a Host device. There are three parts to this test.

1. The Host is fully powered up, has its drivers loaded, and then receives the Module or Cable Assembly with and without a link partner connected to the Module or Cable Assembly during insertion.
2. The Host is powered on with the Module or Cable Assembly inserted and connected to a link partner that has not yet powered on.
3. The Host is powered on with the Module or Cable Assembly inserted and connected to a link partner that has already been powered on.

These three conditions are checked, as there may be different signals on the line during the boot up sequences of the hosts, such as remote and local fault, that could cause the system to improperly not establish a link.

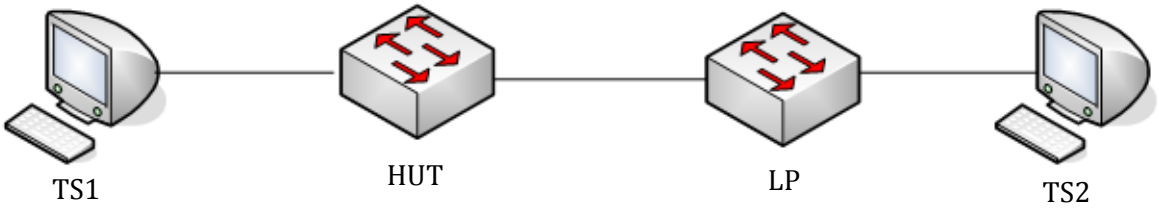
The act of verifying the link is not necessarily obvious, and difficulties arise in determining the cause of the link not being active, if problems exist. Indications such as link lights and status indicators, while they can provide very useful and visible information, may not always represent the status of the link. In addition, frames should be able to be passed from one device to the other once the link has been established.

This test is an interoperability test. Failure of this test does not mean that the Module, Cable Assembly or Host is non-conformant. It does suggest that a problem in the ability of two devices to work "properly" together exists and further work should be done to isolate the cause of the failure.

If the link under test is implementing a 100GBASE-SR4 phy, the test herein should be performed with FEC enabled per IEEE 802.3bj Clause 92.

If the link under test is implementing a 25GBASE-CR phy, the test herein should be performed with FEC enabled per IEEE 802.3by Clause 110.

Test Setup: The frames transmitted in these tests are defined in Appendix C. The Default Test Setup for the HUT and LP is defined in Appendix D. The following diagram describes the test layout. The MUT/CUT is used for all connections.



Test Procedure:

Part A. The HUT receives the MUT/CUT while fully powered and operational.
In Part A, Steps 4, 8, 10-12, 16-20 are only applicable Modules.

1. Power off the HUT and LP.
2. Ensure that the Test Setup is configured.
3. Remove the MUT/CUT from the HUT
4. Disconnect the cable connecting to the MUT in the LP.
5. Power on the HUT and LP.
6. Ensure that the devices are fully up and all needed drivers are loaded.
7. Insert the MUT/CUT back into the HUT
8. Reconnect the cable to the MUT in the LP.
9. From TS1, transmit Traffic Stream 6.2 at baseline established in Test 6.1 in order to verify that the link was properly established.
10. Remove the cable from the MUT in the HUT for a few seconds, then reinsert.
11. From TS1, transmit Traffic Stream 6.2 at baseline established in Test 6.1 in order to verify that the link was properly established.
12. Remove the cable from the MUT in the HUT
13. Remove the MUT/CUT from the HUT
14. Reinsert the MUT/CUT in the HUT and then reconnect the cable (if MUT is being tested).
15. From TS1, transmit Traffic Stream 6.2 at baseline established in Test 6.1 in order to verify that the link was properly established.
16. Remove the cable from the MUT in the HUT
17. Remove the MUT from the HUT
18. Reconnect the cable to the MUT.
19. Reinsert the MUT in the HUT.
20. From TS1, transmit Traffic Stream 6.2 at baseline established in Test 6.1 in order to verify that the link was properly established.

Part B. The MUT/CUT receives no input signal during power up.

1. Power off the HUT and LP.
2. Ensure that the Test Setup is configured.
3. Power on the HUT
4. Ensure that the device is fully up and all needed drivers are loaded.
5. Power on the LP
6. Ensure that the device is fully up and all needed drivers are loaded.

7. From TS1, transmit Traffic Stream 6.2 at baseline established in Test 6.1 in order to verify that the link was properly established.

Part C. The MUT/CUT receives signal from the LP during power up.

1. Power off the HUT and LP.
2. Ensure that the Test Setup is configured.
3. Power on the LP
4. Ensure that the device is fully up and all needed drivers are loaded.
5. Power on the HUT
6. Ensure that the device is fully up and all needed drivers are loaded.
7. From TS1, transmit Traffic Stream 6.2 at baseline established in Test 6.1 in order to verify that the link was properly established.
8. Reboot the HUT and LP

Observable results: The HUT and LP must be examined for indicators of a proper link. This is typically an LED that lights when link is established. Local management may provide information about configuration and status, as well. The passing of valid frames between the two devices should serve as final validation that the link has been established. The testing stations will exchange packets with each other. The links between the testing stations and the Host must be error free.

Part A:

- In steps 9, 11, 15, and 19, the HUT and LP should establish a valid link each time the MUT/CUT reconnects both devices.
- In steps 9, 11, 15, and 19, TS2 must receive all of the frames transmitted by TS1.

Part B:

- In step 7, the HUT and LP should establish a valid link when both devices are fully operational.
- In step 7, TS2 must receive all of the frames transmitted by TS1.

Part C:

- In step 7, the HUT and LP should establish a valid link when both devices are fully operational.
- In step 7, TS2 must receive all of the frames transmitted by TS1.

Possible Problems: Some Modules or Cable Assemblies may require power that is not supplied by the Host; these combinations will not be tested.

Due to known issues with some types of test equipment and Direct Attached Copper cables, it may be desirable to use a 'golden module' to attach the HUT to the Testing Station, however a golden module should not be used for this test. If a golden module is used for this test it would eliminate the use of the pluggable module / Cable under test and invalidate the results of testing the Pluggable Module/ Cable/ NOS/ OCP Switch combination. If problems are encountered that appear to be due to incompatibilities between the Testing Station and DAC, a different type of Testing Station should be used, such as another test equipment manufacturer, or a Server with NIC and traffic generation software.

If the link under test is implementing a 100GBASE-SR phy, the test herein should be performed with FEC enabled per IEEE 802.3bm Clause 91.

If the link under test is implementing a 25GBASE-CR phy, the test herein should be performed with FEC enabled per IEEE 802.3by Clause 110.

If the link under test is implementing a 100GBASE-CR phy breakout to 25GBASE-CR phy, the test herein should be performed with FEC disabled.

Test 6.3 - Packet Error Rate Estimation

Purpose: To determine if a Host can exchange packets with a Module or Cable Assembly such that a bit error rate of 10^{-12} is achieved

Resource Requirements:

- Link monitoring and traffic generating capabilities.
- Local management indicators on the HUT and LP that indicate the state of the link.
- Known good optical fiber cable with appropriate connector assembly

Discussion: This test is designed to verify the ability of a Host to exchange packets with a Module or Cable Assembly. The exchange of packets must produce a packet error rate that is low enough to meet a desired bit error rate. The bit error rate as specified in the IEEE Std 802.3ae-2012 is 10^{-12}. The number of frames to be sent depends on the Module or Cable Assembly type that is used by the Host.

Approximately $2.47*10^{8}$ 1518-byte frames need to be transmitted without error, to ensure that the bit error rate is less than 10^{-12} with 95% confidence. This applies to all Module and Cable Assemblies types.

If more than 7 packets are lost during the exchange, then the BER criteria has not been met and the test fails. In addition to packets lost, local management information may make it possible to isolate the packet loss to either the transmit side or the receive side of the test channel relative to the Host and Module/Cable Assembly. If more than 7 packets are lost in either side of the channel, then the Host and Module/Cable Assembly combination has violated the BER and the result is considered a failure.

The observable results in this testing process are one or more packet counters. Since a single packet contains many bits, the measurement technique does not really measure the bit error rate. The PASS/FAIL criteria assume that no more than one bit is in error in a lost packet. Thus a device may in theory pass a test with a bit error in excess of 1 in 10^{12}.

However, given that any one bit in error will corrupt the packet, multiple errors within a packet do not, in practice, make a difference in the number of packets that must be retransmitted on real links. Thus, a short-term clock deviation that causes a bit error rate of 5 bits in a stream of 10^{12} bits will, under most conditions, cause as many packet errors as a device with a bit error rate of 1 in 10^{12}.

The results obtained from this testing process should not be seen as a true measure of the bit error rate but as information that may suggest the need for further analysis.

Under some circumstances, additional fiber lengths may be made available for testing.

Test Setup: The frames transmitted in these tests are defined in Appendix C. The Default Test Setup for the HUT is defined in Appendix D. Physical Test Setup is defined in Appendix B. The MUT/CUT is used for all connections. If an LR4 or LR4 Lite tranciver is the MUT, the variable attenuator shown in the test setup should be configured to add no more than 2.5 dB of loss for LR4 Lite configurations and no more than 5.5 dB of loss for LR4 configurations.

Test Procedure

Part A. BER

1. Ensure that the Test Setup is configured.
2. Reset all counters that will be used to measure or monitor the exchange of packets
3. From TS1, transmit Traffic Stream 6.3 A at baseline established in Test 6.1.
4. Using the available counters, identify the number of packets received and transmitted.

Part B: Longevity

1. Ensure that the Test Setup is configured.
2. Reset all counters that will be used to measure or monitor the exchange of packets
3. Transmit Traffic Stream 6.3 B at baseline established in Test 6.1 for one hour.
4. Using the available counters, identify the number of packets received and transmitted.
5. Reboot the HUT.

Note: These tests can be repeated with various data patterns in the frames transmitted to create various transmitter stress situations.

Observable Results

Part A:

- In step 4, verify that no more than 6 received frames have errors or were dropped.

Part B:

- In step 4, verify that a BER of no greater than 10^{-12} was maintained over the duration of the test.

Possible Problems: Due to known issues with some types of test equipment and Direct Attached Copper cables, it may be desirable to use a 'golden module' to attach the HUT to the Testing Station, however a golden module should not be used for this test. If a golden module is used for this test it would eliminate the use of the pluggable module / Cable under test and invalidate the results of testing the Pluggable Module/ Cable/ NOS/ OCP Switch combination. If problems are encountered that appear to be due to incompatibilities between the Testing Station and DAC, a different type of Testing Station should be used, such as another test equipment manufacturer, or a Server with NIC and traffic generation software.

If the link under test is implementing a 100GBASE-SR4 phy, the test herein should be performed with FEC enabled per IEEE 802.3bm Clause 91.

If the link under test is implementing a 25GBASE-CR phy, the test herein should be performed with FEC enabled per IEEE 802.3by Clause 110.

If the link under test is implementing a 100GBASE-CR phy breakout to 25GBASE-CR phy, the test herein should be performed with FEC disabled.

Test 6.4 - Packet Loss/Stress Test

Purpose: To verify that no obvious buffer management problems occur when directing a large volume of traffic at the Host and Module/Cable Assembly combination.

Resource Requirements:

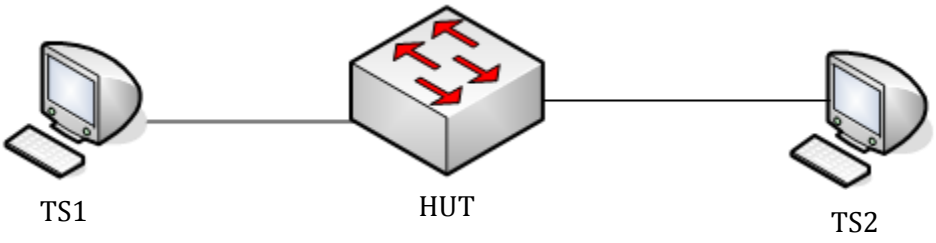
- Link monitoring and traffic generating capabilities on TS1 and TS2.
- Local management indicators on the HUT and LP that indicate the state of the link.
- Known good optical fiber cable with appropriate connector assembly

Discussion: This test is designed to verify that the Host and Module/Cable Assembly combination has no obvious buffer management problems. The Host and Module/Cable Assembly combination does not have to respond to or forward all of the frames, but the test should not cause any system failures. Two sets of frame sizes are used for this test. For the first test run, 64-byte frames are used, since they are the smallest frames and therefore require the most overhead processing in the system. The second set of frames are 1518 bytes in length.

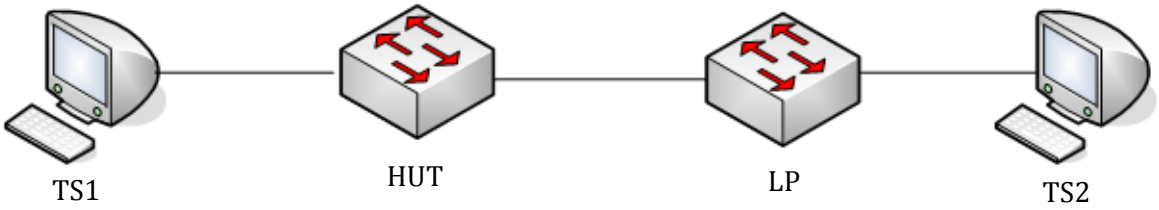
Test Setup: Further description for Parts C and D is provided in Appendix B, which describes a daisy-chain setup. The frames transmitted in these tests are defined in Appendix C. The Default Test Setup for the HUT and LP is defined in Appendix D. The MUT/CUT is used for all connections.

TS1 and TS2 may be either a dedicated traffic analyzer and generator system, or a given combination of OCP or non-OCP Server, OCP or non-OCP NIC, and OS.

Part A: The following diagram describes the test layout.



Part B: The following diagram describes the test layout.



Parts C and D: See Appendix B.

Test Procedure:

Part A. Stress Test - No LP

1. Ensure that the Test Setup is configured.
2. Reset all counters that will be used to measure or monitor the exchange of packets.
3. Transmit Traffic Stream1 6.4 at baseline established in Test 6.1.
4. Observe all management and status indicators of the Host Under Test
5. Transmit Traffic Stream2 6.4 at baseline established in Test 6.1.
6. Observe all management and status indicators of the Host Under Test

Part B. Stress Test – With LP

1. Ensure that the Test Setup is configured.
2. Reset all counters that will be used to measure or monitor the exchange of packets.
3. Transmit Traffic Stream1 6.4 at baseline established in Test 6.1.
4. Observe all management and status indicators of the Host Under Test
5. Transmit Traffic Stream2 6.4 at baseline established in Test 6.1.
6. Observe all management and status indicators of the Host Under Test

Part C. Stress Test - Fully Loaded Chassis - No LP

1. Ensure that the Test Setup is configured (see appendix B).
2. Reset all counters that will be used to measure or monitor the exchange of packets.
3. Transmit Traffic Stream1 6.4 at baseline established in Test 6.1.
4. Observe all management and status indicators of the Host Under Test
5. Transmit Traffic Stream2 6.4 at baseline established in Test 6.1.
6. Observe all management and status indicators of the Host Under Test

Part D. Stress Test - Fully Loaded Chassis – With LP

1. Ensure that the Test Setup is configured (see appendix B).
2. Reset all counters that will be used to measure or monitor the exchange of packets.
3. Transmit Traffic Stream1 6.4 at baseline established in Test 6.1.
4. Observe all management and status indicators of the Host Under Test
5. Transmit Traffic Stream2 6.4 at baseline established in Test 6.1.
6. Observe all management and status indicators of the Host Under Test

Observable results:

Part A:

- In steps 4 and 6, the HUT should not have power cycled and should be able to maintain 95% line rate performance without dropping packets.

Part B:

- In steps 4 and 6, the HUT should not have power cycled and should be able to maintain 95% line rate performance without dropping packets.

Part C:

- In steps 4 and 6, the HUT should not have power cycled and should be able to maintain 95% line rate performance without dropping packets.

Part D:

- In steps 4 and 6, the HUT should not have power cycled and should be able to maintain 95% line rate performance without dropping packets.

Possible Problems: In some NOS/switch combinations it may be necessary to send 'warm up' traffic from the Testing Station prior to starting the test in order to allow the NOS to properly populate the Filtering Database. This is acceptable.

Due to known issues with some types of test equipment and Direct Attached Copper cables, it may be necessary to use a 'golden module' to attach the HUT to the Testing Station. The golden module can be any cable or pluggable module that was previously tested successfully with the HUT and Testing Station. Oftentimes the golden module used when testing a combination using DACs, may be an AOC or optical module that is known to work with the Testing Station.

Although a BER may be determined from test results, only a Pass/Fail indication will be provided in the test results.

If the link under test is implementing a 100GBASE-SR4 phy, the test herein should be performed with FEC enabled per IEEE 802.3bm Clause 91.

If the link under test is implementing a 25GBASE-CR phy, the test herein should be performed with FEC enabled per IEEE 802.3by Clause 110.

If the link under test is implementing a 100GBASE-CR phy breakout to 25GBASE-CR phy, the test herein should be performed with FEC disabled.

If the link under test include a 1x4 breakout cable, test 6.4 C may not be applicable.

If the link under test include a 1x4 breakout cable, it may not be possible to connect every port when peformed test 6.4 D. The test should be performed with as many ports connected as possible given the layout of the switch.

Appendix A: Module Validation Criteria

SFP+ Module Validation Criteria:
Statement from vendor that product is designed to meet the specifications below:

MSA governing specifications:

SFF-8431 – Specification for SFP+ with addendum revision 4.1
SFF-8432 – Specification for Improved Pluggable Form Factor
SFF-8472 – Rev 11.3 or later Diagnostic Monitoring Interface for Optical Transceivers (for SFP+ EEPROM)

Management Interface:

Serial ID EEPROM
Digital Optical Monitoring (DOM) compliance to SFF-8472, where applicable
Low speed signaling requirements

Optical or Copper Performance:

IEEE Spec compliance to 802.3 (as appropriate)

Environmental:

Data Center Environment or
Standard Environment
RoHS-6 compliant
Class 1 Eye Safety per IEC-60825-1

Reliability:

GR-468 criteria

QSFP+ Module Validation Criteria:
Statement from vendor that product is designed to meet the specifications below:

MSA governing specifications:

SFF-8436 - Rev. 4.8 or later (Primary MSA, now transferred to EIA-964)
SFF-8636 – Rev. 1.7 or later (for QSFP+ EEPROM)
SFF-8635 - Rev. 0.5 or later (Mechanical: Must comply with SFF-8436)
SFF-8679 - Rev. 1.5 or later (Electrical and Optical Interfaces)

Management Interface:

Serial ID EEPROM
Digital Optical Monitoring (DOM) compliance to SFF-8472, where applicable
Low speed signaling requirements
Optical Performance or Copper
IEEE Spec compliance

Environmental:

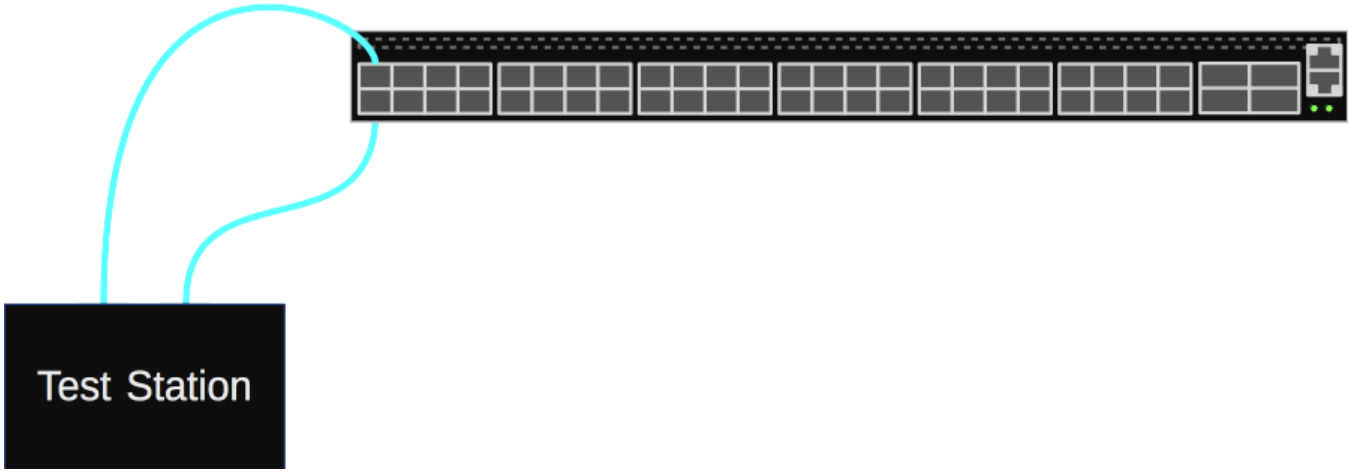
Data Center Environment or
Standard Environment
RoHS-6 compliant
Class 1 Eye Safety per IEC-60825-1

Reliability:

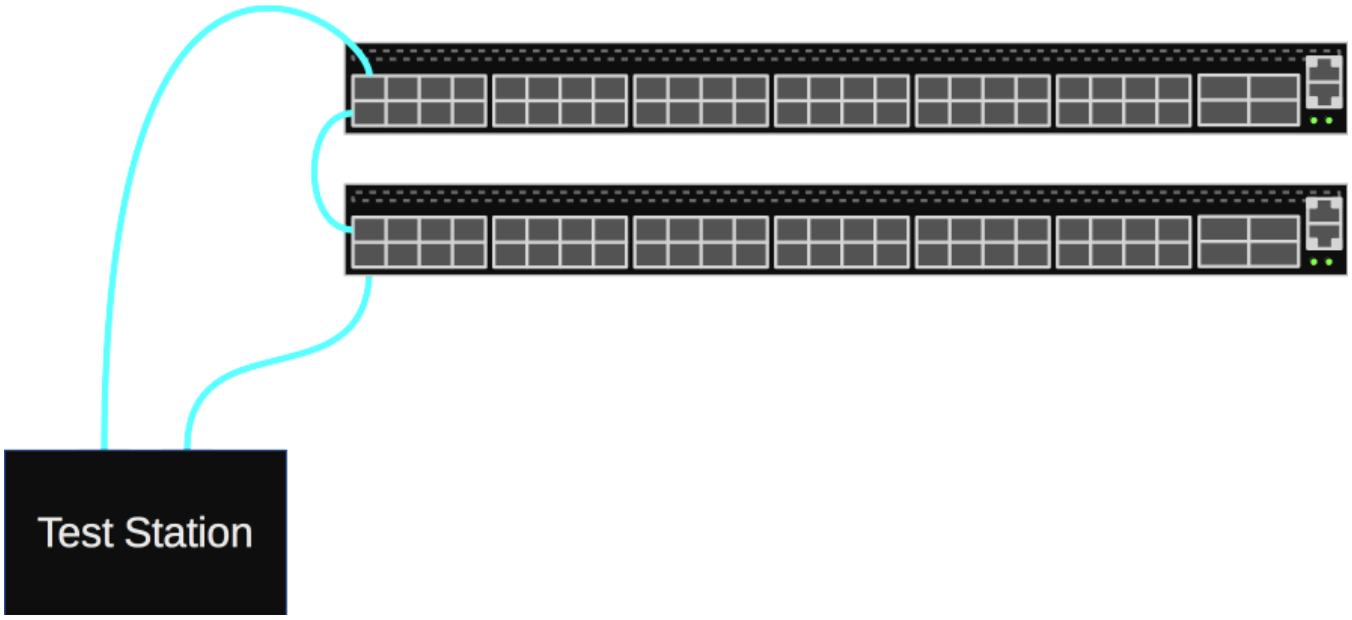
GR-468 criteria

Appendix B: Physical Test Setups

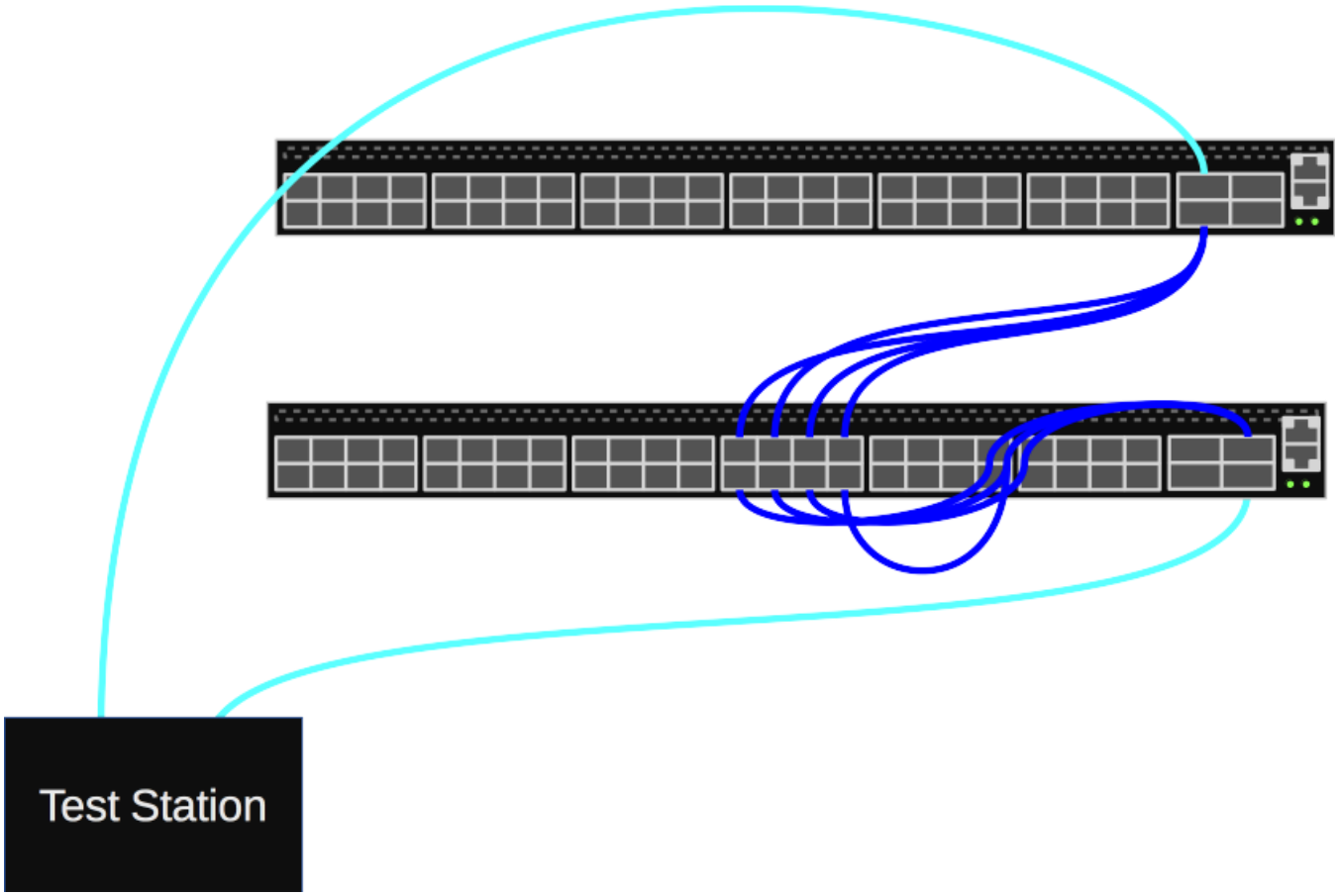
Test 6.1



Test 6.2 and 6.3

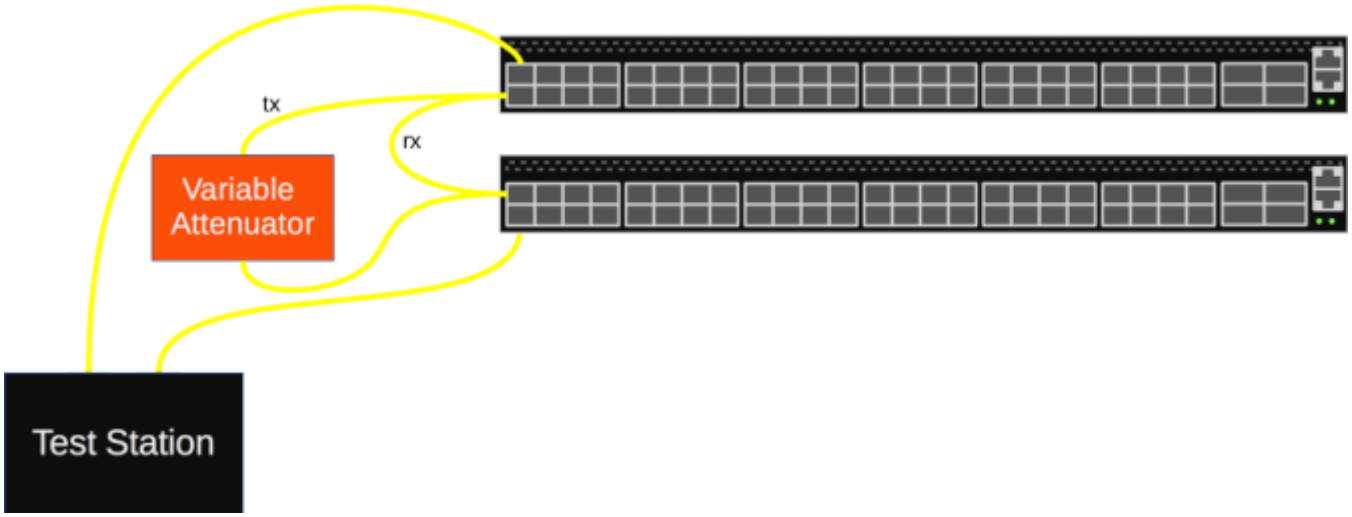


Test 6.2 and 6.3 Using 1x4 Breakout Cables

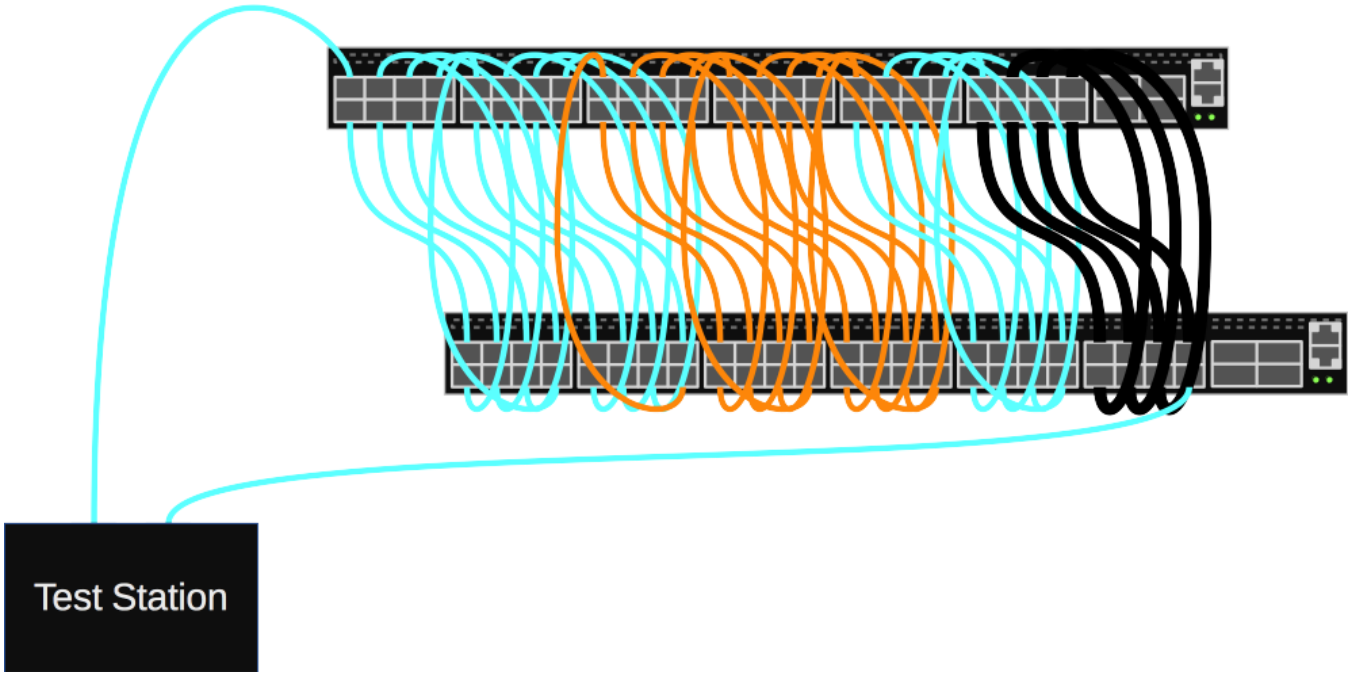


Certain switches may need to be configured to operate in a 'break-out' mode, to be used with a breakout cable. This is acceptable for the purposes of this test.

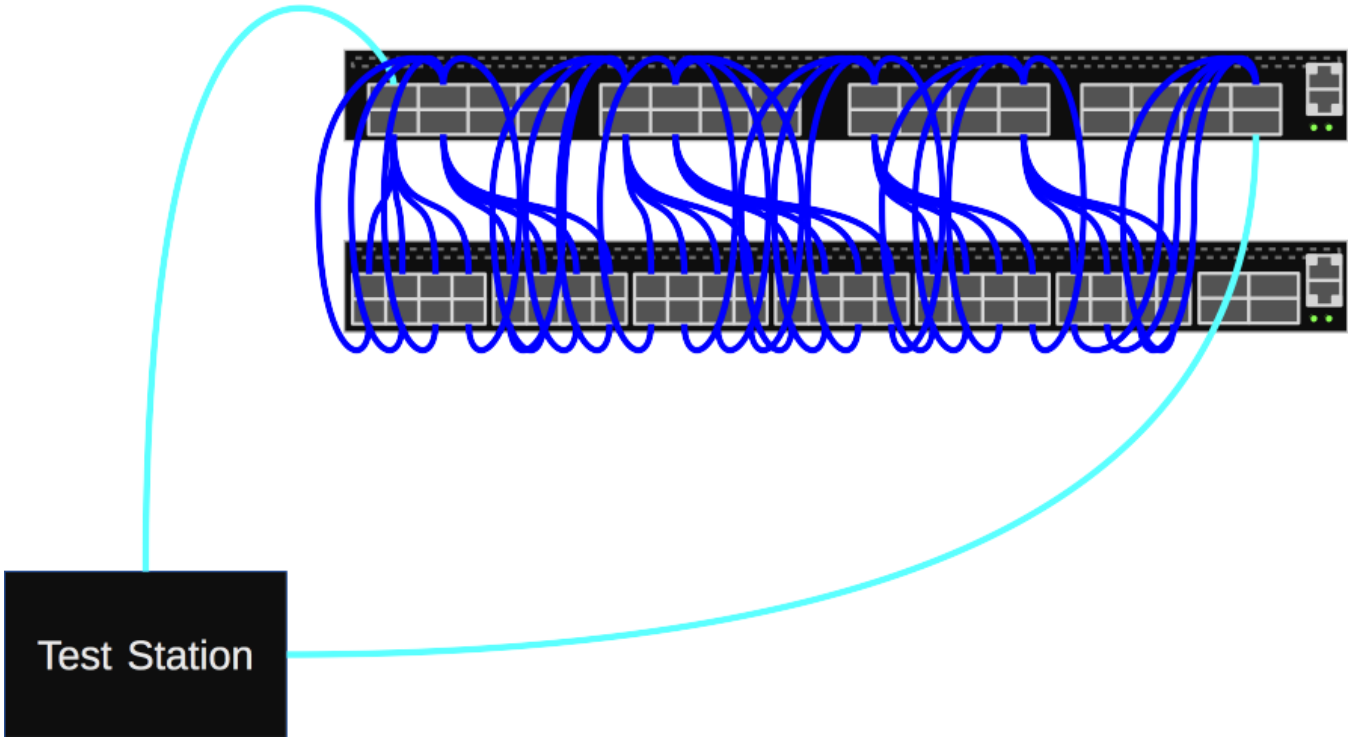
Test 6.3B Using LR4 or LR4 Lite Trancievers



Test 6.4 - Fully loaded Host Under Test



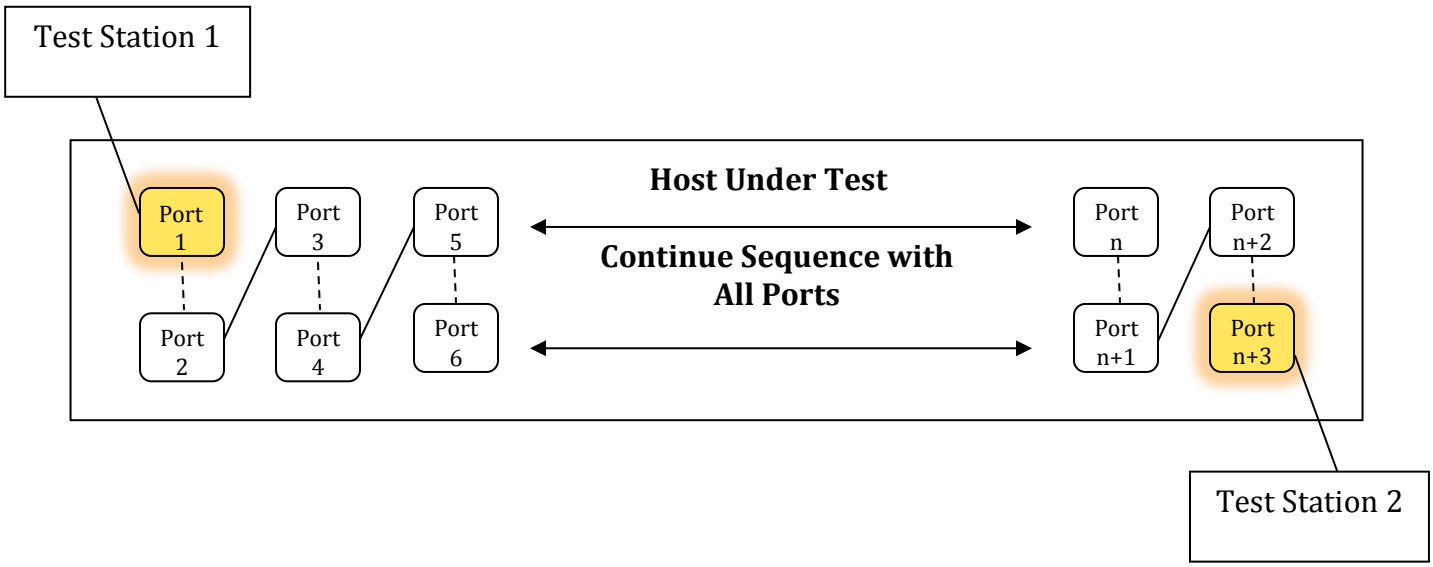
Test 6.4 - Fully loaded Host Under Test using 1x4 Breakout Cables



Certain switch products may have a maximum number of SERDES that can be supported, which is less than the total number of SERDES necessary to use the switch with every port connected to a breakout cable. If this is the case, its necessary to note the maximum number of SERDES supported by the switch, and use an interop configuration that only uses the SERDES supported by the switch.

Certain switches may need to be configured to operate in a 'break-out' mode, to be used with a breakout cable. This is acceptable for the purposes of this test.

The following diagram describes the test layout for daisy chaining a chassis with two test stations connected to the HUT. If a chassis supports multiple module/cable assembly types (i.e. SFP+ and QSFP+), all ports of all types should be populated. While preferred, it is not necessary to populate all ports with the same module or cable assembly type.



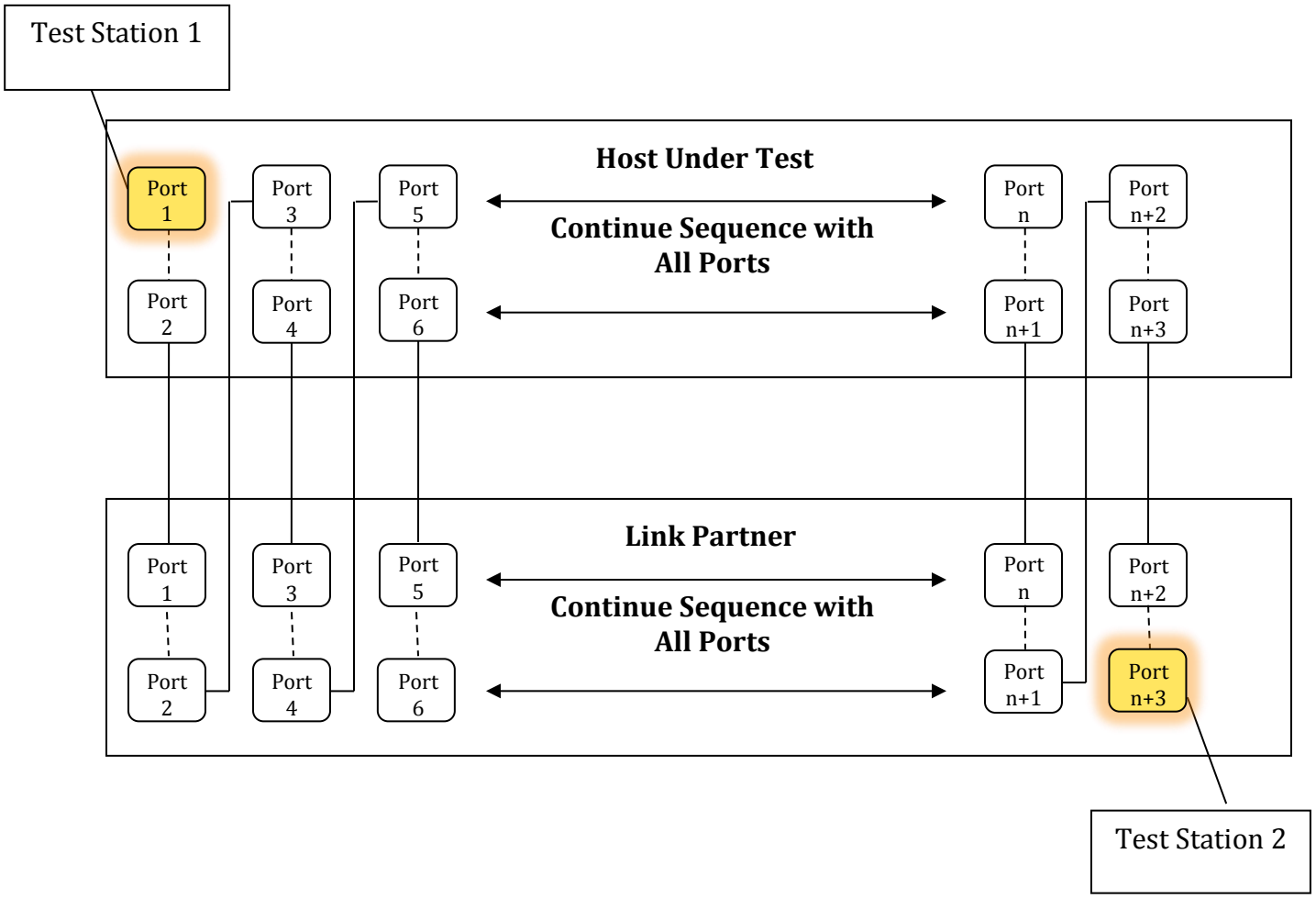
——— Physical Connection via compliant cable
------ Virtual Connection via VLAN

The test uses the following setup for the Host Under Test:

- Disable Spanning Tree Protocol
- Set Acceptable frame type parameter to admit all frames on all ports
- Set Ingress Filtering to reset (disabled) on all ports
- Configure Port 1 on the HUT to have PVID 1
- Configure Port 2 on the HUT to be an untagged member of Vlan 1
- Configure Port 3 on the HUT to have PVID 2
- Configure Port 4 on the HUT to be an untagged member of Vlan 2
- Continue this sequence until every port on the HUT is configured
- Connect TS1 to port 1 on the HUT for transmittal of frames
- Connect TS2 to the last port on the HUT for transmittal of frames

Fully loaded Host Under Test Connected to Link Partner

The following diagram describes the test layout for daisy chaining two chassis with one test stations connected to the Host Under Test and another test station connected to the Link Partner.



Physical Connection via compliant cable
Virtual Connection via VLAN

The test uses the setup previously described above for the HUT and the LP. The only difference being: Connect TS2 to the last port on the ***LP*** for transmittal of frames.

Appendix C: Traffic Streams

Test Traffic Format

The following frames will be used throughout this test suite. The fixed pattern to be used in all frames is simply *BFC* repeated.

Traffic Stream 6.1 A: 64-byte frames with a fixed data pattern
TS1: 10 frames
SA: 00 00 61 00 11 11
DA: 00 00 61 00 22 22

Traffic Stream 6.1 B: 64-byte frames with a fixed data pattern

TS1: 1 billion frames	TS2: 1 frame per 10 seconds
SA: 00 00 61 00 11 11	SA: 00 00 61 00 22 22
DA: 00 00 61 00 22 22	DA: 00 00 61 00 11 11

Traffic Stream 6.2: 64-byte frames with a fixed data pattern
TS1: 10 frames
SA: 00 00 62 00 11 11
DA: 00 00 62 00 22 22

Traffic Stream 6.3 A: 1518-byte frames with a fixed data pattern

TS1: 247 million frames	TS2: 1 frame per 10 seconds
SA: 00 00 63 00 11 11	SA: 00 00 63 00 22 22
DA: 00 00 63 00 22 22	DA: 00 00 63 00 11 11

Traffic Stream 6.3 B: 1518-byte frames with a fixed data pattern,

TS1: Continuous Stream	TS2: 1 frame per 10 seconds
SA: 00 00 63 00 11 11	SA: 00 00 63 00 22 22
DA: 00 00 63 00 22 22	DA: 00 00 63 00 11 11

Traffic Stream1 6.4: 64-byte frames with a fixed data pattern

TS1: 1 billion frames	TS2: 1 frame per 10 seconds
SA: 00 00 64 00 11 11	SA: 00 00 64 00 22 22
DA: 00 00 64 00 22 22	DA: 00 00 64 00 11 11

Traffic Stream2 6.4: 1518-byte frames with a fixed data pattern,

TS1: 1 billion frames	TS2: 1 frame per 10 seconds
SA: 00 00 64 00 11 11	SA: 00 00 64 00 22 22
DA: 00 00 64 00 22 22	DA: 00 00 64 00 11 11

Appendix D: Default Test Setup

Unless otherwise specified, all tests will use the following default values:

Port Admin Status	Enabled (all ports)
Acceptable Frame Type Parameter	Admit-all-Frames
LLDP	Disabled
MAC Ageing Time	300 seconds
Bridge Spanning Tree Admin Status	Disabled
PVID	1 (all ports)
VLAN Membership	1 – untagged (all ports)
Ingress Filtering	Reset (i.e. Disable Ingress Filtering)
Host Under Test's Filtering Database	No entries

Appendix E: Test Equipment

- Agilent J-BERT N4903A High Performance Serial BERT
- Agilent DCA-X86100D Wide Bandwidth Oscilloscope
- Agilent DCA-86108B 50 GHz Precision Waveform analyzer
- Anritsu P1800A Signal Quality Analyzer with MU181020B 14Gb/s PPG (x2)
- Agilent N4916B De-Emphasis Signal Converter
- Agilent E5071C 20GHz Network Analyzer

Appendix F: SFP+ and QSFP+ Values

* SFP+ (I2C address A2h, Byte 0 - 55) detailed listing of alarm and warning thresholds:

Temperature High Alarm Threshold (Byte 0, 1)
Temperature Low Alarm Threshold (Byte 2, 3)
Temperature High Warning Threshold (Byte 4, 5)
Temperature Low Warning Threshold (Byte 6, 7)
Supply Voltage High Alarm Threshold (Byte 8, 9)
Supply Voltage Low Alarm Threshold (Byte 10, 11)
Supply Voltage High Warning Threshold (Byte 12, 13)
Supply Voltage Low Warning Threshold (Byte 14, 15)
TX bias High Alarm Threshold (Byte 16, 17)
TX bias Low Alarm Threshold (Byte 18, 19)
TX bias High Warning Threshold (Byte 20, 21)
TX bias Low Warning Threshold (Byte 22, 23)
TX power High Alarm Threshold (Byte 24, 25)
TX power Low Alarm Threshold (Byte 26, 27)
TX power High Warning Threshold (Byte 28, 29)
TX power Low Warning Threshold (Byte 30, 31)
RX power High Alarm Threshold (Byte 32, 33)
RX power Low Alarm Threshold (Byte 34, 35)
RX power High Warning Threshold (Byte 36, 37)
RX power Low Warning Threshold (Byte 38, 39)
Reserved (Byte 40 – 55)

* SFP+ (I2C address A2h, Byte 96 - 109) detailed listing of monitoring values:
Temperature (Byte 96, 97)
Supply Voltage (Byte 98, 99)
TX bias channel 1 (Byte 100, 101)
TX output power (Byte 102, 103)
RX input power (Byte 104, 105)
Reserved (Byte 106 – 109)

* QSFP+ (I2C address A0h, Page 3 Byte 128 – 223) detailed listing of alarm and warning thresholds:
Temperature High Alarm Threshold (Byte 128, 129)
Temperature Low Alarm Threshold (Byte 130, 131)
Temperature High Warning Threshold (Byte 132, 133)
Temperature Low Warning Threshold (Byte 134, 135)
Reserved (Byte 136 – 143)
Supply Voltage High Alarm Threshold (Byte 144, 145)
Supply Voltage Low Alarm Threshold (Byte 146, 147)
Supply Voltage High Warning Threshold (Byte 148, 149)
Supply Voltage Low Warning Threshold (Byte 150, 151)

Reserved (Byte 152 – 159)
Vendor Specific (Byte 160 – 175)
RX power High Alarm Threshold (Byte 176, 177)
RX power Low Alarm Threshold (Byte 178, 179)
RX power High Warning Threshold (Byte 180, 181)
RX power Low Warning Threshold (Byte 182, 183)
TX bias High Alarm Threshold (Byte 184, 185)
TX bias Low Alarm Threshold (Byte 186, 187)
TX bias High Warning Threshold (Byte 188, 189)
TX bias Low Warning Threshold (Byte 190, 191)
TX power High Alarm Threshold (Byte 192, 193) [comment: defined in SFF-8638 only]
TX power Low Alarm Threshold (Byte 194, 195) [comment: defined in SFF-8638 only]
TX power High Warning Threshold (Byte 196, 197) [comment: defined in SFF-8638 only]
TX power Low Warning Threshold (Byte 198, 199) [comment: defined in SFF-8638 only]
Reserved thresholds for channel parameter set 4 (Byte 200 – 207)
Vendor Specific (Byte 208 – 223)

* QSFP+ (I2C address A0h, Page 0 Byte 22 – 81) detailed listing of monitoring values:
Temperature (Byte 22, 23)
Reserved (Byte 24, 25)
Supply Voltage (Byte 26, 27)
Reserved (Byte 28, 29)
Vendor Specific (Byte 30 - 33)
RX input power channel 1 (Byte 34, 35)
RX input power channel 2 (Byte 36, 37)
RX input power channel 3 (Byte 38, 39)
RX input power channel 4 (Byte 40, 41)
TX bias channel 1 (Byte 42, 43)
TX bias channel 2 (Byte 44, 45)
TX bias channel 3 (Byte 46, 47)
TX bias channel 4 (Byte 48, 49)
TX output power channel 1 (Byte 50, 51) [comment: defined in SFF-8638 only]
TX output power channel 2 (Byte 52, 53) [comment: defined in SFF-8638 only]
TX output power channel 3 (Byte 54, 55) [comment: defined in SFF-8638 only]
TX output power channel 4 (Byte 56, 57) [comment: defined in SFF-8638 only]
Reserved channel monitor set 4 (Byte 58 - 65)
Vendor Specific (Byte 66 - 81)

Appendix G: Debug Information

The following outlines best practices for collecting information on failures uncovered when executing this test plan in order to aid in debugging.

1. Which test was being executed?
2. What version of the Open Network Systems Interoperability Test Plan was being performed?
3. Were there any deviations from the prescribed process?
4. Describe the failure: i.e. Bit errors; packet loss; CRC errors; link flap; link down; etc.
5. What are the specific indications of failure?
   - 5.1. Was the failure detected at A or B?
   - 5.2. Any indication if it is Tx or Rx failure?
   - 5.3. What were the specific steps to try to correct failure?
     - 5.3.1. How many times was the test attempted
     - 5.3.2. Was the result the same for each test execution?
     - 5.3.3. Was it an immediate result?
     - 5.3.4. Were other identical modules from same vendor tried (if a module test)?
     - 5.3.5. Were similar parts from another vendor tried? Did they work? In slots A or B or required both to be changed?

6. Link partner A:
   - 6.1. Host System Vendor
   - 6.2. Host Model number
   - 6.3. Version information for the Host
   - 6.4. CPLD Version
   - 6.5. Serial number of host
   - 6.6. Was a configuration command or script used to configure?
   - 6.7. If yes, what is name and version number of configuration script?
   - 6.8. What NOS was loaded?
   - 6.9. Version of NOS?
   - 6.10. Any special configuration commands or scripts run within NOS to get test to run? Version of those scripts or command sequences.
   - 6.11. Slot # for link partner A
   - 6.12. Any special configuration condition for slot?
   - 6.13. Pluggable device vendor
   - 6.14. Pluggable device part number
   - 6.15. Pluggable device serial number

7. Link partner B:
   - 7.1. Host System Vendor
   - 7.2. Host Model number
   - 7.3. Version information for the Host
   - 7.4. CPLD Version
   - 7.5. Serial number of host
   - 7.6. Was a configuration command or script used to configure?
   - 7.7. If yes, what is name and version number of configuration script?
   - 7.8. What NOS was loaded?
   - 7.9. Version of NOS?

7.10. Any special configuration commands or scripts run within NOS to get test to run? Version of those scripts or command sequences.
7.11. Slot # for link partner A
7.12. Any special configuration condition for slot?
7.13. Pluggable device vendor
7.14. Pluggable device part number
7.15. Pluggable device serial number

8. From Pluggable device A
   8.1. Capture EEPROM dump after failure but before any changes are made with resets, re-plugging pluggable
   8.2. Capture status of pluggable device flags before any changes are made with resets, re-plugging pluggable
   8.3. Capture the DOM values of Tx optical power, Rx optical power, LDI (laser current), Module temperature

9. From Pluggable device B
   9.1. Capture EEPROM dump after failure but before any changes are made with resets, re-plugging pluggable
   9.2. Capture status of pluggable device flags before any changes are made with resets, re-plugging pluggable
   9.3. Capture the DOM values of Tx optical power, Rx optical power, LDI (laser current), Module temperature

10. Measure the optical power entering the Rx of link partner B (i.e. at the exit of the fiber connection to verify the integrity of the fiber)
11. Measure the optical power entering the Rx of link partner A (i.e. at the exit of the fiber connection to verify the integrity of the fiber)

12. Capture the optical eye leaving the fiber connected to Rx link partner B (requires optical input of oscilloscope with CDR function).
13. Capture the optical eye leaving the fiber connected to Rx link partner A (requires optical input of oscilloscope with CDR function).

Appendix H: Module/Cable Assembly Sample Quantity Requirements

This appendix will help the test technician to determine the necessary quantity of samples of a given module or cable assembly that is necessary to perform a given test. Some tests described in this document require the switch under test to be completely populated with modules or cable assemblies, in order to simulate a real-world fully loaded use case. Although the ideal circumstance is populate the switch uniformly with one type of module or cable assembly, this is not always practical due to the difficulty and expense of obtaining enough modules or cable assemblies. Therefore it is acceptable to use combinations of different modules and cable assemblies in order to fully populate the switch ports.

The ***preferred*** number of module/cable assembly samples will enable the technician to populate 100% of the maximum allowable ports per the switch manufacturer specifications. The ***minimum*** number of samples will enable the technician to populate 50% of the maximum allowable ports per the switch manufacturer specifications.

Its recommend that companies testing DAC cables provide cables of 3m in length. Companies may provide other lengths if they prefer.

The quantities provided in the table below are based on common switch port counts at the time of writing. The percentages provided in the above paragraph can help the test technician to scale the quantity of samples necessary if a higher port count switch is being tested.

Module / Cable Type	Minimum # of Samples Needed per SKU	Preferred # of Samples per SKU
10G SFP+ SR AOC Cables	12	24
10G SFP+ DAC Cables	12	24
10G SFP+ SR Optical Modules	24	48
10G SFP+ x4 to 40G QSFP+ 'Breakout' DAC	12	24
10G SFP+ LR Optical Modules	24	48
25G SFP28 AOC Cables	12	24
25G SFP28 DAC Cables	12	24
25G SFP28 x4 to 100G QSFP28 'Breakout' DAC	12	24
40G QSFP+ SR AOC Cables	18	36
40G QSFP+ DAC Cables	18	36
40G QSFP+ SR optical modules	18	36
40G QSFP+ LR optical modules	18	36
100G QSFP28 AOC Cables	8	16
100G QSFP28 DAC Cables	8	16
100G QSFP28 SR Optical Modules	16	32

Appendix I: Test Optimization Rules

As more and more combinations of pluggable module/cable, NOS, and Open Networking switches are tested together confidence is increased not only in the tested combinations, but also in the components that make up those combinations. As such, it may not be necessary to perform all of the tests described in this document in order to establish confidence in a particular product combination, especially if that test only tests a single component, or a combination of components that were previously tested together.

To eliminate duplicated effort and to reduce test time, the following rules are provided to help the test engineer choose which tests are most relevant to the combination under test:

- If a given combination of host/pluggable have already been tested together successfully with a given NOS, and now are being tested with a different or updated NOS, it is not necessary to perform Group 1, 2, 3, 4 again. It is only necessary to test Group 5 and 6.
- If a host has been tested with a hardware based traffic generator at or near 100% line rate with one configuration, it is not necessary to perform subsequent test configurations with a hardware based traffic generator. Subsequent test configurations can be performed with a NIC and software based traffic generation tools.