University of New Hampshire InterOperability Laboratory
Ethernet Consortium

Superseded

As of June 28th, 2000 the Ethernet Consortium Clause # 28 Auto Negotiation State Machine Base Page Exchange Conformance Test Suite version 4.0.2 has been superseded by the release of the Auto Negotiation State Machine Base Page Exchange Conformance Test Suite version 4.0.3. This document along with earlier versions, are available on the Ethernet Consortium test suite archive page.

Please refer to the following site for both current and superseded test suites:

http://www.iol.unh.edu/testsuites/ethernet/archive.html

FAST ETHERNET
&
GIGABIT ETHERNET

Clause 28 Auto-Negotiation
State Machine Test Suite

Technical Document

Last Updated: November 4, 1999 3:30 p.m.

Fast Ethernet Consortium
InterOperability Laboratory
Research Computing Center
University of New Hampshire

Morse Hall, Room 332
Durham, NH 03824
Phone: (603) 862-0166
Fax: (603) 862-1915
http://www.iol.unh.edu/consortiums/fe

Gigabit Ethernet Consortium
InterOperability Laboratory
Research Computing Center
University of New Hampshire

7 Leavitt Lane, Room 106
Durham, NH 03824
Phone: (603) 862-4822
Fax: (603) 862-4181
http://www.iol.unh.edu/consortiums/ge

MODIFICATION RECORD

- January 13, 2000 Version 4.0.1
  Ben Schultz: Minor editorial changes to the Initial Release.
- November 4, 1999 Version 4.0.0 Initial Release:
  Bob Noseworthy: Improved procedures, additional Management tests, and minor editorial changes from draft release.
- September 10, 1999 Version 4 draft release
- May 5, 1999 Version 3.1 Released

Modifications since last revision:

Updated to IEEE Std 802.3 1998 Edition and changed test numbering to conform with system used in other test suites. New: Test 28.2.2

Test Group 1: FLP Burst Transmission
- Test #28.1.1 - Separation of FLP Bursts
- Test #28.1.2 - Internal Separation of FLP Bursts
- Test #28.1.3 - Transmitted Link Code Word (Base Page) Encoding
- Test #28.1.4 - NLP Compliance

Test Group 2: FLP Burst Reception
- Test #28.2.1 - Acknowledge Bit
- Test #28.2.2 - Transmit Disable State
- Test #28.2.3 - Behavior with Incomplete FLPs
- Test #28.2.4 - Acceptance of Long FLPs
- Test #28.2.5 - Next Page and Remote Fault Bits
- Test #28.2.6 - Selector Field Reserved Combinations
- Test #28.2.7 - Technology Ability Field Reserved Bits
- Test #28.2.8 - Range of NLP Timer
- Test #28.2.9 - Identification of Link Partner as Auto-Negotiation Able
- Test #28.2.10 - Range of FLP Pulse Timer
- Test #28.2.11 - Range of Data Detect Timer
- Test #28.2.12 - Consistency Match
- Test #28.2.13 - Range of Break Link Timer
- Test #28.2.14 - Range of Link Fail Inhibit Timer
- Test #28.2.15 - Complete Acknowledge

Test Group 3: Establishing a Link
- Test #28.3.1 - Range of Link Loss Timer
- Test #28.3.2 - Link Count Max
- Test #28.3.3 - Single Link Ready
- Test #28.3.4 - Range of Link Test Timers
- Test #28.3.5 - Range of Auto-Negotiation Wait Timer
- Test #28.3.6 - Link Integrity and RD Active
- Test #28.3.7 - Parallel Detection of 10Base-T Devices
- Test #28.3.8 - Parallel Detection of 100Base-TX Devices
- Test #28.3.9 - Parallel Detection of 100Base-T4 Devices
- Test #28.3.10 - Priority Resolution Function
- Test #28.3.11 - Failed Link for HCD

Test Group 4: Next Page Functionality
- Test #28.4.1 - Transmitted Next Pages
- Test #28.4.2 - Next Page Consistency Matchs
- Test #28.4.3 - Null Message Page
- Test #28.4.4 - Next Page Bit
- Test #28.4.5 - Toggle Bit
- Test #28.4.6 - Message and Unformatted Pages
- Test #28.4.7 - Reception of Next Pages
- Test #28.4.8 - Transmit Disable
- Test #28.4.9 - Priority Resolution Following Next Page Exchange

- September 17, 1997 Version 3.01 Released

Modifications since last revision:

Most improvements apply to testing Figure 28-17.

Note test #7.28 was downgraded to informative due to the loose definition of the size of "Link Code Word"

New: Tests #21.28, #22.28, #23.28, #25.28, #39.28

Modified: Tests #3.28, #7.28, #24.28

Test Group 1: FLP Burst Transmission
- Test #1.28 - Separation of FLP Bursts
- Test #2.28 - Internal Separation of FLP Bursts
- Test #3.28 - Burst Content
- Test #4.28 - NLP Compliance
- Test #5.28 - Transmitted Link Code Word (Base Page) Encoding

Test Group 2: FLP Burst Reception
- Test #6.28 - Acknowledge Bit
- Test #7.28 - Refusal of Incomplete FLPs
- Test #8.28 - Acceptance of Long FLPs
- Test #9.28 - Next Page and Remote Fault Bits
- Test #10.28 - Selector Field Reserved Combinations
- Test #11.28 - Technology Ability Field Reserved Bits
- Test #12.28 - Range of NLP Timer
- Test #13.28 - Identification of Link Partner as Auto-Negotiation Able
- Test #14.28 - Range of FLP Pulse Timer
- Test #15.28 - Range of Data Detect Timer
- Test #16.28 - Consistency Match
- Test #17.28 - Range of Break Link Timer
- Test #18.28 - Range of Link Fail Inhibit Timer
- Test #19.28 - Complete Acknowledge

Test Group 3: Establishing a Link
- Test #20.28 - Complete Acknowledge
- Test #21.28 - Link Count Max
- Test #22.28 - Single Link Ready
- Test #23.28 - Range of Link Test Timers
- Test #24.28 - Range of Auto-Negotiation Wait Timer
- Test #25.28 - Link Integrity and RD Active
- Test #26.28 - Parallel Detection of 10Base-T Devices
- Test #27.28 - Parallel Detection of 100Base-TX Devices
- Test #28.28 - Parallel Detection of 100Base-T4 Devices
- Test #29.28 - Priority Resolution Function
- Test #30.28 - Failed Link for HCD

Test Group 4: Next Page Functionality
- Test #31.28 - Transmitted Next Pages
- Test #32.28 - Next Page Consistency Match
- Test #33.28 - Null Message Page
- Test #34.28 - Next Page Bit
- Test #35.28 - Toggle Bit
- Test #36.28 - Message and Unformatted Pages
- Test #37.28 - Reception of Next Pages
- Test #38.28 - Transmit Disable
- Test #39.28 - Priority Resolution Following Next Page Exchange

- April 16, 1997 Version 2.0 Released

Modifications since last revision:

Defined tests for Next Page testing

New: Tests #26.28, #27.28, #28.28, #29.28, #30.28. #31.28, #32.28, #33.28

Modified: Tests #9.28

Test Group 1: FLP Burst Transmission
- Test #1.28 - Separation of FLP Bursts
- Test #2.28 - Internal Separation of FLP Bursts

Test #3.28 - Number of Pulses in a Burst
Test #4.28 - NLP Compliance
Test #5.28 - Transmitted Link Code Word (Base Page) Encoding
Test Group 2: FLP Burst Reception
Test #6.28 - Acknowledge Bit
Test #7.28 - Refusal of Incomplete FLPs
Test #8.28 - Acceptance of Long FLPs
Test #9.28 - Next Page and Remote Fault Bits
Test #10.28 - Selector Field Reserved Combinations
Test #11.28 - Technology Ability Field Reserved Bits
Test #12.28 - Range of NLP Timer
Test #13.28 - Identification of Link Partner as Auto-Negotiation Able
Test #14.28 - Range of FLP Pulse Timer
Test #15.28 - Range of Data Detect Timer
Test #16.28 - Consistency Match
Test #17.28 - Range of Break Link Timer
Test #18.28 - Range of Link Fail Inhibit Timer
Test #19.28 - Range of Auto-Negotiation Wait Timer
Test Group 3: Establishing a Link
Test #20.28 - Complete Acknowledge
Test #21.28 - Parallel Detection of 10Base-T Devices
Test #22.28 - Parallel Detection of 100Base-TX Devices
Test #23.28 - Parallel Detection of 100Base-T4 Devices
Test #24.28 - Priority Resolution Function
Test #25.28 - Failed Link for HCD
Test Group 4: Next Page Functionality
Test #26.28 - Transmitted Next Pages
Test #27.28 - Next Page Consistency Matchs
Test #28.28 - Null Message Page
Test #29.28 - Next Page Bit
Test #30.28 - Toggle Bit
Test #31.28 - Message and Unformatted Pages
Test #32.28 - Reception of Next Pages
Test #33.28 - Transmit Disable

- January 7, 1997 Version 1.1 Released

Modifications since last revision:

Concatenated group 2 from Version 1.0 into test #5.28
Massive renumbering of tests and groups.
New: Tests #16.28, #17.28, #18.28, #19.28
Modified: Tests #5.28

Test Group 1: FLP Burst Transmission
Test #1.28 - Separation of FLP Bursts
Test #2.28 - Internal Separation of FLP Bursts
Test #3.28 - Number of Pulses in a Burst
Test #4.28 - NLP Compliance
Test #5.28 - Transmitted Link Code Word (Base Page) Encoding
Test Group 2: FLP Burst Reception
Test #6.28 - Acknowledge Bit
Test #7.28 - Refusal of Incomplete FLPs
Test #8.28 - Acceptance of Long FLPs
Test #9.28 - Next Page Bit
Test #10.28 - Selector Field Reserved Combinations
Test #11.28 - Technology Ability Field Reserved Bits
Test #12.28 - Range of NLP Timer
Test #13.28 - Identification of Link Partner as Auto-Negotiation Able
Test #14.28 - Range of FLP Pulse Timer
Test #15.28 - Range of Data Detect Timer
Test #16.28 - Consistency Match
Test #17.28 - Range of Break Link Timer
Test #18.28 - Range of Link Fail Inhibit Timer
Test #19.28 - Range of Auto-Negotiation Wait Timer
Test Group 3: Establishing a Link

Test #20.28 - Complete Acknowledge
Test #21.28 - Parallel Detection of 10Base-T Devices
Test #22.28 - Parallel Detection of 100Base-TX Devices
Test #23.28 - Parallel Detection of 100Base-T4 Devices
Test #24.28 - Priority Resolution Function
Test #25.28 - Failed Link for HCD

- October 14, 1996 Version 1.0 Released

Initial Release

Test Group 1: Transmitted FLP Burst Composition
Test #1.28 - Separation of FLP Bursts
Test #2.28 - Internal Separation of FLP Bursts
Test #3.28 - Number of Pulses in a Burst
Test #4.28 - NLP Compliance
Test Group 2: Transmitted Link Code Word (Base Page) Encoding
Test #5.28 - Transmitted Selector Field Combination
Test #6.28 - Transmitted Technology Ability Field
Test #7.28 - Remote Fault, Acknowledge, and Next Page Bits
Test Group 3: FLP Burst Reception
Test #8.28 - Acknowledge Bit
Test #9.28 - Refusal of Incomplete FLPs
Test #10.28 - Acceptance of Long FLPs
Test #11.28 - Range of NLP Timer
Test #12.28 - Range of FLP Pulse Timer
Test #13.28 - Identification of Link Partner as Auto-Negotiation Able
Test #14.28 - Range of Data Detect Timer
Test #15.28 - Next Page Bit
Test #16.28 - Technology Ability Field Reserved Bits
Test #17.28 - Selector Field Reserved Combinations
Test Group 4: Establishing a Link
Test #18.28 - Complete Acknowledge
Test #19.28 - Parallel Detection of 10Base-T Devices
Test #20.28 - Parallel Detection of 100Base-TX Devices
Test #21.28 - Parallel Detection of 100Base-T4 Devices
Test #22.28 - Priority Resolution Function
Test #23.28 - Failed Link for HCD

ACKNOWLEDGMENTS

The University of New Hampshire would like to acknowledge the efforts of the following individuals in the development of this test suite.

Andy Baldman	University of New Hampshire
Jerry Grand	National Semiconductor
Roy Lavender	University of New Hampshire
Eric Lynskey	University of New Hampshire
Bob Noseworthy	University of New Hampshire
Jake O'Dell	University of New Hampshire
Ben Schultz	University of New Hampshire
Karen Tuttle	University of New Hampshire
Ben Verschueren	University of New Hampshire

INTRODUCTION

Overview

The University of New Hampshire's InterOperability Laboratory (IOL) is an institution designed to improve the interoperability of standards based products by providing an environment where a product can be tested against other implementations of a standard. This suite of tests has been developed to help implementers evaluate the functioning of their Clause 28 Auto-Negotiation based products. The tests do not determine if a product conforms to the IEEE 802.3 standard, nor are they purely interoperability tests. Rather, they provide one method to isolate problems within an auto-negotiating device. Successful completion of all tests contained in this suite does not guarantee that the tested device will operate with other auto-negotiating devices. However, combined with satisfactory operation in the IOL's interoperability test bed, these tests provide a reasonable level of confidence that the Device Under Test (DUT) will function well in most auto-negotiating environments.

Organization of Tests

The tests contained in this document are organized to simplify the identification of information related to a test and to facilitate in the actual testing process. Each test contains an identification section that describes the test and provides cross-reference information. The discussion section covers background information and specifies why the test is to be performed. Tests are grouped in order to reduce setup time in the lab environment. Each test contains the following information:

Test Number

The Test Number associated with each test follows a simple grouping structure. Listed first is the Test Group Number followed by the test's number within the group. This allows for the addition of future tests to the appropriate groups of the test suite without requiring the renumbering of the subsequent tests.

Purpose

The purpose is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.

References

The references section lists cross references to the IEEE 802.3 standards and other documentation that might be helpful in understanding and evaluating the test and results.

Resource Requirements

The requirements section specifies the hardware, and test equipment that will be needed to perform the test. The items contained in this section are special test devices or other facilities, which may not be available on all devices.

Last Modification
This specifies the date of the last modification to this test.

Discussion
The discussion covers the assumptions made in the design or implementation of the test as well as known limitations. Other items specific to the test are covered here.

Test Setup
The setup section describes the configuration of the test environment. Small changes in the configuration should be included in the test procedure.

Procedure
The procedure section of the test description contains the step-by-step instructions for carrying out the test. It provides a cookbook approach to testing, and may be interspersed with observable results.

Observable Results
The observable results section lists observables that can be examined by the tester to verify that the DUT is operating properly. When multiple values are possible for an observable, this section provides a short discussion on how to interpret them. The determination of a pass or fail for a certain test is often based on the successful (or unsuccessful) detection of a certain observable.

Possible Problems
This section contains a description of known issues with the test procedure, which may effect test results in certain situations.

TABLE OF CONTENTS

GROUP 1: BASE PAGE TRANSMISSION

Scope: The following tests cover Auto-Negotiation operation specific to the transmission of Base Pages.

Overview: These tests are designed to verify that the device under tests transmits acceptable normal link pulses (NLPs), which are properly spaced, forming FLPs with acceptable content making up the Base Page transmitted by the device.

Test #28.1.1: Transmit Link Burst Timer

Purpose: To verify proper separation of consecutive fast link pulse (FLP) bursts.

References:

[1] IEEE Std 802.3, 1998 Edition: Subclause 28.3.2, Table 28-8, Figure 28-14 Transmit state diagram.

Resource Requirements:

- Line Monitor: A system capable of detecting, time stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.

Last Modification: July 28, 1999

Discussion: A station capable of Auto-Negotiation must transmit fast link pulse (FLP) bursts. Not only is the content and composition of these bursts important, but also the timing of the bursts. This test is designed to verify that the timing of the device under test's consecutive FLP bursts fall within the specified range of 5.7-22.3ms.

Test Setup: Using a Cat 5 cord, connect the DUT's transmitter to the Line Monitor. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. The DUT is configured to send FLP bursts
2. Monitor the transmitted bursts
3. The separation of each burst is measured from the last NLP sent in an FLP to the first NLP sent in the next FLP.

Observable Results:

The separation of FLP bursts from the last NLP in an FLP to the first NLP in the next FLP must be within the range of be 14 ± 8.3 ms.

Possible Problems: None.

Test #28.1.2: Interval Timer

Purpose: To verify that the device under test (DUT) transmits FLPs with valid pulse separation.

References:

[1] IEEE Std 802.3, 1998 Edition: Subclause 28.3.2, Table 28-8, Figure 28-14 Transmit state diagram.

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.

Last Modification: July 8, 1999

Discussion: To ensure that the content of an FLP burst is interpreted accurately, the individual pulses that make up the burst must be analyzed. This test is designed to verify that the device under test sends FLP bursts whose clock and data pulses are spaced properly. This spacing is governed by the Interval Timer which is defined to be within the range of 55.5us to 69.5us.

Test Setup: Using a Cat 5 cord, connect the DUT's transmitter to the Line Monitor. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. The DUT is configured to send FLP bursts
2. Monitor the transmitted bursts
3. The spacing between data/clock NLPs within an FLP is measured.

Observable Results:

- For data zeros, the spacing between clock pulses should be 125±14 us
- For data ones, the spacing from the clock to the data pulse, and from the data pulse to the clock pulse, should be 62.5±7 us.

Possible Problems: None.

Test #28.1.3: Transmit Link Code Word (Base Page) Encoding

Purpose: To verify that the device under test (DUT) transmits valid base page data.

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 28.2.1.1.1, 28.2.1.2, 28.2.1.2.1, 28.2.1.2.2, 28.2.1.2.3, 28.2.1.2.4, 28.2.1.2.5, Annex 28A, 28B, 28B.1, 28B.2

Resource Requirements:

- Line Monitor: A system capable of detecting and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The monitor should allow the NLPs to pass through while minimally impacting the channel.

Last Modification: July 27, 1999

Discussion: This test is designed to verify that the device under test transmits Link Code Words with acceptable content. There are defined selector field combinations that a station is permitted to transmit in its Link Code Word. The technology ability field of the Link Code Word advertises a station's abilities. The final three bits in the Link Code Word (Remote Fault bit, Acknowledge bit, Next Page bit) should all have a proper initial setting. The default value for the RF bit on a non-faulting link is zero. The Ack bit should be initially zero. The NP bit should be one if it supports Next Page exchange and zero if it doesn't or does not wish to implement a NP exchange. In this test, it is confirmed that the device under test transmits a Link Code Word with the selector field combination corresponding to IEEE 802.3, advertises the data service abilities that it supports in its technology ability field, and has the RF, Ack, and NP bits set correctly.

Test Setup: Using a Cat 5 cord, connect the DUT's transmitter to the Line Monitor. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. The DUT is configured to send FLP bursts
2. Monitor the transmitted bursts
3. The number of pulses and the data present in several bursts is observed
4. The contents of the selector field (first five data bits), technology ability field (D[5:12]), and of the Remote Fault bit, Acknowledge bit, and Next Page bit are acquired

Observable Results:

- The number of pulses in a burst should be 19-33 (inclusive)
- The selector field combination should correspond to S[4:0]=00001 as defined in table 28-9
- The technology ability field should advertise the proper abilities as indicated in table 28-10
- The DUT should not advertise any abilities that it does not possess
- The initial value of the Remote Fault bit should be zero
- The initial value of the Acknowledge bit should be zero
- The value of the Next Page bit should be one if it supports Next Page exchange and zero if it doesn't or does not wish to implement a NP exchange

Possible Problems: None.

Test #28.1.4: NLP Compliance

Purpose: To verify the device under test's link pulse waveforms meet specification.

References:

[1] IEEE Std 802.3, 1998 Edition Sections 14.3.1.2.1, Figure 14-12, 28.1.4.1, 28.2.1.1, 28.4
[2] IEEE Std 1802.3d-1993 Sections 6.3.4.8, 6.3.4.9

Resource Requirements:

- Oscilloscope: A digitizing signal analyzer which meets or exceeds the specifications for an oscilloscope as defined in IEEE Std 1802.3d-1993 Section 6.3.4.8
- Differential Voltage Probes: Meets or exceeds specifications defined in IEEE Std 1802.3d-1993 Section 6.3.4.9
- TP Test Card: A testing card with an RJ-45 interface with cable termination of Test Load 1, or Test Load 2 (as defined in IEEE 802.3 Section 14.3.1.2.1 and Figure 14-11) and an Unshielded twisted pair model (as defined in IEEE Std 802.3 Section 14.3.1.2) which can be inserted inline.

Last Modification: July 27, 1999

Discussion: All link pulses need to conform to the transmitter waveform specifications for Link Test Pulses defined in IEEE 802.3 Figure 14-12, including those contained in an FLP burst. This test is designed to verify that the device under test produces link pulses within specification.

Test Setup: Using Category 5 UTP cable, connect the DUT to the TP Test Card. Connect the Oscilloscope to the TP Test Card using Differential Voltage Probes.

Procedure:

1. The DUT is configured to send FLP bursts
2. Monitor the transmitted bursts
3. Observe the link pulse waveforms across each test load defined in fig. 14-11
4. Repeat procedure with loads connected through the twisted pair model (TPM).

Observable Results:

- Under each test setup, the FLP's link pulses should fit within the NLP template defined in Figure 14-12.
- After the differential output voltage drops below -50 mV, it shall remain below +50 mV.

Possible Problems: None.

Test #28.1.5: Break Link Timer

Purpose: To verify that the DUT ceases transmission within the acceptable range.

References:

[1] IEEE Std 802.3, 1998 Edition: Section 28.2.3.2, 28.3

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: August 27, 1999

Discussion: Once a device has entered the TRANSMIT DISABLE state, it must wait a specified amount of time before it restarts the Auto-Negotiation process. This time is defined by the device's "break_link_timer," and is required to be between 1200 and 1500 ms. This test is designed to verify that the device under test restarts the Auto-Negotiation process after entering the TRANSMIT DISABLE state within this range.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Establish a connection (not a link) to the DUT
2. Use the Traffic Generator to put the DUT in the ACKNOWLEDGE DETECT state. Send a series of 20 identical, validly formed FLP bursts without the ACK bit set. Once reception of the FLP bursts cease, the DUT should enter the TRANSMIT DISABLE state.
3. Verify that the DUT restarts Auto-Negotiation.
4. Measure the amount of time between when the DUT ceased FLP transmission (upon entry of the TRANSMIT DISABLE state) and when the first FLP of the re-negotiation process was transmitted. This time will be the value of break_link_timer plus any additional gap due to partial completion of an FLP's transmit_link_burst_timer.
5. Repeat steps 2 thru 4 several times.

Observable Results:

- Assuming a fixed value for the implemented break_link_timer, the minimum of the observed gaps is the DUT's break_link_timer, which should be in the range of 1200 to 1500 ms

Possible Problems: If the DUT fails to enter the ACKNOWLEDGE DETECT state, the number of FLPs sent may need to be increased (see 28.2.1 Ability Match) or the encoding of the FLPs may need to be altered. If the DUT does not restart Auto-Negotiation due to a flp_receive_idle=true while in ACKNOWLEDGE DETECT, then a consistency match error could be sent to the DUT to try to cause an Auto-Negotiation restart (see 28.2.3 Consistency Match). Else, resetting the DUT's phy and/or restarting Auto-Negotiation via management should also produce a break_link_timer gap, measurable via the techniques outlined above.

Test #28.1.6: Link Fail Inhibit Timer

Purpose: To verify that the device under test will wait a specified amount of time between when it parallel detects a link partner and when it establishes that link.

References:

[1] IEEE Std 802.3, 1998 Edition: Section 28.2.3.2, 28.3

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: July 27, 1999

Discussion: Once a device has entered the FLP LINK GOOD CHECK state, it must receive a link_status=OK message from its link partner within a specified amount of time. If this message is not received, it will enter the TRANSMIT DISABLE state and wait for the duration of its break_link_timer before starting a re-negotiation. This time is defined by the device's "link_fail_inhibit_timer," and is required to be between 750 and 1000 ms. This test is designed to verify that the device under test enters the TRANSMIT DISABLE state from the FLP LINK GOOD CHECK state when a link_status=OK message is not received from its link partner in the acceptable range of time.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

Part A:

1. Establish a connection (not a link) to the DUT
2. Use the Traffic Generator to put the device into the COMPLETE ACKNOWLEDGE state. Any method is acceptable. Ex: Send 20 FLPs without ACK set, then 20 FLPs with ACK set.
3. Verify that the DUT restarts Auto-Negotiation.
4. Measure the amount of time between when the station transmitted it's final FLP after entering the COMPLETE ACKNOWLEDGE state and when the first FLP of the renogotiation process was transmitted. This will be the value of break_link_timer + link_fail_inhibit_timer plus any additional gap due to partial completion of an FLP's transmit_link_burst_timer.
5. Subtract the value of break_link_timer (see results of test #28.1.5) from the minimum observed value to acquire the value of link_fail_inhibit_timer

Part B – for devices with a 10Base-T PMA:

6. Repeat steps 1-3 above, changing the advertised abilities to include only 10Base-T abilities.

7. Measure the amount of time NLPs are sent from the DUT and verify it is also link_fail_inhibit_timer.

Observable Results:

- All observations of the DUT's link_fail_inhibit_timer should be in the range of 750 to 1000 ms

Possible Problems: None.

Test #28.1.7: Remote Fault Bit

Purpose: To verify that if the DUT implements the Remote Fault function, that the DUT properly sets the remote fault bit in its Link Code Word and keeps the remote fault bit set until the COMPLETE ACKNOWLEDGE state has been reached.

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 28.2.3.5

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: September 29, 1999

Discussion: A device that elects to support the Remote Fault function must not reset the RF encoding until the device transitions to the COMPLETE ACKNOWLEDGE state during base page exchange, thus ensuring that the link partner receives the fault indication. This test observes the device's transmitted RF bits when signaling a remote fault, in order to determine if the device continues sending the RF code until the COMPLETE ACKNOWLEDGE state is entered.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. If the DUT supports the indication of a remote fault, then cause the DUT to indicate a remote fault by any means, else this test cannot be performed.
2. Verify that the DUT is sending a Link Code Word with the Remote Fault bit set.
3. Send the DUT a series of FLPs such that the DUT should obtain an ability match (see test 28.2.2)
4. Observe transmissions from the DUT
5. Repeat steps 3-4 but send the DUT enough FLPs to obtain both an ability match and an acknowledge match.
6. Observe transmissions from the DUT

Observable Results:

- In part 2, the DUT should have the Remote Fault bit set in all FLPs that are transmitted
- In part 4, the DUT should have the Remote Fault bit set when it sends FLPs with the ACK bit set, and when the DUT restarts Auto-Negotiation, the Remote Fault bit should still be set.
- In part 6, when the DUT restarts Auto-Negotiation, the Remote Fault bit should not be set

Possible Problems: None.

Test #28.1.8: Failed Link for HCD

Purpose: To verify that the device under test starts a re-negotiation upon the reception of a link_status=FAIL from the resolved highest common denominator (HCD) technology.

References:

[1] IEEE Std 802.3, 1998 Edition: Section 28.2.3.2

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) as well as valid link signaling and frames for 10/100/1000Base-T and recording received frames while connected to the receiver of the DUT.

Last Modification: January 13, 2000

Discussion: Once the highest common denominator (HCD) technology has been determined through the parallel detection function, if a station receives a link_status=FAIL message from that priority, it should cause a re-negotiation. This test is designed to verify that the device under test does start a re-negotiation upon the receipt of a link_status=FAIL message from the HCD technology.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Use the Traffic Generator to send a series of FLP bursts that advertise a set of abilities compatible with the DUT.
2. Verify the DUT resolves the HCD and establishes a link
3. Break the link to the Traffic Generator, leaving the Line Monitor attached to the DUT, thus causing the DUT to see a link_status=FAIL for the HCD link.
4. Verify that the DUT starts a re-negotiation

Observable Results:

- Upon reception of the link_status=FAIL message, the DUT should disable all transmission for approximately break_link_timer and restart Auto-Negotiation.

Possible Problems: None.

GROUP 2: BASE PAGE RECEPTION

Scope: The following tests cover Auto-Negotiation operation specific to the reception of Base Pages.

Overview: These tests are designed to verify that the device under tests reacts properly to the receipt of both valid and invalid fast link pulse (FLP) bursts.

Test #28.2.1: Ability Match

Purpose: To verify that the device under test enters the ACKNOWLEDGE DETECT state upon reception of complete, consecutive and consistent FLP bursts, ignoring the value of the Acknowledge bit.

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 28.2.1.2, 28.1.4.2, 28.2.1.2.4

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: January 13, 2000

Discussion: Once an auto-negotiating device identifies its link partner as Auto-Negotiation able, it will enter the ACKNOWLEDGE DETECT state only after it receives at least 3 complete, consecutive and consistent Link Code Words from its link partner, ignoring the Acknowledge bit. Once the ACKNOWLEDGE DETECT state is entered, the station should send out FLP bursts containing its Link Code Word with the Acknowledge bit (the fifteenth data pulse) set to logic one. This test is designed to verify that the device under test will set the Acknowledge bit after the reception of 3 or more complete, consecutive and consistent Link Code Words.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

Part A:

1. Use the Traffic Generator to send 1 FLP to the DUT.
2. Monitor the FLPs sent back by the DUT and determine whether the Acknowledge bit is set
3. If it was not set, repeat the procedure with an increasing number (n) of FLPs until the Acknowledge bit is set.
4. Send (n) FLPs to DUT all with the Acknowledge bit set to a logic one. Where (n) is the minimum number of FLPs determined in step 3 to put the DUT in the ACKNOWLEDGE DETECT state.
5. Repeat step 4 using FLPs that have Acknowledge bits that alternate between 1 and 0.

Part B:

6. Use the Traffic Generator to send (n) FLPs, alternating between an initial FLP and a valid FLP containing different advertised abilities, such that the number of FLPs would be enough to put the station into the ACKNOWLEDGE DETECT state
7. Monitor the FLPs sent back by the DUT and determine whether the Acknowledge bit is set

8. Repeat steps 6-7 by sending all combinations of FLPs that are one bit different than the initial FLP

Part C:

9. Send a series of FLPs designed to put the DUT in the ACKNOWLEDGE DETECT State.
10. Monitor the FLPs sent from the DUT after returning to the ABILITY DETECT state and determine whether the Acknowledge bit is set

Observable Results:

a) The Acknowledge bit should be set after the reception of at least 4 complete and matching FLPs, regardless of the value of the Acknowledge bit. Record the number of FLPs required to put the DUT into the ACKNOWLEDGE DETECT state for use in later tests
b) The DUT should not enter the ACKNOWLEDGE DETECT state and thus the Acknowledge bit should never be set.
c) Upon returning to the ABILITY DETECT state, the DUT should reset to its default base page and send FLPs without the Acknowledge Bit set

Possible Problems: None.

Test #28.2.2: Acknowledge Match

Purpose: To verify that the device under test enters the COMPLETE ACKNOWLEDGE state only after receiving 3 consecutive and consistent FLPs with the Acknowledge bit set.

References:

[1] IEEE Std 802.3, 1998 Edition: Section 28.2.1.2.4

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: September 29, 1999

Discussion: Well into the Auto-Negotiation process is the COMPLETE ACKNOWLEDGE state. A station reaches this state after first entering the ACKNOWLEDGE DETECT state (which is done when at least 3 complete, consecutive and consistent FLP bursts are received, ignoring the Acknowledge bit, - see Test #28.4.1), and then receiving 3 complete, consecutive and consistent FLPs with the Acknowledge bit set. This test is designed to verify that the device under test requires the reception of 3 consecutive and consistent FLPs with the Acknowledge bit set before doing entering the COMPLETE ACKNOWLEDGE state.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

Part A:

1. Use the Traffic Generator to send a series of (n) FLPs with the Acknowledge bit not set followed by (m) FLPs with the Acknowledge bit set to logic one but otherwise identical to the initial FLPs. Where (n) is the value found in test #28.2.1 to cause the DUT to enter the ACKNOWLEDGE DETECT state. (m) is initially set to one.
2. Observe transmissions from the DUT.
3. Repeat steps 1-2 increasing (m), until the DUT is observed to enter into the COMPLETE ACKNOWLEDGE state.

Part B:

4. Use the Traffic Generator to send two groups of FLPs. The first group consists of (n) FLPs with the Acknowledge bit not set. The second group consists of (2m) FLPs which alternate between FLPs which are identical to the first group, and FLPs which are one bit different from the first group, but all FLPs in this group have the Acknowledge bit set.
5. Repeat step 4 using all one bit different FLPs.

Observable Results:

a) The DUT should enter the COMPLETE ACKNOWLEDGE state after receiving three FLPs with the Acknowledge bit set to logic one.
b) The DUT should never enter the COMPLETE ACKNOWLEDGE state, and should send out FLPs with the Acknowledge bit set until nlp_test_max_timer expires. Following the FLPs should be a gap of 'break_link_timer' until FLP transmission resumes.

Note: Observing if the DUT has previously entered the COMPLETE ACKNOWLEDGE state can be most easily accomplished by any of three methods. By observing the transmission of a Next Page, if a Next Page exchange is required. By observing the transmission of the highest common denominator link signaling, if a link is to be established. Or timing the cessation of FLP transmission to the resumption of FLP transmission if a link is to be established, but no link signaling is provided to the DUT. In this last case, the gap should be link_fail_inhibit_timer + break_link_timer.

Possible Problems: None.

Test #28.2.3: Consistency Match

Purpose: To verify that the device under test performs a consistency match test on received FLPs.

References:

[1] IEEE Std 802.3, 1998 Edition: Section 28.3.1

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: September 29, 1999

Discussion: Upon entering the ACKNOWLEDGE DETECT state of the Auto-Negotiation process, a device must receive 3 consecutive and consistent FLPs from its link partner before it can proceed. However, these FLPs must not only be consistent amongst themselves, but also with the FLPs that the device received to put it into the ACKNOWLEDGE DETECT state. To ensure this, a station must perform a consistency match test. If a consistency mismatch occurs, the device should enter the TRANSMIT DISABLE state and cease sending FLPs. This test is designed to verify that the device under test checks to be sure that the FLPs received in the ACKNOWLEDGE DETECT state are consistent (ignoring the Acknowledge bit) with the FLPs that it received to get it there.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

Part A:

1. Use the Traffic Generator to send two groups of FLPs. The first group consists of (n) FLPs with the Acknowledge bit not set. The second group consists of (m) FLPs are one bit different from the first group, but all FLPs in this group have the Acknowledge bit set. Where (n) is the value found in test #28.2.1 to cause the DUT to enter the ACKNOWLEDGE DETECT state. And where (m) is the value found in test #28.2.2.
2. Monitor the transmit line coming from the DUT
3. Repeat steps 1-2 toggling all bits of the FLPs, except the ACK bit.

Part B: Minimum number of FLPs to complete Auto-Negotiation

4. Use the Traffic Generator to send (n) FLPs all with the Acknowledge bit set. Where (n) is the value found in test #28.2.1 to cause the DUT to enter the ACKNOWLEDGE DETECT state.
5. Monitor the transmit line coming from the DUT.

6. Repeat steps 4-5 increasing the number of FLPs sent until the DUT is observed to enter the COMPLETE ACKNOWLEDGE state.

Observable Results:

a) The DUT should cease transmitting FLPs once the inconsistent FLPs are received
b) The DUT should enter COMPLETE ACKNOWLEDGE after reception of 4 or 5 FLPs with the ACK bit set.

Possible Problems: None

Test #28.2.4: Complete Acknowledge

Purpose: To verify that the device under test sends out a valid number of Link Code Words after the COMPLETE ACKNOWLEDGE state has been entered.

References:

[1] IEEE Std 802.3, 1998 Edition: Section 28.2.1.2.4, 28.3.1, 28.3.4 Figure 28-16

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: August 23, 1999

Discussion: Well into the Auto-Negotiation process is the COMPLETE ACKNOWLEDGE state. A station reaches this state after first entering the ACKNOWLEDGE DETECT state (which is done when at least 3 complete, consecutive and consistent FLP bursts are received, ignoring the Acknowledge bit- see Test #6.28), and then receiving 3 complete, consecutive and consistent FLPs with the Acknowledge bit set. Once the COMPLETE ACKNOWLEDGE state has been entered, a station should send out 6 to 8 (inclusive) more FLPs containing its Link Code Word and with the Acknowledge bit set to 1. This test is designed to verify that the device under test sends out 6 to 8 (inclusive) FLPs after entering the COMPLETE ACKNOWLEDGE state.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Establish a connection (not a link) to the DUT
2. Use the Traffic Generator to send a series of FLPs- first some with the Acknowledge bit not set (enough to put the DUT into the Acknowledge Detect state- refer to results of test #28.2.1) followed by 3 with the Acknowledge bit set to logic one, to put the DUT into the COMPLETE ACKNOWLEDGE state
3. Monitor the transmit line coming from the DUT and count the number of FLPs sent by the DUT after the COMPLETE_ACKNOWLEDGE state has been entered

Observable Results:

- After COMPLETE ACKNOWLEDGE state has been entered, the DUT should send out 6 to 8 (inclusive) FLPs containing its Link Code Word. Following the FLPs should be a gap of link_fail_inhibit_timer + break_link_timer until FLP transmission resumes.

Possible Problems: None

Test #28.2.5: Behavior with Incomplete FLPs

Purpose: To observe the device under test's behavior upon receipt of incomplete FLP bursts.

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 28.2.1.2, 28.3.1 & Figures 28-7, 28-15 Receive state diagram

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: January 13, 2000

Discussion: This test identifies how a given implementation chooses to handle FLPs with less than 16 data positions. While Figure 28-15 'Receive state diagram', will accept incomplete FLPs without error, a difficulty in interpretation lies with the definition of 'ability_match' in 28.3.1. Here it is stated that the Acknowledge bit will be set upon reception of three matching consecutive Link Code Words. While section 28.2.1.2 and Figure 28-7 'Base page encoding' suggest a Link Code Word is 16 bits, this is not stated explicitly. Thus, if one interprets a Link Code Word to be 16 bits (or greater, refer to #28.2.6), then any FLP containing less than 16 data positions would be ignored as such a short FLP would not be used in the ability_match function. Alternatively, if a Link Code Word is interpreted to mean any length bit-vector, then any short/incomplete FLP must be used in an ability_match. This would allow for the possibility of ability_match being set to true upon receipt of three matching consecutive, but short, FLPs. While such a scenario would undoubtedly present problems, the likelihood seems small. A benefit gained through such an approach may be increased robustness as incomplete FLPs resulting from error conditions and/or line noise will not be ignored by the auto-negotiating device, as is the case in the first case.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

Part A:

1. Establish a connection (not a link) to the DUT.
2. Use a Traffic Generator to send the DUT enough incomplete FLPs, consisting of only 9 clock pulses and spaced so that the time to send all four FLPs is larger than nlp_test_max_timer, to put the DUT into the ACKNOWELDGE DETECT state. (see test #28.2.1)
3. Observe whether the DUT entered the ACKNOWLEDGE DETECT state.

Part B: (informative)

4. Establish a connection (not a link) to the DUT
5. Use a Traffic Generator to send the DUT enough incomplete FLPs consisting of only 10 data bits to put the DUT into the ACKNOWLEDGE DETECT state (see test #28.2.1)
6. Observe whether the DUT entered the ACKNOWLEDGE DETECT state
7. Repeat steps 4-6, incrementing the number of data bits until the DUT is observed to enter the ACKNOWLEDGE DETECT state.

Part C:

8. Establish a connection (not a link) to the DUT
9. Use a Traffic Generator to send the DUT a series of the following 2 FLPs alternating at 16 ms apart: a 17 pulse FLP containing the following data: 1 1 0 0 0 1 1 1 1 1 with no clock pulse after the final 1 an 8 pulse FLP containing the following data: 0 0 0 0 1 0 with a final clock pulse
10. Observe whether the DUT entered the Acknowledge Detect state

Observable Results:

a) The DUT should not enter the ACKNOWLEDGE DETECT state.
b) As mentioned in the discussion above, a DUT may or may not enter the ACKNOWLEDGE DETECT state when the number of data bits is less than 16, corresponding to 17 clock pulses. The number of clock pulses at which the DUT enters the ACKNOWLEDGE DETECT state is the rx_bit_cnt_check value. This value needs to lie between 10 and 17.
c) The DUT should not enter the ACKNOWLEDGE DETECT state.

Possible Problems: None

Test #28.2.6: Acceptance of Long FLPs

Purpose: To verify that the device under test properly accepts FLPs that have more than 16 data positions by ignoring all but the first 16 data bits.

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 28.2.2, 28.2.2.1, 28.3.3 (Rx_bit_cnt), Figure 28-15 Receive state diagram

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: January 13, 2000

Discussion: An FLP burst normally consists of 17 to 33 pulses, with normally 16 data bits. However, if a device receives an FLP with more than 16 data positions, it should still accept the burst. The first 16 data bits should be kept and any additional should be ignored. This test is designed to determine whether the Device Under Test properly accepts FLPs with more than 16 data bits.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

Part A:

1. Use a Traffic Generator to send enough valid FLPs with 1 extra data position corresponding to a '1' (1 extra clock pulse and 1 data pulses) attached to the end to put the DUT into the Acknowledge Detect state (see #28.2.1).
2. Observe whether the DUT enters the ACKNOWLEDGE DETECT state.

Part B:

3. Repeat steps 1 and 2 above, sending 5 additional data bits corresponding to 10001.

Observable Results:

- The DUT should enter the ACKNOWLEDGE DETECT state in both cases

Possible Problems: None

Test #28.2.7: Next Page and Remote Fault Bits

Purpose: To verify that the device under test can handle the reception of an FLP from a Next Page capable device as well as the reception of a flagged remote fault bit.

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 28.2.1.2, 28.2.1.2.3, 28.2.1.2.5, 28.2.3.4, 28.2.3.5

Resource Requirements:

- Line Monitor: A system capable of detecting, time stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: July 27, 1999

Discussion: When a station is connected to a Next Page able device, it will receive FLP bursts with set Next Page bits (the final bit of the Link Code Words set to logic one). Regardless of whether the receiving station is Next Page able or not, it should still accept the Link Code Word as valid. When connected to any station, it is possible for a device to receive a logic one in the Remote Fault (RF) bit position (bit D13) of the Link Code Word. If a device supports the remote fault function, the only defined behavior is to set the remote fault bit in the MII status register. Other than that, there is no specification as to what action a device should take upon reception of a remote fault. This test is designed to verify that the device under test is capable of receiving a flagged Next Page and/or remote fault bit.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

Part A:

1. Establish a connection (not a link) to the DUT
2. Use the Traffic Generator to send enough FLPs with the Next Page bit set to a logic one to put it into the COMPLETE ACKNOWLEDGE state (see tests #28.2.1 Ability Match and #28.2.2 Acknowledge Match)
3. Verify that the DUT enters the COMPLETE ACKNOWLEDGE state

Part B:

4. Repeat with FLPs with the remote fault bit set to a logic one

Observable Results:

a) The DUT should enter the COMPLETE ACKNOWLEDGE state

b) The DUT should enter the COMPLETE ACKNOWLEDGE state. If the DUT supports the remote fault function, then the DUT should set the remote fault bit in its MII status register, and any other behavior is unpredictable

Possible Problems: None

Test #28.2.8: Selector Field Combinations

Purpose: To verify that the device under test accepts FLPs with the selector field set to a reserved combination or to the defined Isochronous Ethernet combination.

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 28.2.1.2, 28.2.1.2.1, 28.3.1, Annex 28A, 28B, 28B.1

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: January 13, 2000

Discussion: There are combinations for the selector field that are reserved by the IEEE. A station is never supposed to transmit these combinations, but there are no specifications as to the combinations that can be received. Therefore, as long as complete and consistent Link Code Words are received, a station should accept them as valid regardless of the selector field combination. This test is designed to verify that the device under test will accept a Link Code Word with the selector field set to a reserved combination. A second Selector Field combination has been defined as Isochronous Ethernet (0,1,0,0,0).

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

Part A: ACKNOWLEDGE DETECT with different selector field combinations

1. Establish a connection (not a link) to the DUT
2. Use the Traffic Generator to send enough FLPs with the selector field combination of 0,0,1,1,1 (ordered bit S0 to S4) to put it into the ACKNOWLEDGE DETECT state (see test #28.2.1)
3. Verify that the DUT enters the ACKNOWLEDGE DETECT state
4. Repeat steps 2 and 3 changing the selector field combination to 0,1,0,0,0

Part B: COMPLETE ACKNOWLEDGE with different selector field combinations

5. Use the Traffic Generator to send enough FLPs with the selector field combination of 0,0,1,1,1 (ordered bit S0 to S4) with the ACK bit set to put it into the COMPLETE ACKNOWLEDGE state (see test #28.2.1)
6. Repeat step 5 changing the selector field combination to 0,1,0,0,0

Observable Results:
a) The DUT should enter the ACKNOWLEDGE DETECT state.
b) The DUT should enter the COMPLETE ACKNOWLEDGE state.

Possible Problems: None

Test #28.2.9: Technology Ability Field Bits

Purpose: To verify that the device under test accepts FLPs with different combinations of the technology ability field bits set to logic one.

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 28.2.1.2, 28.2.1.2.2, 28.2.3.3, Annex 28B.2

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: January 13, 2000

Discussion: The technology ability field contains eight bits that indicate supported technologies specific to the selector field value. Bits A0:A4 are encoded as 10Base-T, 10Base-T full duplex, 100Base-Tx, 100Base-Tx full fuplex, 100Base-T4, and Pause operation for full duplex links, respectively. The last three bits of the technology ability field of a Link Code Word are reserved by the IEEE. A station is supposed to transmit these bits as logic zero. Regardless of what abilities a device advertises, it is supposed to be able to receive any of the technology ability field bits set to a one without a problem. This test is designed to verify that the device under test will accept a Link Code Word with various combinations of the technology ability field set to logic one.

Test Setup: Using a Cat 5 cord, connect the DUT's transmitter to the Line Monitor. Terminate the DUT's transmit channel with a 100Ω line termination. Using a Cat 5 cord, connect the DUT's receiver to the Traffic Generator using a 100Ω line termination.

Procedure:

1. Establish a connection (not a link) to the DUT
2. Use the Traffic Generator to send enough FLPs with bit A0 set to logic one to put it into the ACKNOWLEDGE DETECT state (see test #28.2.1)
3. Verify that the DUT enters the ACKNOWLEDGE DETECT state
4. Repeat steps 1-3 but send FLPs encoded with bit combinations set to logic one including A1, A2, A3, and A4.

Observable Results:

- The DUT should enter the ACKNOWLEDGE DETECT state regardless of the received value of the technology ability field bits.

Possible Problems: None

Test #28.2.10: Identification of Link Partner as Auto-Negotiation Able

Purpose: To verify that the device under test is able to recognize its link partner as capable of Auto-Negotiation within specification.

References:

[1] IEEE Std 802.3, 1998 Edition: Section 28.2.2.1, Figure 28-15, Receive state diagram.

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: January 13, 2000

Discussion: When establishing a link, a station is required to recognize its link partner as Auto-Negotiation able within a certain range of pulses in an FLP burst. This test is designed to verify that the device under test adheres to this range. As determined from the Receive state diagram, flp_cnt is determined to be 1 less than the number of pulses required to recognize its link partner as Auto-Negotiation able.

Test Setup: Using a Cat 5 cord, connect the DUT's transmitter to the Line Monitor. Terminate the DUT's transmit channel with a 100Ω line termination. Using a Cat 5 cord, connect the DUT's receiver to the Traffic Generator using a 100Ω line termination.

Procedure:

1. Establish a connection (not a link) to the DUT
2. Use a Traffic Generator to send the DUT pulses (beginning with one pulse) spaced at 50μs, wait 16ms, then send enough valid FLP bursts to put the DUT into the ACKNOWLEDGE DETECT state. The proper number of FLP bursts should be one less than the value determined in test #28.2.1, as that value includes the FLP required to identify a device as Auto-Negotiation able.
3. Determine whether the DUT has entered the ACKNOWLEDGE DETECT state
4. If the DUT did not enter the ACKNOWLEDGE DETECT state, repeat steps 1 through 3 increasing the number of initial pulses until the DUT enters the ACKNOWLEDGE DETECT state

Observable Results:

- The DUT should recognize the Link Partner as Auto-Negotiation able within 7 to 18 (inclusive) pulses. Flp_cnt is one less than this determined number

Possible Problems: None

Test #28.2.11: Range of NLP Timer

Purpose: To verify that the device under test accepts FLP bursts with proper spacing, and refuses those with spacing outside of the acceptable range.

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 28.2.2.1, 28.3.2

Resource Requirements

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: January 13, 2000

Discussion: As well as characteristic requirements, FLP bursts have requirements for the delay between consecutive bursts. In order to be accepted, as valid, received FLP bursts must have a delay between them between "nlp_test_min_timer" and "nlp_test_max_timer." The value for "nlp_test_min_timer" must be between 5 and 7ms. The value for "nlp_test_max_timer" must be between 50 and 150ms. This test is to verify that the device under test accepts FLP bursts with spacing within these ranges, and refuses FLP bursts with spacing outside of these ranges. Note, "nlp_test_min_timer" is measured from the beginning of an FLP to the beginning of the next FLP, whereas "nlp_test_max_timer" is measured from the end of an FLP to the beginning of the next FLP.

Test Setup: Using a Cat 5 cord, connect the DUT's transmitter to the Line Monitor. Terminate the DUT's transmit channel with a 100Ω line termination. Using a Cat 5 cord, connect the DUT's receiver to the Traffic Generator using a 100Ω line termination.

Procedure:

Part A: nlp_test_min_timer

1. Establish a connection (not a link) to the DUT
2. Use a Traffic Generator to send the DUT enough FLP bursts spaced between 2ms and 10ms to put it into the ACKNOWLEDGE DETECT state (see test #28.2.1)
3. Observe whether the DUT entered the ACKNOWLEDGE DETECT state
4. Repeat steps 1 through 3 varying the spacing of the FLPs until the DUT range at which DUT enters the ACKNOWLEDGE DETECT state and does not enter the ACKNOWLEDGE DETECT state is found.

Part B: nlp_test_max_timer

5. Repeat steps 1 through 3 varying the spacing of the FLPs starting between 30ms and 200ms, until the range at which DUT enters the ACKNOWLEDGE DETECT state and does not enter the ACKNOWLEDGE DETECT state is found.

Observable Results:

a) The nlp_test_min_timer should lay between 5ms and 7ms
b) The nlp_test_max_timer should lay between 50ms and 150ms

Possible Problems: None

Test #28.2.12: Range of FLP Test Timer

Purpose: To verify that the device under test determines that its link partner is Auto-Negotiation able upon receiving pulses spaced within flp_test_min_timer and flp_test_max_timer, and does not recognize a device as Auto-Negotiation able upon receiving pulses spaced outside the acceptable range.

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 28.2.2.1, 28.3.2, Figure 28-15 Receive state diagram

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: July 27, 1999

Discussion: As well as characteristic requirements, FLP bursts have requirements for the delay between consecutive pulses within the burst. In order to be accepted, as valid, received pulses must have a delay between them between "flp_test_min_timer" and "flp_test_max_timer." The value for "flp_test_min_timer" must be between 5 and 25 μs. The value for "flp_test_max_timer" must be between 165 and 185 μs. This test is to verify that the device under test accepts FLP bursts with pulses spaced within these ranges, and refuses FLPs with pulses spaced outside of these ranges.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

Part A: flp_test_min_timer

1. Establish a connection (not a link) to the DUT
2. Use a Traffic Generator to send the DUT enough pulses spaced at 5μs to identify the link partner as Auto-Negotiation able (refer to #28.2.10), wait 16ms, then send enough valid FLP bursts to put the DUT into the ACKNOWLEDGE DETECT state. The proper number of FLP bursts should be one less than the value determined in #28.2.1 as that value includes the FLP required to identify a device as Auto-Negotiation able.
3. Observe whether the DUT entered the ACKNOWLEDGE DETECT state
4. Repeat steps 1 through 3 varying the pulse spacing until the DUT enters ACKNOWLEDGE DETECT state

Part B: flp_test_max_timer

5. Repeat steps 1 through 3 varying the pulse spacing, starting at 185µs until the DUT enters the ACKNOWLEDGE DETECT state

Observable Results:

a) The flp_test_min_timer should lay between 5µs and 25µs
b) The flp_test_max_timer should lay between 165µs and 185µs

Possible Problems: None

Test #28.2.13: Range of Data Detect Timer

Purpose: To verify that the device under test accepts data pulses with proper spacing and refuses data pulses with spacing outside the acceptable range.

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 28.2.2.1, 28.3.2, Figure 28-15 Receive state diagram

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: January 13, 2000

Discussion: As well as characteristic requirements, FLP bursts have requirements for the delay between clock and data pulses within the burst. In order to be accepted as valid, received data pulses must have a delay between them and the previous clock pulse between "data_detect_min_timer" and "data_detect_max_timer." The value for "data_detect_min_timer" must be between 15 and 47 μs. The value for "data_detect_max_timer" must be between 78 and 100 μs. This test is designed to verify that the device under test accepts FLP bursts with data pulses spaced within these ranges, and ignores FLPs with data pulses spaced outside of these ranges. As defined in Figure 28-15, if an FLP containing the data pattern 1,0 is sent with the data 1 transmitted a time exceeding 100 μs following the clock pulse, then the data_detect_max_timer should be violated. In a conformant device, this should result in the interpretation of the data pattern as 0,1. Thus, by alternating the transmission of this test FLP with FLPs containing typical spacing, a conformant device should not enter the ACKNOWLEDGE DETECT state. This technique is used to test the validity of data_detect_max_timer.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

Part A: data_detect_min_timer

1. Establish a connection (not a link) to the DUT
2. Use the Traffic Generator to send the DUT enough FLPs, alternating between FLPs with the first data pulse spaced 15μs from the clock pulse and FLPs with perfect spacing, to put it into the ACKNOWLEDGE DETECT state (see test #28.2.1)
3. Observe whether the DUT entered the ACKNOWLEDGE DETECT state

Repeat steps 1 through 3, varying the gap from the clock pulse to the data pulse until the DUT enters the ACKNOWLEDGE DETECT state

Part B: data_detect_max_timer

4. Repeat steps 1 through 3, varying the gap from the clock pulse to the data pulse, starting at 100µs, until the DUT enters the ACKNOWLEDGE DETECT state

Part C: ignoring pulses below data_detect_min_timer

5. Repeat steps 1 through 3, changing the FLP to contain two "data" pulses, one before the implemented data_detect_min_timer is finished, and another after the data_detect_min_timer is finished. (the time between the clock and the first data pulse should be the same as the time between the two data pulses).

Observable Results:

a) The data_detect_min_timer should lay between 15µs and 47µs
b) The data_detect_max_timer should lay between 78µs and 100µs
c) The DUT should ignore the first data pulse and decode the second data pulse as a logic one causing the DUT to enter the ACKNOWLEDGE DETECT State

Possible Problems: None

Test #28.2.14: Transmit Disable State

Purpose: To verify that the device under test enters the ABILITY DETECT state upon completion of break_link_timer from the TRANSMIT DISABLE state

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 28.2.1.2, 28.1.4.2, 28.2.1.2.4

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: July 28, 1999

Discussion: Once an auto-negotiating device enters the TRANSMIT DISABLE state, it should stop transmission for break_link_timer before it re-enters the ABILITY DETECT state. However, there is no specification as to whether the DUT's receiver has to be turned off in the TRANSMIT DISABLE state. If a sequence of FLPs designed to cause an auto-negotiating station to enter the ACKNOWLEDGE DETECT state is sent to the DUT during Transmit Disable, acknowledge detect can be set to true. However, once break_link_timer is finished, the DUT will enter the ABILITY DETECT state where acknowledge detect is reset to false. Thus, the DUT will need to get another ability match once it enters the ABILITY DETECT state.

Test Setup: Using a Cat 5 cord, connect the DUT's transmitter to the Line Monitor. Terminate the DUT's transmit channel with a 100Ω line termination. Using a Cat 5 cord, connect the DUT's receiver to the Traffic Generator using a 100Ω line termination.

Procedure:

1. Establish a connection (not a link) to the DUT
2. Use the Traffic Generator to send a series of 4 FLPs designed to cause the DUT to enter the ACKNOWLEDGE DETECT state (determined in test #28.2.1)
3. Once the DUT halts its FLP transmission, send the same sequence of FLPs at periodic intervals less than break_link_timer
4. Monitor the DUT's FLP transmission during this process

Observable Results:

- The DUT should resume FLP transmission after break_link_timer is finished, regardless of the received FLPs during the time where the DUT was in the TRANSMIT DISABLE state

Possible Problems: None

GROUP 3: PARALLEL DETECTION

Scope: The following tests cover Auto-Negotiation operation specific to the Parallel Detection mechanism.

Overview: These tests are designed to verify that an auto-negotiating device can properly detect a legacy (non-auto-negotiating) fixed speed device.

Test #28.3.1: Single Link Ready

Purpose: To verify that the device under test properly monitors the status of single_link_ready during parallel detection.

References:

[1] IEEE Std 802.3, 1998 Edition: Section 28.3, Figures 28-16 & 28-17

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: July 28, 1999

Discussion: When a device implementing a 10Base-T PMA begins to receive link test pulses it must indicate link_status[NLP]=READY after 'lc_max' number of pulses have been received. According to Figure 28-16, once link_status[NLP]=READY is indicated, the device should cease transmitting FLPs and start autoneg_wait_timer. Single_link_ready is then used to indicate if exactly one PMA is currently ready. If no link is ready or if more than a single link is simultaneously ready then single_link_ready=false, mr_parallel_detection_fault=true, and FLP transmission should resume "immediately". This test is designed to verify that the process described above functions appropriately.

Test Setup: Using a Cat 5 cord, connect the DUT's transmitter to the Line Monitor. Terminate the DUT's transmit channel with a 100Ω line termination. Using a Cat 5 cord, connect the DUT's receiver to the Traffic Generator using a 100Ω line termination.

Procedure:

1. Establish a connection (not a link) to the DUT
2. Use a Traffic Generator to send the DUT 'lc_max' pulses spaced at 16ms.
3. Determine the duration for which the DUT has ceased transmitting FLPs

Observable Results:

- The DUT should cease FLP transmission for approximately link_loss_timer

Possible Problems: None

Test #28.3.2: Range of Auto-Negotiation Wait Timer

Purpose: To verify that the implemented value of autoneg_wait_timer is within the specified range of 500 to 1000ms.

References:

[1] IEEE Std 802.3, 1998 Edition: Section 28.3.2, Figure 28-16 Arbitration state diagram

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: July 28, 1999

Discussion: In order for an Auto-Negotiation able device to properly parallel detect a link partner, it must receive a valid single_link_ready=true signal from its link partner for a period of time before it negotiates to that link. This time is defined by the device's "autoneg_wait_timer," and is specified to be between 500 and 1000 ms. This test is designed to verify that the device under test does not parallel detect to a link before waiting a time within this range. This timer cannot be measured precisely from the RJ-45 interface; however, it can be bounded. The upper bound can be established by causing a single link to be ready and observing the gap between cessation of FLPs and commencement of the link pulses/stream. This delay includes any inter-FLP gap that the device may be in the midst of when detection of single_link_ready occurs. Additionally, any delay from the proper link being enabled to actual signaling appearing on the line will add to the value of the observed gap. The lower bound may be established for devices implementing a 10Base-T PMA by first determining the implemented values of lc_max and link_loss_timer. With these values known, the DUT can be sent a burst of link test pulses corresponding to lc_max plus the duration of autoneg_wait_timer found for the upper bound. The number of pulses in the burst may then be decreased until the DUT is observed to source FLPs following reception of the pulses, instead of NLPs (10Base-T link). This transition identifies the range of the lower bound. This range should be autoneg_wait_timer minus the time required to detect single_link_ready=false.

Test Setup: Using a Cat 5 cord, connect the DUT's transmitter to the Line Monitor. Terminate the DUT's transmit channel with a 100Ω line termination. Using a Cat 5 cord, connect the DUT's receiver to the Traffic Generator using a 100Ω line termination.

Procedure:

1. Establish a connection (not a link) to the DUT
2. Use a Traffic Generator to send the station valid NLPs continuously with valid spacing
3. Monitor the DUT's transmit line
4. Verify that the DUT establishes a 10Base-T link

5. Measure the time between when the DUT ceased transmission of FLPs and when the DUT began transmitting NLPs. The minimum of these observations is the upper bound of autoneg_wait_timer
6. Break link, and calculate the number of NLPs to send to satisfy: X*NLP_gap = 'upper bound of autoneg_wait_timer'.
7. Send X + lc_max NLPs at a gap of 'NLP_gap' to the DUT.
8. Repeat step 7, decreasing X until the DUT sources FLPs following cessation of the NLPs from the Traffic Generator. (the gap should be approximately link_loss_timer)

Observable Results:

- The DUT's autoneg_wait_timer should be in the range of 500 to 1000 ms

Possible Problems:

- If only the upper or lower bound lays outside the conformance window, then the autoneg_wait_timer cannot be found conformant or non-conformant.

GROUP 4: 10BASE-T RELATED TESTS

Scope: The following tests cover 10BASE-T operation specific to the NLP Receive Link Integrity Test state diagram.

Overview: These tests are designed to verify the operation of the NLP Receive Link Integrity Test state diagram for 10BASE-T devices. This state machine was introduced in clause 28 replacing the previously defined Link Integrity Test Function state Diagram of Figure 14-6 in clause 14 of IEEE 802.3. The primary motivation for this change was to prevent an Auto-Negotiation capable 10BASE-T device from detecting a link when non-10BASE-T frames (such as 100BASE-TX idle) was received.

NOTE: THESE TESTS CANNOT BE PERFORMED IF THE DUT DOES NOT SUPPORT A 10BASE-T PMA.

Test #28.4.1: Link Count Max

Purpose: To verify that the device under test implements lc_max within 2 to 10 link test pulses.

References:

[1] IEEE Std 802., 1998 Edition: Sections 14.2.3.1 Figure 14-12, 28.3 Figures 28-16 & 28-17

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: July 28, 1999

Discussion: When a device implementing a 10Base-T PMA begins to receive link test pulses conformant to Figure 14-12, it must indicate link_status[NLP]=READY after 'lc_max' number of pulses have been received. According to Figure 28-16, once link_status[NLP]=READY is indicated, the device should cease transmitting FLPs. To prevent a device from indicating link off a received FLP, the state machine depicted in Figure 28-17 resets if a pulse is received before the link_test_min_timer has expired. This test is designed to verify that the implemented value of lc_max is between 2 and 10 pulses (inclusive).

Test Setup: Using a Cat 5 cord, connect the DUT's transmitter to the Line Monitor. Terminate the DUT's transmit channel with a 100Ω line termination. Using a Cat 5 cord, connect the DUT's receiver to the Traffic Generator using a 100Ω line termination.

Procedure:

1. Establish a connection (not a link) to the DUT
2. Use a Traffic Generator to send the DUT 2 pulses spaced at 16ms.
3. Determine whether the DUT has ceased transmitting FLPs
4. If the DUT did not cease FLP transmission, repeat steps 1 through 3 varying the number of pulses sent until the DUT ceases FLP transmission.

Observable Results:

- The DUT should cease FLP transmission for approximately link_loss_timer after receiving between 2 to 10 link test pulses

Possible Problems: None

Test #28.4.2: Range of Link Test Timers

Purpose: To verify that the device under test accepts NLPs (link test pulses) with proper spacing, and refuses those with spacing outside of the acceptable range.

References:

[1] ANSI/IEEE Std 802.3, 1998 Edition: Sections 14.2.1.7, 28.3, Figure 28-17, Arbitration state diagram

Resource Requirements

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: January 13, 2000

Discussion: The acceptable gap between NLPs (10Base-T link test pulses) is defined to be between "link_test_min_timer" and "link_test_max_timer". The value for "link_test_min_timer" must be between 2 and 7 ms. The value for "link_test_max_timer" must be between 25 and 150 ms. This test is designed to verify that a device implementing a 10Base-T PMA will establish a 10Base-T link upon receipt of NLPs with valid spacing, and refuses link with spacing outside of these ranges.

Test Setup: Using a Cat 5 cord, connect the DUT's transmitter to the Line Monitor. Terminate the DUT's transmit channel with a 100Ω line termination. Using a Cat 5 cord, connect the DUT's receiver to the Traffic Generator using a 100Ω line termination.

Procedure:

Part A: link_test_min_timer

1. Establish a connection (not a link) to the DUT
2. Use a Traffic Generator to send the DUT lc_max link pulses spaced at 7ms apart to cause it to enter the LINK STATUS CHECK state
3. Determine whether the DUT entered the LINK STATUS CHECK state by monitoring the DUT for any delay in FLP transmission
4. Repeat steps 1 through 3 varying the spacing of the link pulses until the DUT fails to enter the Parallel Detect State

Part B: link_test_max_timer

5. Repeat steps 1 through 3 varying the spacing of the link pulses from 25ms and higher

Part C:

6. Repeat steps 1-3 sending link pulses continuously and spaced closer together than the determined link_test_min_timer

Observable Results:

a) The link_test_min_timer should lay between 2ms and 7ms
b) The link_test_max_timer should lay between 25ms and 150ms
c) The device should never enter the LINK STATUS CHECK state

Possible Problems: None

Test #28.4.3: Range of Link Loss Timer

Purpose: To verify that the device under test implements link_loss_timer within 50ms and 150ms.

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 14.2.1.7, 28.3, Figures 28-16 & 28-17

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: July 28, 1999

Discussion: Once a 10Base-T link has been detected, the link should not fail unless frames or link test pulses are not received for a period of time governed by the link_loss_timer.

Test Setup: Using a Cat 5 cord, connect the DUT's transmitter to the Line Monitor. Terminate the DUT's transmit channel with a 100Ω line termination. Using a Cat 5 cord, connect the DUT's receiver to the Traffic Generator using a 100Ω line termination.

Procedure:

1. Establish a connection (not a link) to the DUT
2. Use a Traffic Generator to send the DUT a sufficient number of link pulses to cause the device to enter the FLP LINK GOOD state. Once the link is up, halt for 150ms after the last link pulse
3. Determine whether the DUT has broken link
4. Repeat steps 1 through 3 varying the gap until the DUT always keeps a good link.

Observable Results:

- The DUT should keep link with a gap within 50ms and 150ms

Possible Problems: None

Test #28.4.4: Link Integrity and RD Active

Purpose: To verify that the device under test maintains 10Base-T link upon reception of valid 10Base-T frames.

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 14.2.3.1, 14.3.1.3.2 Figures 14-16, 14-17, 28.3, Figure 28-17

Resource Requirements

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: July 28, 1999

Discussion: Auto-Negotiating devices implementing a 10Base-T PMA must support Figure 28-17 "NLP Receive Link Integrity Test state diagram", unlike legacy 10Base-T implementation which follow Figure 14-6 "Link Integrity Test Function state diagram". The significant difference between these figures is that link may not be established based on the reception of 10Base-T frames (indicated as RD=active). However, once a 10Base-T link is ready, reception of either link test pulses or 10Base-T frames may maintain the link. However, as indicated in section 14.3.1.3.2, reception of signaling not meeting the requirements of Figures, 14-16, or 14-17 should not be accepted as RD=active. This includes 100Base-TX signaling.

Test Setup: Using a Cat 5 cord, connect the DUT's transmitter to the Line Monitor. Terminate the DUT's transmit channel with a 100Ω line termination. Using a Cat 5 cord, connect the DUT's receiver to the Traffic Generator using a 100Ω line termination.

Procedure:

Part A: Link maintenance via RD=active

1. Establish a connection (not a link) to the DUT
2. Use a Traffic Generator to send the DUT 'lc_max' link pulses spaced at 16ms followed by validly formed 10Base-T frames spaced at 16ms
3. Determine whether the DUT entered into a good link by determining if it is sending NLPs. Also, if the means exists, determine if the DUT received the frames after link_control[NLP]=ENABLE occurs.

Part B: Refusal of link based on RD=active

4. Establish a connection (not a link) to the DUT
5. Use a Traffic Generator to send the DUT validly formed 10Base-T frames spaced at 16ms for a duration exceeding autoneg_wait_timer
6. Determine whether the DUT entered into a good link by determining if it is sending NLPs. Also, if the means exists, determine if the DUT received any of the frames

Part C: Refusal of link maintenance upon reception of 100Base-TX signaling

7. Establish a connection (not a link) to the DUT
8. Use a Traffic Generator to send the DUT 'lc_max' link pulses spaced at 16ms, then 100Base-TX signaling for several seconds, followed by validly formed 10Base-T frames spaced at 16ms
9. Determine whether the DUT remains in a 10Base-T link by monitoring if it is sending out NLPs throughout the process. Also, if the means exists, determine if the DUT received any of the frames

Observable Results:

a) Once the device enters the FLP LINK GOOD state, the DUT should be sending out NLPs and receiving the frames
b) The DUT should never establish a link, and thus, never send out NLPs and never receive the frames
c) The DUT should exit break its 10Base-T link and parallel detect to 100Base-TX upon reception of the 100Base-TX idle. Once it is switched back to the 10Base-T frames, the 100Base-TX link should be broken and no link should be formed by the detection of the frames. Also, none of the frames sent after the 100Base-TX idle should be received

Possible Problems: None

GROUP 5: NEXT PAGE EXCHANGE

Scope: The following tests cover Auto-Negotiation operation specific to the Next Page exchange process.

Overview: These tests are designed to verify that the device under test properly implements the media independent interface (MII) register set as it pertains to the Auto-Negotiation function. Register functions explored are defined in Clause 22 (MII), Clause 28 (Auto-Negotiation) and Clause 40 (1000BASE-T) of IEEE 802.3 and 802.3ab. Many of these tests are aimed at verifying the critical link between a conformant Auto-Negotiation state machine implementation and the overall system's management and control software.

NOTE: THESE TESTS CANNOT BE PERFORMED IF THE DUT DOES NOT SUPPORT A NEXT PAGE EXCHANGE OR ALLOW A NEXT PAGE EXCHANGE TO BE INITIATED.

Test #28.5.1: Next Page Exchange Restart

Purpose: To verify that the device under test enters the TRANSMIT DISABLE state from the NEXT PAGE WAIT state if flp_receive_idle becomes true.

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 28.3.1, Figure 28-16 Arbitration state diagram

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: July 28, 1999

Discussion: Once the Next Page exchange process has begun, if a device's link partner for some reason stops sending Next Pages, the device should cease transmission as well. When in the NEXT PAGE WAIT state, if a device detects flp_receive_idle=true, then it should immediately transition to the TRANSMIT DISABLE state. This test is designed to verify that the device under test exits the Next Page exchange process if flp_receive_idle becomes true.

Test Setup: Using a Cat 5 cord, connect the DUT's transmitter to the Line Monitor. Terminate the DUT's transmit channel with a 100Ω line termination. Using a Cat 5 cord, connect the DUT's receiver to the Traffic Generator using a 100Ω line termination.

Procedure:

1. Establish a connection (not a link) to the DUT
2. Use the Traffic Generator to send the DUT enough FLPs to put it through the COMPLETE ACKNOWLEDGE state (see test #28.2.2)
3. Send the DUT a message page with the NP bit set to 1 (going through the COMPLETE ACKNOWLEDGE state), then cease transmission of Next Pages
4. Verify that the DUT enters the TRANSMIT DISABLE state

Observable Results:

- After the expiration of nlp_max_timer, the device should enter the TRANSMIT DISABLE state and cease transmission of Next Pages

Possible Problems: If the DUT does not support a Next Page exchange, then this test cannot be performed.

Test #28.5.2: Next Page Consistency Match

Purpose: To verify that the device under test still performs a consistency match test on received Next Pages.

References:

[1] IEEE Std 802.3, 1998 Edition: Section 28.3.1

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: July 28, 1999

Discussion: This test is virtually identical to test #28.2.3, but is repeated here to verify that the consistency match test is carried through to the Next Page exchange process and is performed on Next Pages. See test #28.2.3 for full details.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Establish a connection (not a link) to the DUT
2. Use the Traffic Generator to send the DUT enough FLPs to get it through the COMPLETE ACKNOWLEDGE state (see test #28.2.2)
3. Send a series of message pages- first some with the Acknowledge bit not set (enough to put the DUT into the ACKNOWLEDGE DETECT state- refer to results of test #28.2.1) followed by 3 with the Acknowledge bit set to logic one and bit D10 holding the opposite value as the initial 4 message pages
4. Monitor the transmit line coming from the DUT

Observable Results:

- The DUT should cease transmitting Next Pages immediately once the inconsistent message pages are received

Possible Problems: If the DUT does not support a Next Page exchange, then this test cannot be performed.

Test #28.5.3: Reception of Toggle Bit

Purpose: To verify that the device under test checks the value of the Toggle Bit when transitioning from NEXT PAGE WAIT to ACKNOWLEDGE DETECT to see if the received Next Pages correctly alternate the value of the Toggle Bit.

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 28.2.1.2, 28.2.3.4, 28.2.3.4.1, 28.2.3.4.6

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: July 28, 1999

Discussion: During Next Page exchange, the toggle bit (bit D11) of the received Next Pages serves a simple purpose. The value of this bit alternates between 0 and 1 in consecutive pages, and therefore provides the receiving station with a quick and easy check to verify that it is receiving Next Pages in the proper order. If a device receives consecutive pages without the toggle bit toggled, it should sit in the NEXT PAGE WAIT state until it receives a Next Page with the proper toggle bit value. This test is designed to verify that the device under test makes sure that its received Next Pages are toggled properly.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Establish a connection (not a link) to the DUT
2. Use the Traffic Generator to send enough FLPs to put the DUT through the COMPLETE ACKNOWLEDGE state (see test #28.2.2)
3. Send the DUT enough Next Pages to allow it to send all of its message and unformatted pages with the following modification: reverse the values of the toggle bit of the last 2 pages (by doing this, you end up with toggle values of either 0 0 1 or 1 1 0 for the last 3 pages)
4. Monitor the transmission from the DUT.

Observable Results:

- The DUT should not leave the NEXT PAGE WAIT state on reception of the second to last page, but should accept the last page and conclude the Next Page exchange

Possible Problems: If the DUT does not support a Next Page exchange, then this test cannot be performed.

Test #28.5.4 Transmitted Toggle Bit Value

Purpose: To verify that the device under test properly alternates values of 0 and 1 in the toggle bit position (bit D11) of its Next Pages.

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 28.2.1.2, 28.2.3.4, 28.2.3.4.1, 28.2.3.4.6

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: July 28, 1999

Discussion: During Next Page exchange, the toggle bit (bit D11) of the transmitted Next Pages serves a simple purpose. The value of this bit alternates between 0 and 1 in consecutive pages, and therefore provides the receiving station with a quick and easy check to verify that it is receiving Next Pages in the proper order. Therefore, it is important that the DUT sets these bits properly, starting with its first Next Page, whose toggle bit value takes the opposite value of bit D11 in the device's Link Code Word. This test is designed to verify that the device under test sets the toggle bit properly throughout the exchange of Next Pages.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Use the Traffic Generator to send enough FLPs to put the DUT through the COMPLETE ACKNOWLEDGE state (see test #28.2.2)
2. Send the DUT enough Next Pages to allow it to send all of its message and unformatted pages.
3. Monitor the transmitted Next Pages
4. Verify that the DUT sets the toggle bit properly in all of its Next Pages

Observable Results:

- The value of the toggle bit in the first Next Page should have the opposite value of bit D11 in the DUT's Link Code Word
- The value of the toggle bit of the Next Page transmitted by the DUT's should always take the opposite value of the toggle bit of the previous Next Page (if the previous value was a 0, it should be a 1, and vice versa)

Possible Problems: If the DUT does not support a Next Page exchange, then this test cannot be performed.

Test #28.5.5: Reception of rx_link_code_word[NP]=0

Purpose: To verify that the DUT will properly complete a Next Page exchange when rx_link_code_cord[NP]=0 while tx_link_code_word[NP]=0 in the ACKNOWLEDGE DETECT state.

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 28.3.1, 28.3.4, Figure 28-16

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: August 4, 1999

Discussion: When a device has finished transmitting Next Pages, and its link partner still has more Next Pages to send, the device should set its Next Page bit to zero and transmit null message pages. Once the device receives the last Next Page from its link partner, which will have the Next Page bit set to zero, the two devices can exit COMPLETE ACKNOWLEDGE and enter FLP LINK GOOD CHECK. It is possible that a device that has its Next Page bit set to zero, while in COMPLETE ACKNOWLEDGE, will begin to receive a page from its link partner with the Next Page bit also set to zero. Once the device has sent its remaining abilities with the acknowledge bit set, ack_finished=true, tx_link_code_word[NP]=0, and rx_link_code_word[NP]=0. This could possibly cause a premature transition to FLP LINK GOOD CHECK. The link partner would still have its last Next Page to send, and the device would have ended the Next Page exchange to attempt to establish a link. A device should not act on reception of rx_link_code_word[NP]=0 until the NEXT PAGE WAIT state has been entered. Only if a page received here has the Next Page bit set to zero should the DUT then transition to FLP LINK GOOD CHECK after exiting COMPLETE ACKNOWLEDGE.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Establish a connection (not a link) to the DUT
2. Send a series of FLPs to the DUT such that the DUT proceeds to transmit all of its Next Pages, and sets its Next Page bit to zero
3. Send a null message page with the Next Page bit set to one enough times to put the DUT in COMPLETE ACKNOWLEDGE
4. Before the DUT exits COMPLETE ACKNOWLEDGE, send the DUT a null message page with the Next Page bit set to zero

5. Observe transmissions from the DUT

Observable Results:

- The DUT should not enter FLP LINK GOOD CHECK

Possible Problems: If the DUT does not support a Next Page exchange, then this test cannot be performed.

GROUP 6: MANAGEMENT REGISTERS

Scope: The following tests cover Auto-Negotiation operation specific to the management register set.

Overview: These tests are designed to verify that the device under test properly implements the media independent interface (MII) register set as it pertains to the Auto-Negotiation function. Register functions explored are defined in Clause 22 (MII), Clause 28 (Auto-Negotiation) and Clause 40 (1000BASE-T) of IEEE 802.3 and 802.3ab. Many of these tests are aimed at verifying the critical link between a conformant Auto-Negotiation state machine implementation and the overall system's management and control software.

NOTE: THESE TESTS CANNOT BE PERFORMED IF REGISTER ACCESS IS NOT PROVIDED.

Test #28.6.1: AN Advertisement Register

Purpose: To verify that the Auto-Negotiation advertisement register (Register 4) is reflected in the Link Code Words transmitted by the DUT.

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 28.2.4.1.3, Table 28-2, Annex 28A, Annex 28B, Annex 28D, 40.5.1.1 Table 40-3

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.

Last Modification: July 28, 1999

Discussion: For a device to advertise abilities that it possesses, it must be able to configure the abilities advertised during the Auto-Negotiation process so that they match the device's true capabilities. Register 4 of the MII is defined to contain these abilities, however, if the device does not use a MII then the logical equivalent must be provided.

Advertisement register bit definitions

Bit(s)	Name	Description	R/W
4.15	Next Page	See 28.2.1.2	R/W
4.14	Reserved	Write as 0	RO
4.13	Remote Fault	See 28.2.1.2	R/W
4.12:5	Technology Ability Field	See 28.2.1.2	R/W
4.4:0	Selector Field	See 28.2.1.2	R/W

Test Setup: Using a Cat 5 cord, connect the DUT's transmitter to the Line Monitor. Terminate the DUT's transmit channel with a 100Ω line termination. Using a Cat 5 cord, connect the DUT's receiver to the Traffic Generator using a 100Ω line termination.

Procedure:

1. Via management, access Register 4 and write the value 8001h
2. Observe transmission from the DUT
3. Repeat steps 1-3 with other test values including (but not limited to) E001h, 0000h, and FFFFh

Observable Results:

a) The Link Code Words transmitted by the DUT should contain the bit values 4.15, and 4.13-4.0 that were written to Register 4.
b) The Link Code Words transmitted by the DUT should contain the bit value of zero for 4.14.

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #28.6.2: AN Link Partner Ability Register

Purpose: To verify that the Auto-Negotiation link partner ability register is set according to Table 28-8 based upon the reception of Link Code Words by the DUT.

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 28.2.4.1.4, Table 28-3, Annex 28A, Annex 28D

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: July 28, 1999

Discussion: For a device to resolve a proper link configuration, it must accurately receive its partner's abilities and relate them to management. Register 5 of the MII is defined to contain these abilities, if the DUT does not use a MII then the logical equivalent must be provided.

Link Partner ability register bit definitions

Bit(s)	Name	Description	R/W
5.15	Next Page	See 28.2.1.2	RO
5.14	Acknowledge	See 28.2.1.2	RO
5.13	Remote Fault	See 28.2.1.2	RO
5.12:5	Technology Ability Field	See 28.2.1.2	RO
5.4:0	Selector Field	See 28.2.1.2	RO

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Send the DUT Link Code Words containing the value 8001h
2. Access and read Register 5.
3. Repeat steps 1-2 by sending values including (but not limited to) FFFFh, 0000h
4. Attempt to write FFFFh to Register 5, the read the contents of Register 5.

Observable Results:

a) The bits of the Link Code Word received by the DUT should be contained in Register 5 exactly as they were received.
b) The DUT should not allow any of the bits of Register 5 to be written.

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #28.6.3: Main Reset

Purpose: To verify that bit 0.15 controls the resetting of the PHY and Auto-Negotiation process.

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 22.2.4.1, Table 22-7, 22.2.4.1, 28.2.4.1.7, Table 28-7, 28.3.1, 28.3.4, Figure 28-16

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: July 28, 1999

Discussion: Bit 0.15 of the control register gives management the ability to reset all of the control and status registers, as well as restarting the Auto-Negotiation process.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Wait until the DUT has begun to transmit FLPs
2. Set bit 0.15 in the control register
3. Observe transmissions from the DUT

Observable Results:

- The DUT should stop Auto-Negotiation, wait break_link_timer, and then restart Auto-Negotiation by sending FLPs.

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #28.6.4: Auto-Negotiation Enable

Purpose: To verify that bit 0.12 controls the enabling/disabling of the Auto-Negotiation process.

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 22.2.4.1, Table 22-7, 22.2.4.1.4, 28.3.1, 28.2.4.1.7, Table 28-7, 28.3.4, Table 28-16

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: July 28, 1999

Discussion: Management has the ability to enable Auto-Negotiation by setting bit 0.12 to one and to disable Auto-Negotiation by setting bit 0.12 to zero. If the management has set bit 0.12 to zero, then the DUT should never source FLPs, and a link will be established using bits 0.13 and 0.6 (speed selection), and bit 0.8 (duplex mode) of the control register. When bit 0.12 is set to one, the DUT should transmit FLPs and establish a link using the Auto-Negotiation process.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination

Procedure:

1. Write a value of one to bit 0.12
2. Observe transmissions from the DUT
3. Repeat steps 1 and 2, writing a value of zero to bit 0.12
4. Repeat steps 1 and 2, writing a value of one to bit 0.12

Observable Results:

a) The DUT should commence Auto-Negotiation and transmit FLPs after step 1.
b) The DUT should cease Auto-Negotiation, wait break_link_timer, and then proceed to transmit valid link signaling (based on bits 0.6 and 0.13) after step 3.
c) The DUT should cease idle transmission, wait break_link_timer, and then transmit FLPs after step 4.

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #28.6.5: Auto-Negotiation Restart

Purpose: To verify that bit 0.9 controls the restarting of Auto-Negotiation.

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 22.2.4.1.7 28.2.4.1.7, Table 28-7, 28.3.1, 28.3.4, Figure 28-16

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: July 28, 1999

Discussion: The MII Control Register provides a means for management to restart Auto-Negotiation by writing a value of one to bit 0.9 of the register. This is a way to restart Auto-Negotiation without resetting the entire PHY.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Send a series of FLPs to the DUT encoded with 8001h
2. While the DUT is sending FLPs, write a value of one to bit 0.9
3. Observe transmissions from the DUT

Observable Results:

- The DUT should cease transmission, wait break_link_timer, and then start to transmit FLPs

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #28.6.6: Auto-Negotiation Complete

Purpose: To verify that bit 1.5 is properly set upon completion of Auto-Negotiation and entrance into the FLP LINK GOOD state.

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 22.2.4.2, Table 22-8, 22.2.4.2.10, 28.2.4.1.7, Table 28-7, 28.3.1, 28.3.4, Table 28-16

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: July 28, 1999

Discussion: Once a link has been established, management needs to be made aware that frame transmission and reception can commence. Bit 1.5 is set when Auto-Negotiation is complete and a link has come up.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Use the Traffic Generator to send enough FLPs to put the DUT through the COMPLETE ACKNOWLEDGE state.
2. Observe the status of bit 1.5
3. Use the Traffic Generator to send enough FLPs to put the DUT through the COMPLETE ACKNOWLEDGE state followed by valid link signaling in order to establish a link
4. Observe the status of bit 1.5

Observable Results:

- The DUT should not set bit 1.5 until it has entered the FLP LINK GOOD state. Thus in step 2 bit 1.5 should be 0, and in step 4 bit 1.5 should be 1.

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #28.6.7: Link Status

Purpose: To verify that bit 1.2 of the status register is set when a valid link has been established and is not set if a valid link has not been established.

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 22.2.4.2, Table 22-8, 22.2.4.2.13, 28.2.6.1.1,

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: July 28, 1999

Discussion: Management is made aware that a valid link has been established by bit 1.2 of the MII Status Register. When this bit is set, it means that the DUT has entered the FLP LINK GOOD state, regardless of whether or not Auto-Negotiation is enabled or disabled.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Send the DUT a series of FLPs and link signaling such that a link will be established
2. Monitor the status of bit 1.2
3. Turn off Auto-Negotiation (if possible)
4. Send the DUT an Idle pattern to manually force a link
5. Monitor the status of bit 1.2

Observable Results:

- The DUT should not set bit 1.2 until the FLP LINK GOOD state has been entered, regardless of whether or not Auto-Negotiation has been used to established a link.

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #28.6.8 Remote Fault

Purpose: To verify that the DUT sets bit 1.4 upon reception of a Link Code Word with the remote fault bit set.

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 28.2.3.5

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: July 28, 1999

Discussion: A device which supports the Remote Fault function must indicate the reception of a base page with the RF bit set by setting bit 1.4 in the MII Status Register. In this way, management is made aware of a remote fault indication from the link partner. After management reads the status register, bit 1.4 should reset to zero. If the DUT does not support the Remote Fault function, no action is necessary.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Read the MII Status Register (Register 1) twice.
2. Use the Traffic Generator to send enough FLPs with the RF bit set to put the DUT through the COMPLETE ACKNOWLEDGE state.
3. Read the MII Status Register (Register 1).
4. Read the MII Status Register again.

Observable Results:

a) In step 3, bit 1.4 may be set.
b) If bit 1.4 was set in step 3, it must be cleared in step 4.

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #28.6.9 Auto-Negotiation Ability

Purpose: To verify that the DUT keeps bit 1.3 set.

References:

[1] IEEE Std 802.3, 1998 Edition: Section 22.2.4.2.12

Resource Requirements:

- None

Last Modification: November 4, 1999

Discussion: Management is made aware that an Auto-Negotiation capable PHY is attached via the status register bit 1.3 "Auto-Negotiation Ability". Thus, management is made aware of the PHYs capability, regardless of the management's desire to enable or disable Auto-Negotiation. While this bit may appear unnecessary in most static implementations, it allows for a DUT with an exposed MII interface to discover the Auto-Negotiation capability of an attached PHY.

Test Setup: Access the DUT's Management Registers.

Procedure:

1. Disable Auto-Negotiation (set bit 0.12 to zero).
2. Read the DUT's Status Register, bit 1.3
3. Enable Auto-Negotiation (set bit 0.12 to one).
4. Read the DUT's Status Register, bit 1.3

Observable Results:

- Bit 1.3 must be set, regardless of whether Auto-Negotiation is enabled or not.

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #28.6.10 Report PHY Capabilities

Purpose: To verify that the PHY set bits 1.15:8 and 15.15:12 appropriately for the PHY's capabilities.

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 22.2.4.2 and 22.2.4.4, Tables 22-8 and 22-9.

Resource Requirements:

- None

Last Modification: January 13, 2000

Discussion: Management is made aware that a PHY's signaling capabilities via the status register bits 1.15:9. If bit 1.8 is set, then the PHY has additional capabilities specified in the Extended Status Register (Register 15) bits 15.15:12. Thus, management is made aware of the PHYs capability, regardless of the management's desire to enable or disable that technology. While these bits may appear unnecessary in most static implementations, it allows for a DUT with an exposed MII/GMII interface to discover the Auto-Negotiation capability of an attached PHY. (Note, an exposed GMII interface is not specified by 802.3)

Status Register technology capability bit definitions

Bit(s)	Name	Description	R/W
1.15	100BASE-T4	1=PHY able to perform 100BASE-T4	RO
1.14	100BASE-X Full Duplex	1=PHY able to perform 100BASE-X FD	RO
1.13	100BASE-X Half Duplex	1=PHY able to perform 100BASE-X HD	RO
1.12	10BASE-T Full Duplex	1=PHY able to perform 10BASE-T FD	RO
1.11	10BASE-T Half Duplex	1=PHY able to perform 10BASE-T HD	RO
1.10	100BASE-T2 Full Duplex	1=PHY able to perform 100BASE-T2 FD	RO
1.9	100BASE-T2 Half Duplex	1=PHY able to perform 100BASE-T2 HD	RO
1.8	Extended Status	1=Extended statys info in Register 15	RO
15.15	1000BASE-X Full Duplex	1=PHY able to perform 1000BASE-X FD	RO
15.14	1000BASE-X Half Duplex	1=PHY able to perform 1000BASE-X HD	RO
15.13	1000BASE-T Full Duplex	1=PHY able to perform 1000BASE-T FD	RO
15.12	1000BASE-T Half Duplex	1=PHY able to perform 1000BASE-T HD	RO

Test Setup: Access the DUT's Management Registers.

Procedure:

1. Read bits 1.15:8 and 15.15:12.

Observable Results:

- Bits 1.15:9 and 15.15:12 must be set appropriately. Bit 1.8 must be set if Register 15 is non 0.

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #28.6.11 Parallel Detection Fault

Purpose: To verify that the DUT sets bit 6.4 upon reception of a parallel indication fault.

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 28.2.4.1.5 Table 28-5, 28.2.4.1.7 Table 28-7, 28.3.4 Figure 28-16

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: August 31, 1999

Discussion: Management is made aware that a parallel detection fault has occurred by reading bit 6.4 of the Auto-Negotiation expansion register. Upon receiving such a fault, the DUT must set this bit. I value of 1 means that a fault has been detected via the parallel detection function, while a value of 0 indicates that a fault has not been detected via the parallel detection function. A parallel detection fault occurs if zero or more than one PMA is indicated to have link_status=READY when the autoneg_wait_timer expires during the parallel detection process. The parallel detection fault bit should be reset upon a read to the Auto-Negotiation expansion register.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Send the DUT valid link signaling for <500ms such that the DUT stops sending FLPs. (This may be lc_max NLPs, 100BASE-TX Idle, or 100BASE-T4 link test pulses)
2. Read the Auto-Negotiation Expansion Register (Register 6) twice.

Observable Results:

- Bit 6.4 should be set to one the first time the Auto-Negotiation expansion register is read, and set to zero the second time the register is read.

Possible Problems: If management access is not provided, then this test cannot be performed. If the DUT does not support 10BASE-T, 100BASE-TX or 100BASE-T4 then this test cannot be performed.

Test #28.6.12: Page Received Setting/Resetting

Purpose: To verify that mr_page_rx is set when a new page is received and cleared when the Auto-Negotiation expansion register is read.

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 28.2.4.1.5, Table 28-5, 28.2.4.1.7, Table 28-7, 28.3.1, 28.3.4, Figure 28-16

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: November 3, 1999

Discussion: Management is made aware of the reception of a new page by reading bit 6.1 in the Auto-Negotiation expansion register. If bit 6.1 is set, then management can look at the contents of the received page and act accordingly. Upon reading of this register, this bit is cleared so that management may not read the register again and think that the same page is a new page.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. If the DUT supports Next Page exchange, set the NP bit in the DUT's base page (bit 4.15)
2. Send the DUT a constant stream of FLPs encoded with 8001h
3. Read bit 6.1 twice
4. Repeat steps 1-3 with an encoding of C001h
5. Restart Auto-Negotiation and send enough FLPs encoded with C001h to enter COMPLETE ACKNOWLEDGE followed by a constant stream of FLPs encoded with E808h to again cause the DUT to enter COMPLETE ACKNOWLEDGE.
6. Read bit 6.1 three times

Observable Results:

a) After step 2, bit 6.1 should be zero for both reads
b) After step 3, bit 6.1 should be one for the first read and zero for the second read
c) If the DUT supports Next Page exchange, after step 5, bit 6.1 should be one for the first two reads and zero for the third read

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #28.6.13 Link Partner Auto-Negotiation Able

Purpose: To verify that the DUT sets bit 6.0 upon detection of link partner which is capable of Auto-Negotiation.

References:

[1] IEEE Std 802.3, 1998 Edition: 28.2.4.1.5, 28.2.4.1.7, Table 28-7, Figure 28-16

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: November 4, 1999

Discussion: A device's management is made aware that the Link Partner is capable of Auto-Negotiation when the DUT enters the ACKNOWLEDGE DETECT state and sets mr_lp_autoneg_able to true. This in-turn sets bit 6.0 in the Expansion Register to 1. Whenever the DUT re-enters the ABILITY DETECT state, mr_lp_autoneg_able should be reset to false (6.0 set to 0).

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Send nothing to the DUT and read bit 0 of the Expansion Register (Register 6).
2. Use the Traffic Generator to send a constant stream of identical FLPs without ACK set to put the DUT in the ACKNOWLEDGE DETECT state.
3. Read bit 0 of the Expansion Register (Register 6).
4. Send nothing to the DUT and wait until the DUT re-enters the ABILITY DETECT state (and send FLPs without ACK set)
5. Read bit 0 of the Expansion Register (Register 6).
6. Use the Traffic Generator to send a constant stream of FLPs alternating in content and without ACK set, to keep the DUT in the ABILITY DETECT state.
7. Read bit 0 of the Expansion Register (Register 6).

Observable Results:

a) In step 3, bit 6.0 should be set to one.
b) In steps 1, 5 and 7 bit 6.0 should be set to zero.

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #28.6.14: AN Next Page Transmit Register

Purpose: To verify that the Auto-Negotiation Next Page transmit register, set according to Table 28-6, is properly reflected in the Next Pages transmitted by the DUT.

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 28.4.1.6, Table 28-6, 28.2.3.4

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: July 28, 1999

Discussion: During a Next Page exchange, management must have the ability to control the contents of the pages to be transmitted. MII Register 7 is used to specify these abilities, however, if the device does not use a MII then the logical equivalent must be provided. The definition of Register 7 is provided below for convenience.

Next Page transmit register bit definitions

Bit(s)	Name	Description	R/W
7.15	Next Page	See 28.2.3.4	R/W
7.14	Reserved	Write as 0	RO
7.13	Message Page	See 28.2.3.4	R/W
7.12	Acknowledge 2	See 28.2.3.4	R/W
7.11	Toggle	See 28.2.3.4	RO
7.10:0	Message/Unformatted Code Field	See 28.2.3.4	R/W

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Set the NP bit in the DUT's base page (bit 4.15)
2. Send a constant stream of FLPs to the DUT containing the abilities C1E1h
3. Via management, read Register 7 and write a value of 2008h
4. Observe transmission from the DUT
5. Repeat using values including (but not limited to) 2808h, and FFFFh

Observable Results:

a) The Next Pages transmitted by the DUT should have bits 7.15, 7.13, 7.12, and 7.10:0 set to what was written to Register 7.

b) The Next Pages transmitted by the DUT should have bit 7.14 set to zero, and bit 7.11 set to the opposite of the value of bit 4.11 in the initial Link Code Word sent by the DUT.

Possible Problems: If management access is not provided, then this test cannot be performed. If the DUT does not support a Next Page exchange, then this test cannot be performed.

Test #28.6.15: AN Link Partner Ability Next Page Register

Purpose: To verify that the Auto-Negotiation link partner ability Next Page register is set according to Table 28-8 based upon the reception of Next Pages by the DUT.

References:

[1] IEEE Std 802.3, 1998 Edition: Section 28.2.3.4
[2] IEEE Std 802.3ab, 1999 Edition: Section 28.2.4.1.7, Table 28-8

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: January 13, 2000

Discussion: For a device to resolve a proper link configuration, it must accurately receive its partner's Next Page abilities and relate them to management. Register 8 of the GMII is defined to contain these abilities, however, if the DUT does not use a GMII then the logical equivalent must be provided. The definition of Register 8 is provided below for convenience.

Link Partner Next Page Ability register bit definitions

Bit(s)	Name	Description	R/W
8.15	Next Page	See 28.2.3.4	RO
8.14	Reserved	See 28.2.3.4	RO
8.13	Message Page	See 28.2.3.4	RO
8.12	Acknowledge 2	See 28.2.3.4	RO
8.11	Toggle	See 28.2.3.4	RO
8.10:0	Message/Unformatted Code Field	See 28.2.3.4	RO

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Set the NP bit in the DUT's base page (bit 4.15)
2. Send the DUT enough FLPs with the Next Page bit set so that the DUT enters the COMPLETE ACKNOWLEDGE state, followed by a constant stream of FLPs encoded with 2008h.
3. It should be necessary to write any value (typically 2001) to register 7 to cause the DUT to enter the NEXT PAGE WAIT and thus eventually return to the COMPLETE ACKNOWLEDGE state.
4. Via management, access and read Register 8

5. Repeat using Next Pages including (but not limited to) 2808h, FFFFh and 0000h. If the toggle bit (D11) is set to a value of zero in the Next Pages (as in a next page value of 0000h), it should be set to a value of one in the base pages.
6. Write the value FFFFh to Register 8. Then read Register 8.

Observable Results:

a) The bits of the Next Pages received by the DUT should be contained in Register 8 exactly as they were received.
b) A write to Register 8 should not affect its contents.

Possible Problems: If management access is not provided, then this test cannot be performed. If the DUT does not support a Next Page exchange, then this test cannot be performed.

Test #28.6.16 mr_next_page_loaded

Purpose: To verify that mr_next_page_loaded is set upon write to the Auto-Negotiation Next Page Transmit Register, and cleared in the states NEXT PAGE WAIT and TRANSMIT DISABLE.

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 28.2.4.1.7, Table 28-7, 28.3.1, 28.3.4, Figure 28-16

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: September 7, 1999

Discussion: The mr_next_page_loaded variable is a key parameter in the transition from COMPLETE ACKNOWLEDGE to NEXT PAGE WAIT. It prevents the Auto-Negotiation protocol from proceeding until management has had time to load the AN Next Page transmit register with the Next Page to be transmitted. This occurs after the management has had time to read the previous Next Page received from its link partner (in the AN link partner ability Next Page register). mp_next_page_loaded is automatically set when management writes the AN Next Page transmit register, but should be cleared in the TRANSMIT DISABLE or NEXT PAGE WAIT states. This test observes that the proper effects of mr_np_loaded being set takes place, and that the value is reset appropriately.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Set the Next Page bit in the devices base page (write a 1 to bit 15 of MII Register 4).
2. Write '2201h' to the Next Page Transmit Register (MII Register 7).
3. Restart Auto-Negotiation (write a 1 to bit 12 of MII Register 0).
4. Use the Traffic Generator to send a constant stream of FLPs with the Next Page bit set to cause the DUT to enter the COMPLETE ACKNOWLEDGE state. The FLPs should be a repeating pattern such as 20 81E1 and 20 C1E1.
5. Observe transmissions from the DUT.
6. If the DUT properly remained in the COMPLETE ACKNOWLEDGE state while sending its base page in step 5, then write '2301h' to Register 7. Else, if the DUT remained in the COMPLETE ACKNOWLEDGE state while sending its first Next Page (2201h), then part (a) fails and then write '2301h' to Register 7 to trigger the 2nd Next Page transmission. Else stop.

7. Observe transmissions from the DUT.
8. If the DUT properly remained in the COMPLETE ACKNOWLEDGE state in step 7, then write '2401h' to Register 7.

Observable Results:

a) Resetting in TRANSMIT DISABLE state: In step 5, the DUT should remain in the COMPLETE ACKNOWLEDGE state and continue to send its base page with ACK.
b) Setting mr_next_page_loaded: In step 7, the DUT should commence transmitting the contents of register 7, with the proper toggle and ack bit values.
c) Resetting in NEXT PAGE WAIT state: In step 7, the DUT should remain in the COMPLETE ACKNOWLEDGE state and continue to send its first Next Page (2301h).

Possible Problems: If the DUT does not support Next Page exchange, then this test cannot be performed. If management access is not provided, then this test cannot be performed.

Test #28.6.17 Next Page Able

Purpose: To verify that the DUT sets bit 6.2 if it is capable of a Next Page exchange.

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 28.2.4.1.5

Resource Requirements:

- None

Last Modification: November 4, 1999

Discussion: A PHY which supports Next Page exchange must indicate this capability to management by setting bit 6.2 in the Expansion Register (Register 6), regardless of whether a Next Page exchange is desired. While this bit may appear unnecessary in most static implementations, it allows for a DUT with an exposed MII interface to discover any Next Page exchange capability of an attached PHY.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Disable Next Page advertisement (set bit 4.15 to zero).
2. Read bit 6.2 of the MII Expansion Register (Register 6).
3. Enable Next Page advertisement (set bit 4.15 to one).
4. Read bit 6.2 of the MII Expansion Register (Register 6).

Observable Results:

- Bit 6.2 must be set if the DUT supports a Next Page exchange, regardless of whether a Next Page exchange is currently desired.

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #28.6.18 Link Partner Next Page Able

Purpose: To verify that the DUT sets bit 6.3 upon reception of a base page which has bit 15 set.

References:

[1] IEEE Std 802.3, 1998 Edition: Sections 28.2.4.1.5, 28.2.4.1.7, Table 28-7, Figure 28-16

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: November 4, 1999

Discussion: A device's management is made aware that the Link Partner is capable of a Next Page exchange, and also desires a Next Page exchange when the DUT enters the COMPLETE ACKNOWLEDGE state. Upon entrance, the DUT sets mr_lp_np_able to true, this in-turn sets bit 6.3 in the Expansion Register to 1. Whenever the DUT re-enters the ABILITY DETECT state, mr_lp_np_able should be reset to false (6.3 set to 0).

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Disable Next Page advertisement (set bit 4.15 to zero).
2. Send nothing to the DUT and read bit 6.3 of the Expansion Register (Register 6).
3. Use the Traffic Generator to send a constant stream of identical FLPs with ACK and NP set to put the DUT in the COMPLETE ACKNOWLEDGE state.
4. Read bit 6.3 of the Expansion Register (Register 6).
5. The DUT should remain in the COMPLETE ACKNOWLEDGE state indefinitely. Write a 0 to bit 0.9 or 0.15 to restart Auto-Negotiation or reset the PHY.
6. Read bit 6.3 of the Expansion Register (Register 6).
7. Use the Traffic Generator to send a constant stream of identical FLPs with ACK set, and NP not set, putting the DUT in the COMPLETE ACKNOWLEDGE state.
8. Read bit 6.3 of the Expansion Register (Register 6).
9. Enable Next Page advertisement (set bit 4.15 to one) and repeat step 3 and 4.

Observable Results:

a) In step 4 and 9, bit 6.3 should be set.
b) In steps 2, 6 and 8, bit 6.3 should not be set.

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #28.6.19: 1000BASE-T MASTER/SLAVE Control Register bits 9.10:8

Purpose: To verify for 1000BASE-T devices that the MASTER/SLAVE Control Register bits 9.10:8 properly control the advertised Port type and duplex.

References:

[1] IEEE Std 802.3ab, 1999 Edition: Sections 40.5.1.1, Table 40-3, Table 40-4

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: January 13, 2000

Discussion: In order for 1000BASE-T devices to automatically configure themselves, they must complete the exchange of a base page and three Next Pages during the Auto-Negotiation process. A system's management entity could control this entire exchange by the normal writing of MII Register 4 (Base Page Advertised Ability Register) as well as MII Register 7 (Next Page Transmit Register). However, such an approach would require each systems management to be capable of properly following clause 28's Next Page exchange mechanism. To remove this burden from system implementers, many suppliers of 1000BASE-T PHYs also incorporate the option of having an automatic embedded Next Page exchange management entity control the process. To enable this, the embedded controller must be aware of the system's desired mode of operation for the 1000BASE-T port. The system accomplishes this by writing to the MASTER/SLAVE Control Register (GMII Register 9). To specify what type of device the system is (multiport or single port) as well as the desired duplex mode for the port, the system simply writes to bits 9:10-8 (see table below). Once set, the system can either enable the port, reset the port, or restart Auto-Negotiation and the embedded Next Page exchange controller will do the rest of the page exchange work. Recall that these bits are only meaningful if an embedded controller is in use. If one is not present, or disabled, then the system's management entity is required to properly complete the Next Page exchange via the properly timed writing of Register 7. In such an event, it is recommended that the contents of register 9 accurately reflect the abilities advertised in the second Next Page of the 1000BASE-T exchange.

1000BASE-T MASTER/SLAVE Control register bit definitions for ability advertisement

Bit(s)	Name	Description	Type
9.10	Port type	1=Multiport device 0=Single Port device	R/W
9.9	1000BASE-T Full Duplex	1=Advertise PHY is 1000BASE-T full duplex capable 0=Advertise PHY is not 1000BASE-T full duplex capable	R/W
9.8	1000BASE-T Half Duplex	1=Advertise PHY is 1000BASE-T half duplex capable 0=Advertise PHY is not 1000BASE-T half duplex capable	R/W

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Via management access, write to GMII Register 9 bits 10-8 (or equivalent) the value '111b'.
2. Use the Traffic Generator to send enough FLPs to put the DUT through the COMPLETE ACKNOWLEDGE state, followed by enough null pages (with proper toggle bit values) to allow the DUT to transmit all of its Next Pages
3. Monitor the Next Pages transmitted by the DUT.
4. Repeat steps 1 through 3 changing the value written to '000b'

Observable Results:

c) Bits U2 - U4 in the second Next Page (third overall page) transmitted by the DUT should match the value written in step 1, without exception.

Possible Problems: If management access to GMII Register 9 (or equivalent) is not available, then this test cannot be performed.

Test #28.6.20: 1000BASE-T MASTER/SLAVE Control Register bits 9.12:11

Purpose: To verify for 1000BASE-T devices that the MASTER/SLAVE Control Register bits 9.12:11 properly control MASTER-SLAVE Manual Configuration.

References:

[1] IEEE Std 802.3ab, 1999 Edition: Sections 40.5.1.1, Table 40-3, Table 40-4

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: January 13, 2000

Discussion: In order for 1000BASE-T devices to automatically configure themselves, they must complete the exchange of a base page and three Next Pages during the Auto-Negotiation process. A system's management entity could control this entire exchange by the normal writing of MII Register 4 (Base Page Advertised Ability Register) as well as MII Register 7 (Next Page Transmit Register). However, such an approach would require each systems management to be capable of properly following clause 28's Next Page exchange mechanism. To remove this burden from system implementers, many suppliers of 1000BASE-T PHYs also incorporate the option of having an automatic embedded Next Page exchange management entity control the process. To enable this, the embedded controller must be aware of the system's desired mode of operation for the 1000BASE-T port. The system accomplishes this by writing to the MASTER/SLAVE Control Register (GMII Register 9). To specify that the port should be forced to be either MASTER or SLAVE, the system must set bit 9.12 to 1, and set 9.11 to either 1 or 0 (see table below). Once set, the system can either enable the port, reset the port, or restart Auto-Negotiation and the embedded Next Page exchange controller will do the rest of the page exchange work. Recall that these bits are only meaningful if an embedded controller is in use. If one is not present, or disabled, then the system's management entity is required to properly complete the Next Page exchange via the properly timed writing of Register 7. In such an event, it is recommended that the contents of register 9 accurately reflect the abilities advertised in the second Next Page of the 1000BASE-T exchange.

1000BASE-T MASTER/SLAVE Control register bit definitions for MASTER-SLAVE Manual Configuration

Bit(s)	Name	Description	Type
9.12	MASTER-SLAVE Manual Config Enable	1=Enable MASTER-SLAVE Manual Configuration 0=Disable MASTER-SLAVE Manual Configuration	R/W
9.11	MASTER-SLAVE Config Value	1=Configure PHY as MASTER during MASTER-SLAVE negotiation, only when 9.12 is set to logical one. 0= Configure PHY as SLAVE during MASTER-SLAVE negotiation, only when 9.12 is set to logical one.	R/W

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Via management access, write to GMII Register 9 bits 12-11 (or equivalent) the value '11b'.
2. Use the Traffic Generator to send enough FLPs to put the DUT through the COMPLETE ACKNOWLEDGE state, followed by enough null pages (with proper toggle bit values) to allow the DUT to transmit all of its Next Pages
3. Monitor the Next Pages transmitted by the DUT.
4. Repeat steps 1 through 3 changing the value written to '00b', and '10b'.
5. Repeat steps 1 through 3 changing the value written to '01b'.

Observable Results:

a) Bits U0 & U1 in the second Next Page (third overall page) transmitted by the DUT should match the value written in step 1, except for the value written in step 5.
b) In step 5, the DUT may either set U0 to 0, and U1 to 1 (which should be ignored since U0=0) or the DUT may set both U0 and U1 to 0.

Possible Problems: If management access to GMII Register 9 (or equivalent) is not available, then this test cannot be performed.

Test #28.6.21: 1000BASE-T MASTER/SLAVE Status Register

Purpose: To verify for 1000BASE-T devices that the MASTER/SLAVE Status Register conforms to the definition in Table 40-3.

References:

[1] IEEE Std 802.3ab, 1999 Edition: Sections 40.5.1.1, Table 40-3, Table 40-4

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- 1000BASE-T Traffic Generator: A system capable of properly completing the 1000BASE-T Next Page exchange and establishing a valid 1000BASE-T link.

Last Modification: January 13, 2000

Discussion: Once a 1000BASE-T device completes Auto-Negotiation, status information specific to the 1000BASE-T link must be properly represented in the MASTER-SLAVE Status Register (GMII Register 10).

1000BASE-T MASTER/SLAVE Status Register bit definitions

Bit(s)	Name	Description	Type
10.15	MASTER-SLAVE configuration fault	1=MASTER-SLAVE configuration fault detected 0=No MASTER-SLAVE configuration fault detected	RO/LH/ SC
10.14	MASTER-SLAVE configuration resolution	1=Local PHY configuration resolved to MASTER 0=Local PHY configuration resolved to SLAVE	RO
10.13	Local Receiver Status	1=Local Receiver OK (loc_rcvr_status=OK) 0= Local Receiver not OK (loc_rcvr_status=NOT_OK)	RO
10.12	Remote Receiver Status	1=Remote Receiver OK (rem_rcvr_status=OK) 0= Remote Receiver not OK (rem_rcvr_status=NOT_OK)	RO
10.11	LP 1000T FD	1=Link Partner is capable of 1000BASE-T full duplex 0=Link Partner is not capable of 1000BASE-T full duplex	RO
10.10	LP 1000T HD	1=Link Partner is capable of 1000BASE-T half duplex 0=Link Partner is not capable of 1000BASE-T half duplex	RO
10.9:8	Reserved	Reserved	RO
10.7:0	Idle Error Count	Count of each occurrence of rxerror_status=ERROR. Cleared on read. Held at all ones in case of overflow	RO/SC

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Read GMII Register 10 (or equivalent) twice.
2. Via management access, write to GMII Register 10 (or equivalent) the value 'FFFFh'.
3. Read GMII Register 10 (or equivalent).

4. Use the 1000BASE-T Traffic Generator to complete a proper 1000BASE-T next exchange with the DUT and establish a link. Advertise 1000BASE-T Full Duplex and Half Duplex capability.
5. Read Register 10 bits 10.11 and 10.10. Repeat 4 and 5 until all four bit combinations are tested.
6. Use the 1000BASE-T Traffic Generator to complete a proper 1000BASE-T next exchange with the DUT and establish a link, such that the DUT should be MASTER. If necessary, use the line monitor to verify that the DUT should resolve to MASTER.
7. Read Register 10 bit 14.
8. Repeat step 6 and 7, changing the Next Page exchange such that the DUT should be SLAVE.
9. Configure the DUT to be manual_MASTER. Use the 1000BASE-T Traffic Generator to produce a proper 1000BASE-T next exchange with the DUT, advertising that the Traffic Generator is a manual_MASTER. This should cause the DUT to detect a configuration fault.
10. Read Register 10 bit 15, then read register 10 again.
11. Use the 1000BASE-T Traffic Generator to complete a proper 1000BASE-T next exchange with the DUT and establish a link.
12. Read Register 10 bits 10.13 and 10.12
13. With the 1000BASE-T link still established, attempt to degrade the quality of the link between the two devices by any means, but do not break the link. Either by a controlled noise injection, or an uncontrolled noise injection (such as by very briefly loosening the RJ-45 plug & jack connection.)
14. Read Register 10 bits 7:0, if non-zero, read again. Repeat 13 and 14 until a non-zero value is read.

Observable Results:

a) The value read step 3 should be identical to the final value read in step 1.
b) In step 5, the reported link partner duplex capability should match the capability indicated in the received UP1 Next Page.
c) In step 7, bit 14 should be set to one, in step 8, bit 15 should be set to 0.
d) In step 10, bit 15 should initially be set. After the second read, the bit should be cleared.
e) In step 12, bits 13 and 12 should both be set once the link is established.
f) In step 14, on the first read, following the event of errors, the counter should indicate the number of errors (MSB is bit 7). Following the second read the value should be zero.

Possible Problems: If management access to GMII Register 9 (or equivalent) is not available, then this test cannot be performed. In step 13 and 14 the ability to induce errors in either a controlled or uncontrolled manner without causing a link failure may not be possible for a given device.