

**FAST ETHERNET
&
GIGABIT ETHERNET**

**Clause 22, 28 and 40
Management Registers Test Suite**

Technical Document



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Fast Ethernet will only perform Group 1 and Group 2.
Gigabit Ethernet will perform Groups 1, 2, and 3.

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MODIFICATION RECORD

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Erica Williamsen: Updated for editorial improvements.
- January 31, 2001 Version 1.0.5
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- September 8, 2000 Version 1.0.3
Jeremy Kent: Improved procedure for Test #28.1.11 Link Partner Next Page Able.
- August 7, 2000 Version 1.0.2
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Jeremy Kent: Improved observable Results in Test #28.1.2 AN Link Partner Ability Register
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INTRODUCTION

Overview

The University of New Hampshire's InterOperability Laboratory (IOL) is an institution designed to improve the interoperability of standards based products by providing an environment where a product can be tested against other implementations of a standard. This suite of tests has been developed to help implementers evaluate the functioning of their Clause 22, Clause 28 and Clause 40 Auto-Negotiation based products. The tests do not determine if a product conforms to the IEEE 802.3 and IEEE 802.3ab standard, nor are they purely interoperability tests. Rather, they provide one method to isolate problems within an auto-negotiating device. Successful completion of all tests contained in this suite does not guarantee that the tested device will operate with other auto-negotiating devices. However, combined with satisfactory operation in the IOL's interoperability test bed, these tests provide a reasonable level of confidence that the Device Under Test (DUT) will function well in most auto-negotiating environments.

Organization of Tests

The tests contained in this document are organized to simplify the identification of information related to a test and to facilitate in the actual testing process. Each test contains an identification section that describes the test and provides cross-reference information. The discussion section covers background information and specifies why the test is to be performed. Tests are grouped in order to reduce setup time in the lab environment. Each test contains the following information:

Test Number

The Test Number associated with each test follows a simple grouping structure. Listed first is the Test Group Number followed by the test's number within the group. This allows for the addition of future tests to the appropriate groups of the test suite without requiring the renumbering of the subsequent tests.

Purpose

The purpose is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.

References

The references section lists cross references to the IEEE 802.3 standards and other documentation that might be helpful in understanding and evaluating the test and results.

Resource Requirements

The requirements section specifies the hardware, and test equipment that will be needed to perform the test. The items contained in this section are special test devices or other facilities, which may not be available on all devices.

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Last Modification

This specifies the date of the last modification to this test.

Discussion

The discussion covers the assumptions made in the design or implementation of the test as well as known limitations. Other items specific to the test are covered here.

Test Setup

The setup section describes the configuration of the test environment. Small changes in the configuration should be included in the test procedure.

Procedure

The procedure section of the test description contains the step-by-step instructions for carrying out the test. It provides a cookbook approach to testing, and may be interspersed with observable results.

Observable Results

The observable results section lists observables that can be examined by the tester to verify that the DUT is operating properly. When multiple values are possible for an observable, this section provides a short discussion on how to interpret them. The determination of a pass or fail for a certain test is often based on the successful (or unsuccessful) detection of a certain observable.

Possible Problems

This section contains a description of known issues with the test procedure, which may effect test results in certain situations.

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GROUP 1: CLAUSE 22 MANAGEMENT FUNCTION REQUIREMENTS

Scope: The following tests cover Auto-Negotiation operation specific to the management register set.

Overview: These tests are designed to verify that the device under test properly implements the media independent interface (MII) register set as it pertains to the Auto-Negotiation function. Register functions explored are defined in Clause 22 (MII) of IEEE 802.3. Many of these tests are aimed at verifying the critical link between a conformant Auto-Negotiation state machine implementation and the overall system's management and control software.

NOTE: THESE TESTS ARE PERFORMED FOR BOTH FAST ETHERNET AND GIGABIT ETHERNET CONSORTIUMS. THESE TESTS CANNOT BE PERFORMED IF REGISTER ACCESS IS NOT PROVIDED.

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Test #22.1.1: Main Reset

Purpose: To verify that bit 0.15 controls the resetting of the PHY and Auto-Negotiation process.

References:

- [1] IEEE Std 802.3, 2000 Edition: Sections 22.2.4.1 Table 22-7, 22.2.4.1.1, 28.2.4.1.8 Table 28-8, 28.3.1, 28.3.4 Figure 28-16

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: January 31, 2001

Discussion: Bit 0.15 of the control register gives management the ability to reset all of the control and status registers, as well as restarting the Auto-Negotiation process.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100 Ω line termination.

Procedure:

1. Wait until the DUT has begun to transmit FLPs
2. Set bit 0.15 in the control register
3. Observe transmissions from the DUT

Observable Results:

- The DUT should stop Auto-Negotiation, wait break_link_timer, and then restart Auto-Negotiation by sending FLPs.

Possible Problems: If management access is not provided, then this test cannot be performed.

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Test #22.1.2: Auto-Negotiation Enable

Purpose: To verify that bit 0.12 controls the enabling/disabling of the Auto-Negotiation process.

References:

- [1] IEEE Std 802.3, 2000 Edition: Sections 22.2.4.1 Table 22-7, 22.2.4.1.4, 28.2.4.1.8 Table 28-8, 28.3.1, 28.3.4 Figure 28-16

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: January 31, 2001

Discussion: Management has the ability to enable Auto-Negotiation by setting bit 0.12 to one and to disable Auto-Negotiation by setting bit 0.12 to zero. If the management has set bit 0.12 to zero, then the DUT should never source FLPs, and a link will be established using bits 0.13 and 0.6 (speed selection), and bit 0.8 (duplex mode) of the control register. When bit 0.12 is set to one, the DUT should transmit FLPs and establish a link using the Auto-Negotiation process.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination

Procedure:

1. Write a value of one to bit 0.12
2. Observe transmissions from the DUT (a)
3. Repeat steps 1 and 2, writing a value of zero to bit 0.12 (b)
4. Repeat steps 1 and 2, writing a value of one to bit 0.12 (c)

Observable Results:

- a) The DUT should commence Auto-Negotiation and transmit FLPs after step 1.
- b) The DUT should cease Auto-Negotiation and proceed to transmit valid link signaling (based on bits 0.6 and 0.13) after step 3. The DUT may wait `break_link_timer` before sourcing valid link signaling.
- c) The DUT should cease idle transmission, wait `break_link_timer`, and then transmit FLPs after step 4.

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #22.1.3: Auto-Negotiation Restart

Purpose: To verify that bit 0.9 controls the restarting of Auto-Negotiation.

References:

- [1] IEEE Std 802.3, 2000 Edition: Sections 22.2.4.1 Table 22-7, 22.2.4.1.7, 28.2.4.1.8 Table 28-8, 28.3.1, 28.3.4 Figure 28-16

Resource Requirements:

- **Line Monitor:** A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- **Traffic Generator:** A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: January 31, 2001

Discussion: The MII Control Register provides a means for management to restart Auto-Negotiation by writing a value of one to bit 0.9 of the register. This is a way to restart Auto-Negotiation without resetting the entire PHY.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100 Ω line termination.

Procedure:

1. Send a series of FLPs to the DUT encoded with 8001h
2. While the DUT is sending FLPs, write a value of one to bit 0.9
3. Observe transmissions from the DUT

Observable Results:

- The DUT should cease transmission, wait `break_link_timer`, and then start to transmit FLPs

Possible Problems: If management access is not provided, then this test cannot be performed.

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Test #22.1.4: Auto-Negotiation Complete

Purpose: To verify that bit 1.5 is properly set upon completion of Auto-Negotiation and entrance into the FLP LINK GOOD state.

References:

- [1] IEEE Std 802.3, 2000 Edition: Sections 22.2.4.2 Table 22-8, 22.2.4.2.10, 28.2.4.1.8 Table 28-8, 28.3.1, 28.3.4 Figure 28-16

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: January 31, 2001

Discussion: Once a link has been established, management needs to be made aware that frame transmission and reception can commence. Bit 1.5 is set when Auto-Negotiation is complete and a link has come up.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100 Ω line termination.

Procedure:

1. Disable Auto-Negotiation by writing a value of zero to bit 0.12.
2. Use the Traffic Generator to send enough FLPs to put the DUT through the COMPLETE ACKNOWLEDGE state.
3. Observe the status of bit 1.5
4. Use the Traffic Generator to send enough FLPs to put the DUT through the COMPLETE ACKNOWLEDGE state followed by valid link signaling in order to establish a link
5. Observe the status of bit 1.5
6. Repeat steps 2-5 with Auto-Negotiation enabled.

Observable Results:

- a) When Auto-Negotiation is disabled, the value of bit 1.5 should never be set to one.
- b) When Auto-Negotiation is enabled, the DUT should not set bit 1.5 until it has entered the FLP LINK GOOD state. Thus in step 2 bit 1.5 should be 0 and in step 4 bit 1.5 should be 1.

Possible Problems: If management access is not provided, then this test cannot be performed.

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Test #22.1.5: Link Status

Purpose: To verify that bit 1.2 of the status register is set when a valid link has been established and is not set if a valid link has not been established.

References:

- [1] IEEE Std 802.3, 2000 Edition: Sections 22.2.4.2 Table 22-8, 22.2.4.2.13, 28.2.6.1.1, 28.3.1, 28.3.4 Figure 28-16

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: January 31, 2001

Discussion: Management is made aware that a valid link has been established by bit 1.2 of the MII Status Register. When this bit is set, it means that the DUT has entered the FLP LINK GOOD state, regardless of whether or not Auto-Negotiation is enabled or disabled.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Send the DUT a series of FLPs and link signaling such that a link will be established
2. Monitor the status of bit 1.2
3. Turn off Auto-Negotiation (if possible)
4. Send the DUT an Idle pattern to manually force a link
5. Monitor the status of bit 1.2

Observable Results:

- The DUT should not set bit 1.2 until the FLP LINK GOOD state has been entered, regardless of whether or not Auto-Negotiation has been used to established a link.

Possible Problems: If management access is not provided, then this test cannot be performed.

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Test #22.1.6: Auto-Negotiation Ability

Purpose: To verify that the DUT keeps bit 1.3 set.

References:

- [1] IEEE Std 802.3, 2000 Edition: Sections 22.2.4.2 Table 22-8, 22.2.4.2.12, 28.2.4.1.8 Table 28-8

Resource Requirements:

- None

Last Modification: January 31, 2001

Discussion: Management is made aware that an Auto-Negotiation capable PHY is attached via the status register bit 1.3 "Auto-Negotiation Ability". Thus, management is made aware of the PHYs capability, regardless of the management's desire to enable or disable Auto-Negotiation. While this bit may appear unnecessary in most static implementations, it allows for a DUT with an exposed MII interface to discover the Auto-Negotiation capability of an attached PHY.

Test Setup: Access the DUT's Management Registers.

Procedure:

1. Disable Auto-Negotiation (set bit 0.12 to zero).
2. Read the DUT's Status Register, bit 1.3
3. Enable Auto-Negotiation (set bit 0.12 to one).
4. Read the DUT's Status Register, bit 1.3

Observable Results:

- Bit 1.3 must be set, regardless of whether Auto-Negotiation is enabled or not.

Possible Problems: If management access is not provided, then this test cannot be performed.

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Test #22.1.7: Report PHY Capabilities

Purpose: To verify that the PHY set bits 1.15:8 and 15.15:12 appropriately for the PHY's capabilities.

References:

- [1] IEEE Std 802.3, 2000 Edition: Sections 22.2.4.2, Table 22-8, 22.2.4.2.1, 22.2.4.2.2, 22.2.4.2.3, 22.2.4.2.4, 22.2.4.2.5, 22.2.4.2.6, 22.2.4.2.7, 22.2.4.2.16, 22.2.4.4, Table 22-9, 22.2.4.4.1, 22.2.4.4.2, 22.2.4.4.3, 22.2.4.4.4.

Resource Requirements:

- None

Last Modification: January 31, 2001

Discussion: Management is made aware that a PHY's signaling capabilities via the status register bits 1.15:9. If bit 1.8 is set, then the PHY has additional capabilities specified in the Extended Status Register (Register 15) bits 15.15:12. Thus, management is made aware of the PHY's capability, regardless of the management's desire to enable or disable that technology. While these bits may appear unnecessary in most static implementations, it allows for a DUT with an exposed MII/GMII interface to discover the Auto-Negotiation capability of an attached PHY. (Note, an exposed GMII interface is not specified by 802.3)

Status Register technology capability bit definitions

Bit(s)	Name	Description	R/W
1.15	100BASE-T4	1=PHY able to perform 100BASE-T4	RO
1.14	100BASE-X Full Duplex	1=PHY able to perform 100BASE-X FD	RO
1.13	100BASE-X Half Duplex	1=PHY able to perform 100BASE-X HD	RO
1.12	10BASE-T Full Duplex	1=PHY able to perform 10BASE-T FD	RO
1.11	10BASE-T Half Duplex	1=PHY able to perform 10BASE-T HD	RO
1.10	100BASE-T2 Full Duplex	1=PHY able to perform 100BASE-T2 FD	RO
1.9	100BASE-T2 Half Duplex	1=PHY able to perform 100BASE-T2 HD	RO
1.8	Extended Status	1=Extended status info in Register 15	RO
15.15	1000BASE-X Full Duplex	1=PHY able to perform 1000BASE-X FD	RO
15.14	1000BASE-X Half Duplex	1=PHY able to perform 1000BASE-X HD	RO
15.13	1000BASE-T Full Duplex	1=PHY able to perform 1000BASE-T FD	RO
15.12	1000BASE-T Half Duplex	1=PHY able to perform 1000BASE-T HD	RO

Test Setup: Access the DUT's Management Registers.

Procedure:

1. Read bits 1.15:8 and 15.15:12.

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Observable Results:

- Bits 1.15:9 and 15.15:12 must be set appropriately. Bit 1.8 must be set if Register 15 is non 0.

Possible Problems: If management access is not provided, then this test cannot be performed.

GROUP 2: CLAUSE 28 MANAGEMENT REGISTERS

Scope: The following tests cover Auto-Negotiation operation specific to the management register set.

Overview: These tests are designed to verify that the device under test properly implements the media independent interface (MII) register set as it pertains to the Auto-Negotiation function. Register functions explored are defined in Clause 28 (Auto-Negotiation) of IEEE 802.3. Many of these tests are aimed at verifying the critical link between a conformant Auto-Negotiation state machine implementation and the overall system's management and control software.

NOTE: THESE TESTS ARE PERFORMED BY BOTH FAST ETHERNET AND GIGABIT ETHERNET CONSORTIUMS. THESE TESTS CANNOT BE PERFORMED IF REGISTER ACCESS IS NOT PROVIDED.

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Test #28.1.1: AN Advertisement Register

Purpose: To verify that the Auto-Negotiation advertisement register (Register 4) is reflected in the Link Code Words transmitted by the DUT.

References:

- [1] IEEE Std 802.3, 2000 Edition: Sections 28.2.4.1.3 Table 28-2, Annex 28A, Annex 28B, Annex 28D, 40.5.1.1 Table 40-3

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.

Last Modification: January 31, 2001

Discussion: For a device to advertise abilities that it possesses, it must be able to configure the abilities advertised during the Auto-Negotiation process so that they match the device's true capabilities. Register 4 of the MII is defined to contain these abilities, however, if the device does not use a MII then the logical equivalent must be provided.

Advertisement register bit definitions

Bit(s)	Name	Description	R/W
4.15	Next Page	See 28.2.1.2	R/W
4.14	Reserved	Write as 0	RO
4.13	Remote Fault	See 28.2.1.2	R/W
4.12:5	Technology Ability Field	See 28.2.1.2	R/W
4.4:0	Selector Field	See 28.2.1.2	R/W

Test Setup: Using a Cat 5 cord, connect the DUT's transmitter to the Line Monitor. Terminate the DUT's transmit channel with a 100Ω line termination. Using a Cat 5 cord, connect the DUT's receiver to the Traffic Generator using a 100Ω line termination.

Procedure:

1. Via management, access Register 4 and write the value 8001h
2. Observe transmission from the DUT
3. Repeat steps 1-3 with other test values including (but not limited to) E001h, 0000h, and FFFFh

Observable Results:

- a) The Link Code Words transmitted by the DUT should contain the bit values 4.15, and 4.13-4.0 that were written to Register 4.
- b) The Link Code Words transmitted by the DUT should contain the bit value of zero for 4.14.

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Possible Problems: If management access is not provided, then this test cannot be performed.

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Test #28.1.2: AN Link Partner Ability Register

Purpose: To verify that the Auto-Negotiation link partner ability register is set according to Table 28-8 based upon the reception of Link Code Words by the DUT.

References:

- [1] IEEE Std 802.3, 2000 Edition: Sections 28.2.4.1.4, Table 28-3, Annex 28A, Annex 28B, Annex 28D

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: January 31, 2001

Discussion: For a device to resolve a proper link configuration, it must accurately receive its partner's abilities and relate them to management. Register 5 of the MII is defined to contain these abilities, if the DUT does not use a MII then the logical equivalent must be provided.

Link Partner ability register bit definitions

Bit(s)	Name	Description	R/W
5.15	Next Page	See 28.2.1.2	RO
5.14	Acknowledge	See 28.2.1.2	RO
5.13	Remote Fault	See 28.2.1.2	RO
5.12:5	Technology Ability Field	See 28.2.1.2	RO
5.4:0	Selector Field	See 28.2.1.2	RO

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Send the DUT Link Code Words containing the value 8001h
2. Access and read Register 5.
3. Repeat steps 1-2 by sending values including (but not limited to) FFFFh, 0000h
4. Attempt to write FFFFh to Register 5, then read the contents of Register 5.

Observable Results:

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- a) The bits of the Link Code Word received by the DUT should be contained in Register 5 exactly as they were received once the DUT has entered the COMPLETE ACKNOWLEDGE state.
- b) The DUT should not allow any of the bits of Register 5 to be written.

Possible Problems: If management access is not provided, then this test cannot be performed.

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Test #28.1.3: Remote Fault

Purpose: To verify that the DUT sets bit 1.4 upon reception of a Link Code Word with the remote fault bit set.

References:

[1] IEEE Std 802.3, 2000 Edition: Sections 22.2.4.2, Table 22-8, 22.2.4.2.11, 28.2.3.5

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: January 31, 2001

Discussion: A device which supports the Remote Fault function must indicate the reception of a base page with the RF bit set by setting bit 1.4 in the MII Status Register. In this way, management is made aware of a remote fault indication from the link partner. After management reads the status register, bit 1.4 should reset to zero. If the DUT does not support the Remote Fault function, no action is necessary.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Read the MII Status Register (Register 1) twice.
2. Use the Traffic Generator to send enough FLPs with the RF bit set to put the DUT through the COMPLETE ACKNOWLEDGE state.
3. Read the MII Status Register (Register 1).
4. Read the MII Status Register again.

Observable Results:

- a) In step 1, bit 1.4 should not be set and in step 3, bit 1.4 may be set.
- b) If bit 1.4 was set in step 3, it must be cleared in step 4.

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #28.1.4: Parallel Detection Fault

Purpose: To verify that the DUT sets bit 6.4 upon reception of a parallel detection fault.

References:

- [1] IEEE Std 802.3, 2000 Edition: Sections 28.2.4.1.5 Table 28-5, 28.2.4.1.8 Table 28-8, 28.3.1, 28.3.4 Figure 28-16

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: January 31, 2001

Discussion: Management is made aware that a parallel detection fault has occurred by reading bit 6.4 of the Auto-Negotiation expansion register. Upon receiving such a fault, the DUT must set this bit. A value of 1 means that a fault has been detected via the parallel detection function, while a value of 0 indicates that a fault has not been detected via the parallel detection function. A parallel detection fault occurs if zero or more than one PMA is indicated to have link_status=READY when the autoneg_wait_timer expires during the parallel detection process. The parallel detection fault bit should be reset upon a read to the Auto-Negotiation expansion register.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Send the DUT valid link signaling for <500ms such that the DUT stops sending FLPs.
2. Read the Auto-Negotiation Expansion Register (Register 6) twice.
3. Repeat steps 1 & 2 sending valid link signaling for all supported PMAs. (This may be lc_max NLPs, 100BASE-TX Idle, or 100BASE-T4).

Observable Results:

- Bit 6.4 should be set to one the first time the Auto-Negotiation expansion register is read, and set to zero the second time the register is read.

Possible Problems: If management access is not provided, then this test cannot be performed. If the DUT does not support 10BASE-T, 100BASE-TX or 100BASE-T4 then this test cannot be performed.

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Test #28.1.5: Page Received Setting/Resetting

Purpose: To verify that `mr_page_rx` is set when a new page is received and cleared when the Auto-Negotiation expansion register is read.

References:

- [1] IEEE Std 802.3, 2000 Edition: Sections 28.2.4.1.5, Table 28-5, 28.2.4.1.8, Table 28-8, 28.3.1, 28.3.4, Figure 28-16

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: January 31, 2001

Discussion: Management is made aware of the reception of a new page by reading bit 6.1 in the Auto-Negotiation expansion register. If bit 6.1 is set, then management can look at the contents of the received page and act accordingly. Upon reading of this register, this bit is cleared so that management may not read the register again and think that the same page is a new page.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. If the DUT supports Next Page exchange, set the NP bit in the DUT's base page (bit 4.15)
2. Send the DUT a constant stream of FLPs encoded with 8001h
3. Read bit 6.1 twice
4. Repeat steps 1-3 with an encoding of C001h
5. Restart Auto-Negotiation and send enough FLPs encoded with C001h to enter COMPLETE ACKNOWLEDGE followed by a constant stream of FLPs encoded with E808h to again cause the DUT to enter COMPLETE ACKNOWLEDGE.
6. Read bit 6.1 (should be one)
7. Write the desired next page value to register 7
8. Read bit 6.1 (should be one)
9. Read bit 6.1 (should be zero)

Observable Results:

- a) After step 2, bit 6.1 should be zero for both reads
- b) After step 3, bit 6.1 should be one for the first read and zero for the second read

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- c) If the DUT supports Next Page exchange, after step 5, bit 6.1 should be one for the first two reads and zero for the third read

Possible Problems: If management access is not provided, then this test cannot be performed.

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Test #28.1.6: Link Partner Auto-Negotiation Able

Purpose: To verify that the DUT sets bit 6.0 upon detection of link partner which is capable of Auto-Negotiation.

References:

- [1] IEEE Std 802.3, 2000 Edition: 28.2.4.1.5, Table 28-5, 28.2.4.1.8, Table 28-8, 28.3.4 Figure 28-16

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: January 31, 2001

Discussion: A device's management is made aware that the Link Partner is capable of Auto-Negotiation when the DUT enters the ACKNOWLEDGE DETECT state and sets `mr_lp_autoneg_able` to true. This in-turn sets bit 6.0 in the Expansion Register to 1. Whenever the DUT re-enters the ABILITY DETECT state, `mr_lp_autoneg_able` should be reset to false (6.0 set to 0).

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Send nothing to the DUT and read bit 0 of the Expansion Register (Register 6).
2. Use the Traffic Generator to send a constant stream of identical FLPs without ACK set to put the DUT in the ACKNOWLEDGE DETECT state.
3. Read bit 0 of the Expansion Register (Register 6).
4. Send nothing to the DUT and wait until the DUT re-enters the ABILITY DETECT state (and then send FLPs without ACK set)
5. Read bit 0 of the Expansion Register (Register 6).
6. Use the Traffic Generator to send a constant stream of FLPs alternating in content and without ACK set, to keep the DUT in the ABILITY DETECT state.
7. Read bit 0 of the Expansion Register (Register 6).

Observable Results:

- a) In step 3, bit 6.0 should be set to one.
- b) In steps 1, 5 and 7 bit 6.0 should be set to zero.

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Possible Problems: If management access is not provided, then this test cannot be performed.

Test #28.1.7: AN Next Page Transmit Register

Purpose: To verify that the Auto-Negotiation Next Page transmit register, set according to Table 28-6, is properly reflected in the Next Pages transmitted by the DUT.

References:

[1] IEEE Std 802.3, 2000 Edition: Sections 28.2.3.4, 28.4.1.6, Table 28-6

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: January 31, 2001

Discussion: During a Next Page exchange, management must have the ability to control the contents of the pages to be transmitted. MII Register 7 is used to specify these abilities, however, if the device does not use a MII then the logical equivalent must be provided. The definition of Register 7 is provided below for convenience.

Next Page transmit register bit definitions

Bit(s)	Name	Description	R/W
7.15	Next Page	See 28.2.3.4	R/W
7.14	Reserved	Write as 0	RO
7.13	Message Page	See 28.2.3.4	R/W
7.12	Acknowledge 2	See 28.2.3.4	R/W
7.11	Toggle	See 28.2.3.4	RO
7.10:0	Message/Unformatted Code Field	See 28.2.3.4	R/W

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Set the NP bit in the DUT's base page (bit 4.15)
2. Send a constant stream of FLPs to the DUT containing the abilities C1E1h
3. Via management, read Register 7 and write a value of 2008h
4. Observe transmission from the DUT

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5. Repeat using values including (but not limited to) 2808h, and FFFFh

Observable Results:

- a) The Next Pages transmitted by the DUT should have bits 7.15, 7.13, 7.12, and 7.10:0 set to what was written to Register 7.
- b) The Next Pages transmitted by the DUT should have bit 7.14 set to zero, and bit 7.11 set to the opposite of the value of bit 4.11 in the initial Link Code Word sent by the DUT.

Possible Problems: If management access is not provided, then this test cannot be performed. If the DUT does not support a Next Page exchange, then this test cannot be performed.

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Test #28.1.8: AN Link Partner Ability Next Page Register

Purpose: To verify that the Auto-Negotiation link partner ability Next Page register is set according to Table 28-8 based upon the reception of Next Pages by the DUT.

References:

[1] IEEE Std 802.3, 2000 Edition: Section 28.2.3.4, 28.2.4.1.7, Table 28-7

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: January 31, 2001

Discussion: For a device to resolve a proper link configuration, it must accurately receive its partner's Next Page abilities and relate them to management. Register 8 of the GMII is defined to contain these abilities, however, if the DUT does not use a GMII then the logical equivalent must be provided. The definition of Register 8 is provided below for convenience.

Link Partner Next Page Ability register bit definitions

Bit(s)	Name	Description	R/W
8.15	Next Page	See 28.2.3.4	RO
8.14	Reserved	See 28.2.3.4	RO
8.13	Message Page	See 28.2.3.4	RO
8.12	Acknowledge 2	See 28.2.3.4	RO
8.11	Toggle	See 28.2.3.4	RO
8.10:0	Message/Unformatted Code Field	See 28.2.3.4	RO

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Set the NP bit in the DUT's base page (bit 4.15)
2. Send the DUT enough FLPs with the Next Page bit set so that the DUT enters the COMPLETE ACKNOWLEDGE state, followed by a constant stream of FLPs encoded with 2008h.
3. It may be necessary to write any value (typically 2001) to register 7 to cause the DUT to enter the NEXT PAGE WAIT and thus eventually return to the COMPLETE ACKNOWLEDGE state.
4. Via management, access and read Register 8

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5. Repeat using Next Pages including (but not limited to) 2808h, FFFFh and 0000h. If the toggle bit (D11) is set to a value of zero in the Next Pages (as in a next page value of 0000h), it should be set to a value of one in the base pages.
6. Write the value FFFFh to Register 8. Then read Register 8.

Observable Results:

- a) The bits of the Next Pages received by the DUT should be contained in Register 8 exactly as they were received.
- b) A write to Register 8 should not affect its contents.

Possible Problems: If management access is not provided, then this test cannot be performed. If the DUT does not support a Next Page exchange, then this test cannot be performed.

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Test #28.1.9: mr_next_page_loaded

Purpose: To verify that mr_next_page_loaded is set upon write to the Auto-Negotiation Next Page Transmit Register, and cleared in the states NEXT PAGE WAIT and TRANSMIT DISABLE.

References:

[1] IEEE Std 802.3, 2000 Edition: Sections 28.2.4.1.8, Table 28-8, 28.3.1, 28.3.4, Figure 28-16

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: January 31, 2001

Discussion: The mr_next_page_loaded variable is a key parameter in the transition from COMPLETE ACKNOWLEDGE to NEXT PAGE WAIT. It prevents the Auto-Negotiation protocol from proceeding until management has had time to load the AN Next Page transmit register with the Next Page to be transmitted. This occurs after the management has had time to read the previous Next Page received from its link partner (in the AN link partner ability Next Page register). mr_next_page_loaded is automatically set when management writes the AN Next Page transmit register, but should be cleared in the TRANSMIT DISABLE or NEXT PAGE WAIT states. This test observes that the proper effects of mr_np_loaded being set takes place, and that the value is reset appropriately.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Set the Next Page bit in the devices base page (write a 1 to bit 15 of MII Register 4).
2. Write '2201h' to the Next Page Transmit Register (MII Register 7).
3. Restart Auto-Negotiation (write a 1 to bit 12 of MII Register 0).
4. Use the Traffic Generator to send a constant stream of FLPs with the Next Page bit set to cause the DUT to enter the COMPLETE ACKNOWLEDGE state. The FLPs should be a repeating pattern such as 20 81E1 and 20 C1E1.
5. Observe transmissions from the DUT.
6. If the DUT properly remained in the COMPLETE ACKNOWLEDGE state while sending its base page in step 5, then write '2301h' to Register 7. Else, if the DUT remained in the COMPLETE ACKNOWLEDGE state while sending its first Next Page (2201h), then part (a) fails and then write '2301h' to Register 7 to trigger the 2nd Next Page transmission. Else stop.
7. Observe transmissions from the DUT.

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8. If the DUT properly remained in the COMPLETE ACKNOWLEDGE state in step 7, then write '2401h' to Register 7.

Observable Results:

- a) Resetting in TRANSMIT DISABLE state: In step 5, the DUT should remain in the COMPLETE ACKNOWLEDGE state and continue to send its base page with ACK.
- b) Setting mr_next_page_loaded: In step 7, the DUT should commence transmitting its first Next Page, with the proper toggle and ack bit values.
- c) Resetting in NEXT PAGE WAIT state: In step 7, the DUT should remain in the COMPLETE ACKNOWLEDGE state and continue to send its first Next Page (2301h).

Possible Problems: If the DUT does not support Next Page exchange, then this test cannot be performed. If management access is not provided, then this test cannot be performed.

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Test #28.1.10: Next Page Able

Purpose: To verify that the DUT sets bit 6.2 if it is capable of a Next Page exchange.

References:

- [1] IEEE Std 802.3, 2000 Edition: Sections 28.2.4.1.5, Table 28-5, 28.2.4.1.8 Table 28-8, 28.3.1, 28.3.4 Figure 28.16

Resource Requirements:

- None

Last Modification: January 31, 2001

Discussion: A PHY which supports Next Page exchange must indicate this capability to management by setting bit 6.2 in the Expansion Register (Register 6), regardless of whether a Next Page exchange is desired. While this bit may appear unnecessary in most static implementations, it allows for a DUT with an exposed MII interface to discover any Next Page exchange capability of an attached PHY.

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Disable Next Page advertisement (set bit 4.15 to zero).
2. Read bit 6.2 of the MII Expansion Register (Register 6).
3. Enable Next Page advertisement (set bit 4.15 to one).
4. Read bit 6.2 of the MII Expansion Register (Register 6).

Observable Results:

- Bit 6.2 must be set if the DUT supports a Next Page exchange, regardless of whether a Next Page exchange is currently desired.

Possible Problems: If management access is not provided, then this test cannot be performed.

Test #28.1.11 Link Partner Next Page Able

Purpose: To verify that the DUT sets bit 6.3 upon reception of a base page which has bit 15 set.

References:

- [1] IEEE Std 802.3, 2000 Edition: Sections 28.2.4.1.5, Table 28-5, 28.2.4.1.8, Table 28-8, 28.3.1, 28.3.4 Figure 28-16

Resource Requirements:

- **Line Monitor:** A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- **Traffic Generator:** A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: January 31, 2001

Discussion: A device's management is made aware that the Link Partner is capable of a Next Page exchange, and also desires a Next Page exchange when the DUT enters the COMPLETE ACKNOWLEDGE state. Upon entrance, the DUT sets `mr_lp_np_able` to true, this in-turn sets bit 6.3 in the Expansion Register to 1. Whenever the DUT re-enters the ABILITY DETECT state, `mr_lp_np_able` should be reset to false (6.3 set to 0).

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Disable Next Page advertisement (set bit 4.15 to zero).
2. Send nothing to the DUT and read bit 6.3 of the Expansion Register (Register 6).
3. Use the Traffic Generator to send a constant stream of identical FLPs with ACK and NP set to put the DUT in the COMPLETE ACKNOWLEDGE state.
4. Read bit 6.3 of the Expansion Register (Register 6).
5. If the Next Page bit is set, the DUT should remain in the COMPLETE ACKNOWLEDGE state indefinitely. Write a 0 to bit 0.9 or 0.15 to restart Auto-Negotiation or reset the PHY.
6. Read bit 6.3 of the Expansion Register (Register 6).
7. Use the Traffic Generator to send a constant stream of identical FLPs with ACK set, and NP not set, putting the DUT in the COMPLETE ACKNOWLEDGE state.
8. Read bit 6.3 of the Expansion Register (Register 6).
9. Enable Next Page advertisement (set bit 4.15 to one) and repeat step 3 and 4.

Observable Results:

- a) In step 4 and 9, bit 6.3 should be set.

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b) In steps 2, 6 and 8, bit 6.3 should not be set.

Possible Problems: If management access is not provided, then this test cannot be performed.

GROUP 3: CLAUSE 40 MANAGEMENT REGISTERS

Scope: The following tests cover Auto-Negotiation operation specific to the management register set.

Overview: These tests are designed to verify that the device under test properly implements the media independent interface (MII) register set as it pertains to the Auto-Negotiation function. Register functions explored are defined in Clause 40 (1000BASE-T) of IEEE 802.3ab. Many of these tests are aimed at verifying the critical link between a conformant Auto-Negotiation state machine implementation and the overall system's management and control software.

NOTE: THESE TESTS ARE PERFORMED BY GIGABIT ETHERNET ONLY. THESE TESTS CANNOT BE PERFORMED IF REGISTER ACCESS IS NOT PROVIDED.

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Test #40.1.1: 1000BASE-T MASTER/SLAVE Control Register bits 9.10:8

Purpose: To verify for 1000BASE-T devices that the MASTER/SLAVE Control Register bits 9.10:8 properly control the advertised Port type and duplex.

References:

[1] IEEE Std 802.3, 2000 Edition: Sections 40.5.1.1, Table 40-3, Table 40-4

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: January 31, 2001

Discussion: In order for 1000BASE-T devices to automatically configure themselves, they must complete the exchange of a base page and three Next Pages during the Auto-Negotiation process. A system's management entity could control this entire exchange by the normal writing of MII Register 4 (Base Page Advertised Ability Register) as well as MII Register 7 (Next Page Transmit Register). However, such an approach would require each systems management to be capable of properly following clause 28's Next Page exchange mechanism. To remove this burden from system implementers, many suppliers of 1000BASE-T PHYs also incorporate the option of having an automatic embedded Next Page exchange management entity control the process. To enable this, the embedded controller must be aware of the system's desired mode of operation for the 1000BASE-T port. The system accomplishes this by writing to the MASTER/SLAVE Control Register (GMII Register 9). To specify what type of device the system is (multiport or single port) as well as the desired duplex mode for the port, the system simply writes to bits 9:10-8 (see table below). Once set, the system can either enable the port, reset the port, or restart Auto-Negotiation and the embedded Next Page exchange controller will do the rest of the page exchange work. Recall that these bits are only meaningful if an embedded controller is in use. If one is not present, or disabled, then the system's management entity is required to properly complete the Next Page exchange via the properly timed writing of Register 7. In such an event, it is recommended that the contents of register 9 accurately reflect the abilities advertised in the second Next Page of the 1000BASE-T exchange.

1000BASE-T MASTER/SLAVE Control register bit definitions for ability advertisement

Bit(s)	Name	Description	Type
9.10	Port type	1=Multiport device 0=Single Port device	R/W
9.9	1000BASE-T Full Duplex	1=Advertise PHY is 1000BASE-T full duplex capable 0=Advertise PHY is not 1000BASE-T full duplex capable	R/W
9.8	1000BASE-T Half Duplex	1=Advertise PHY is 1000BASE-T half duplex capable 0=Advertise PHY is not 1000BASE-T half duplex capable	R/W

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Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Via management access, write to GMII Register 9 bits 10-8 (or equivalent) the value '111b'.
2. Use the Traffic Generator to send enough FLPs to put the DUT through the COMPLETE ACKNOWLEDGE state, followed by enough null pages (with proper toggle bit values) to allow the DUT to transmit all of its Next Pages
3. Monitor the Next Pages transmitted by the DUT.
4. Repeat steps 1 through 3 changing the value written to '000b'

Observable Results:

- a) Bits U2 - U4 in the second Next Page (third overall page) transmitted by the DUT should match the value written in step 1, without exception.

Possible Problems : If management access to GMII Register 9 (or equivalent) is not available, then this test cannot be performed.

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Test #40.1.2: 1000BASE-T MASTER/SLAVE Control Register bits 9.12:11

Purpose: To verify for 1000BASE-T devices that the MASTER/SLAVE Control Register bits 9.12:11 properly control MASTER-SLAVE Manual Configuration.

References:

[1] IEEE Std 802.3, 2000 Edition: Sections 40.5.1.1, Table 40-3, Table 40-4

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- Traffic Generator: A system capable of generating and transmitting normal link pulses (NLPs) and fast link pulses (FLPs) while connected to the receiver of the DUT.

Last Modification: January 31, 2001

Discussion: In order for 1000BASE-T devices to automatically configure themselves, they must complete the exchange of a base page and three Next Pages during the Auto-Negotiation process. A system's management entity could control this entire exchange by the normal writing of MII Register 4 (Base Page Advertised Ability Register) as well as MII Register 7 (Next Page Transmit Register). However, such an approach would require each systems management to be capable of properly following clause 28's Next Page exchange mechanism. To remove this burden from system implementers, many suppliers of 1000BASE-T PHYs also incorporate the option of having an automatic embedded Next Page exchange management entity control the process. To enable this, the embedded controller must be aware of the system's desired mode of operation for the 1000BASE-T port. The system accomplishes this by writing to the MASTER/SLAVE Control Register (GMII Register 9). To specify that the port should be forced to be either MASTER or SLAVE, the system must set bit 9.12 to 1, and set 9.11 to either 1 or 0 (see table below). Once set, the system can either enable the port, reset the port, or restart Auto-Negotiation and the embedded Next Page exchange controller will do the rest of the page exchange work. Recall that these bits are only meaningful if an embedded controller is in use. If one is not present, or disabled, then the system's management entity is required to properly complete the Next Page exchange via the properly timed writing of Register 7. In such an event, it is recommended that the contents of register 9 accurately reflect the abilities advertised in the second Next Page of the 1000BASE-T exchange.

**1000BASE-T MASTER/SLAVE Control register bit definitions for
MASTER-SLAVE Manual Configuration**

Bit(s)	Name	Description	Type
9.12	MASTER-SLAVE Manual Config Enable	1=Enable MASTER-SLAVE Manual Configuration 0=Disable MASTER-SLAVE Manual Configuration	R/W
9.11	MASTER-SLAVE Config Value	1=Configure PHY as MASTER during MASTER-SLAVE negotiation, only when 9.12 is set to logical one. 0= Configure PHY as SLAVE during MASTER-SLAVE	R/W

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		negotiation, only when 9.12 is set to logical one.	
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Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Via management access, write to GMII Register 9 bits 12-11 (or equivalent) the value '11b'.
2. Use the Traffic Generator to send enough FLPs to put the DUT through the COMPLETE ACKNOWLEDGE state, followed by enough null pages (with proper toggle bit values) to allow the DUT to transmit all of its Next Pages
3. Monitor the Next Pages transmitted by the DUT.
4. Repeat steps 1 through 3 changing the value written to '00b', and '10b'.
5. Repeat steps 1 through 3 changing the value written to '01b'.

Observable Results:

- a) Bits U0 & U1 in the second Next Page (third overall page) transmitted by the DUT should match the value written in step 1, except for the value written in step 5.
- b) In step 5, the DUT may either set U0 to 0, and U1 to 1 (which should be ignored since U0=0) or the DUT may set both U0 and U1 to 0.

Possible Problems: If management access to GMII Register 9 (or equivalent) is not available, then this test cannot be performed.

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Test #40.1.3: 1000BASE-T MASTER/SLAVE Status Register

Purpose: To verify for 1000BASE-T devices that the MASTER/SLAVE Status Register conforms to the definition in Table 40-3.

References:

- [1] IEEE Std 802.3, 2000 Edition: Sections 40.5.1.1, Table 40-3, Table 40-4

Resource Requirements:

- Line Monitor: A system capable of detecting, time-stamping, and recording normal link pulses (NLPs) on both the receive and transmit channels of the DUT. The channel signaling should pass through the line monitor with minimal distortion.
- 1000BASE-T Traffic Generator: A system capable of properly completing the 1000BASE-T Next Page exchange and establishing a valid 1000BASE-T link.

Last Modification: January 13, 2000

Discussion: Once a 1000BASE-T device completes Auto-Negotiation, status information specific to the 1000BASE-T link must be properly represented in the MASTER-SLAVE Status Register (GMII Register 10).

1000BASE-T MASTER/SLAVE Status Register bit definitions

Bit(s)	Name	Description	Type
10.15	MASTER-SLAVE configuration fault	1=MASTER-SLAVE configuration fault detected 0=No MASTER-SLAVE configuration fault detected	RO/LH/SC
10.14	MASTER-SLAVE configuration resolution	1=Local PHY configuration resolved to MASTER 0=Local PHY configuration resolved to SLAVE	RO
10.13	Local Receiver Status	1=Local Receiver OK (loc_rcvr_status=OK) 0= Local Receiver not OK (loc_rcvr_status=NOT_OK)	RO
10.12	Remote Receiver Status	1=Remote Receiver OK (rem_rcvr_status=OK) 0= Remote Receiver not OK (rem_rcvr_status=NOT_OK)	RO
10.11	LP 1000T FD	1=Link Partner is capable of 1000BASE-T full duplex 0=Link Partner is not capable of 1000BASE-T full duplex	RO
10.10	LP 1000T HD	1=Link Partner is capable of 1000BASE-T half duplex 0=Link Partner is not capable of 1000BASE-T half duplex	RO
10.9:8	Reserved	Reserved	RO
10.7:0	Idle Error Count	Count of each occurrence of rxerror_status=ERROR. Cleared on read. Held at all ones in case of overflow	RO/SC

Test Setup: Using Cat 5 cords, connect the DUT and the Traffic Generator to the Line Monitor such that the traffic generator's signaling will be seen by the DUT's receiver. Terminate the DUT's transmit channel with a 100Ω line termination.

Procedure:

1. Read GMII Register 10 (or equivalent) twice.

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2. Via management access, write to GMII Register 10 (or equivalent) the value 'FFFFh'.
3. Read GMII Register 10 (or equivalent).
4. Use the 1000BASE-T Traffic Generator to complete a proper 1000BASE-T Next Page exchange with the DUT and establish a link. Advertise 1000BASE-T Full Duplex and Half Duplex capability.
5. Read Register 10 bits 10.11 and 10.10. Repeat 4 and 5 until all four bit combinations are tested.
6. Use the 1000BASE-T Traffic Generator to complete a proper 1000BASE-T Next Page exchange with the DUT and establish a link, such that the DUT should be MASTER. If necessary, use the line monitor to verify that the DUT should resolve to MASTER.
7. Read Register 10 bit 14.
8. Repeat step 6 and 7, changing the Next Page exchange such that the DUT should be SLAVE.
9. Configure the DUT to be manual_MASTER. Use the 1000BASE-T Traffic Generator to produce a proper 1000BASE-T Next Page exchange with the DUT, advertising that the Traffic Generator is a manual_MASTER. This should cause the DUT to detect a configuration fault.
10. Read Register 10 bit 15, then read register 10 again.
11. Use the 1000BASE-T Traffic Generator to complete a proper 1000BASE-T Next Page exchange with the DUT and establish a link.
12. Read Register 10 bits 10.13 and 10.12
13. With the 1000BASE-T link still established, attempt to degrade the quality of the link between the two devices by any means, but do not break the link. Either by a controlled noise injection, or an uncontrolled noise injection (such as by very briefly loosening the RJ-45 plug & jack connection.)
14. Read Register 10 bits 7:0, if non-zero, read again. Repeat 13 and 14 until a non-zero value is read.

Observable Results:

- a) The value read step 3 should be identical to the final value read in step 1.
- b) In step 5, the reported link partner duplex capability should match the capability indicated in the received UP1 Next Page.
- c) In step 7, bit 14 should be set to one, in step 8, bit 15 should be set to 0.
- d) In step 10, bit 15 should initially be set. After the second read, the bit should be cleared.
- e) In step 12, bits 13 and 12 should both be set once the link is established.
- f) In step 14, on the first read, following the event of errors, the counter should indicate the number of errors (MSB is bit 7). Following the second read the value should be zero.

Possible Problems: If management access to GMII Register 9 (or equivalent) is not available, then this test cannot be performed. In step 13 and 14 the ability to induce errors in either a controlled or uncontrolled manner without causing a link failure may not be possible for a given device.