FAST ETHERNET CONSORTIUM

Clause 25
Physical Medium Dependent (PMD) Test Suite
Version 3.4

Technical Document

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MODIFICATION RECORD

- March 8, 2006 (Version 3.4)
  Shin Horiuchi: Updated references to 802.3™-2005

- May 16, 2005 (Version 3.3)
  Peter Keefe: Editorial Change to Appendix 25.A and 25.C

- August 27, 2004 (Version 3.21)
  Jon Beckwith: Made minor editorial change in 25.1.8

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  Long Awaited Update
  Jon Beckwith: Added test 25.1.8, Transmit Clock Frequency
  Fixed the procedure of test 25.1.7
  Fixed equation 25.C-5
  Removed support for STP in test 25.1.1
  Minor editorial and formatting changes.
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  Jon Beckwith: Changed format to be consistent with other IOL test suites.

- September 9, 1999 (Version 3.1)
  Adam Healey: Added tests 25.2.2, 25.2.3, 25.2.4, Appendix A, C, and D.

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Bob Noseworthy	University of New Hampshire
Gary Pressler	University of New Hampshire
Nathan Bourgoine	University of New Hampshire

INTRODUCTION

The University of New Hampshire's InterOperability Laboratory (IOL) is an institution designed to improve the interoperability of standards based products by providing an environment where a product can be tested against other implementations of a standard. This particular suite of tests has been developed to help implementers evaluate the functionality of the Physical Medium Dependent (PMD) sublayer of their 100Base-Tx products.

These tests are designed to determine if a product conforms to specifications defined in the IEEE 802.3 standard. Successful completion of all tests contained in this suite does not guarantee that the tested device will operate with other devices. However, combined with satisfactory operation in the IOL's interoperability test bed, these tests provide a reasonable level of confidence that the Device Under Test (DUT) will function properly in many 100Base-Tx environments.

The tests contained in this document are organized in such a manner as to simplify the identification of information related to a test, and to facilitate in the actual testing process. Tests are organized into groups, primarily in order to reduce setup time in the lab environment, however the different groups typically also tend to focus on specific aspects of device functionality. A three-part numbering system is used to organize the tests, where the first number indicates the clause of the IEEE 802.3 standard on which the test suite is based. The second and third numbers indicate the test's group number and test number within that group, respectively. This format allows for the addition of future tests to the appropriate groups without requiring the renumbering of the subsequent tests.

The test definitions themselves are intended to provide a high-level description of the motivation, resources, procedures, and methodologies pertinent to each test. Specifically, each test description consists of the following sections:

Purpose

The purpose is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.

References

This section specifies source material *external* to the test suite, including specific subclauses pertinent to the test definition, or any other references that might be helpful in understanding the test methodology and/or test results. External sources are always referenced by number when mentioned in the test description. Any other references not specified by number are stated with respect to the test suite document itself.

Resource Requirements

The requirements section specifies the test hardware and/or software needed to perform the test. This is generally expressed in terms of minimum requirements, however in some cases specific equipment manufacturer/model information may be provided.

Last Modification

This specifies the date of the last modification to this test.

Discussion

The discussion covers the assumptions made in the design or implementation of the test, as well as known limitations. Other items specific to the test are covered here.

Test Setup

The setup section describes the initial configuration of the test environment. Small changes in the configuration should not be included here, and are generally covered in the test procedure section, below.

Procedure

The procedure section of the test description contains the systematic instructions for carrying out the test. It provides a cookbook approach to testing, and may be interspersed with observable results.

Observable Results

This section lists the specific observables that can be examined by the tester in order to verify that the DUT is operating properly. When multiple values for an observable are possible, this section provides a short discussion on how to interpret them. The determination of a pass or fail outcome for a particular test is generally based on the successful (or unsuccessful) detection of a specific observable.

Possible Problems

This section contains a description of known issues with the test procedure, which may affect test results in certain situations. It may also refer the reader to test suite appendices and/or whitepapers that may provide more detail regarding these issues.

GROUP 1: ACTIVE OUTPUT INTERFACE (AOI) TESTS

Overview:

This group of tests verifies several of the electrical specifications of the 100Base-Tx Physical Medium Dependent sublayer outlined in clause 25 of the IEEE 802.3-2005 standard.

Scope:

All of the tests described in this section have been implemented and are currently active at the University of New Hampshire InterOperability Lab.

Test #25.1.1 – Differential Output Voltage

Purpose: To verify that the differential output voltage of the device under test (DUT) is within the conformance limits.

References:

[1] IEEE Std 802.3-2005, clause 25
[2] ANSI X3.263-1995, section 9.1.2.2
[3] Ibid., Figure 9-1
[4] Ibid., Informative Annex J

Resource Requirements: Refer to Appendix 25.A

Last Modification: November 10, 2003 (Version 2.5)

Discussion:

Reference [1] describes the operation of the Physical Medium Dependent (PMD) sublayer for 100Base-Tx devices. This clause incorporates ANSI X3.263-1995, by reference, with the exceptions listed in 25.4. Reference [2] defines the differential output voltage at the Active Output Interface (AOI) for operation over unshielded twisted pair (UTP).

The differential output voltage, V_{out}, is defined to be the intersection of the straight line best fit for amplitude with the vertical line indicating the start of the transition from 0V to V_{out}. The reference for this measurement is defined to be an output waveform consisting of 14 bit times of no transition preceded by a transition from 0V to V_{out}.

The definition of the reference waveform was made with the assumption that the DUT would be sending scrambled, MLT-3 encoded /H/ code-groups. While this is normal for an FDDI device, it is not straightforward to get a 100BASE-TX device to generate this sequence. A 100BASE-TX device normally generates scrambled, MLT-3 encoded /I/ code-groups in which one may find 12 bit times of no transition preceded by a transition from 0V to V_{out}. This waveform is adopted as the reference.

The term "straight line best fit" in the definition of V_{out} is ambiguous. First, the region over which the fit is to be made is not defined. For this measurement, the range has been chosen to be from 8ns past the point where the signal rise crosses 50% of V_{out} to 8ns before the signal fall crosses 50% of V_{out}. These points were chosen to minimize the effect that the transient response has on the "fit". Second, it is not clear from [3] that the fit is allowed to have non-zero slope. A comparable measurement made in [4] takes V_{out} to be the mean voltage at the center of the eye. For this measurement, V_{out} is taken to be mean voltage in the aforementioned range.

Note that by taking the mean voltage, the intersection of the best fit straight line with the vertical line indicating the start of the transition from 0V to V_{out} is irrelevant. This is good because depending on the waveform properties, the start of the transition may be difficult to accurately determine.

Figure 25.1.1-1 summarizes the differential output voltage measurement considerations.

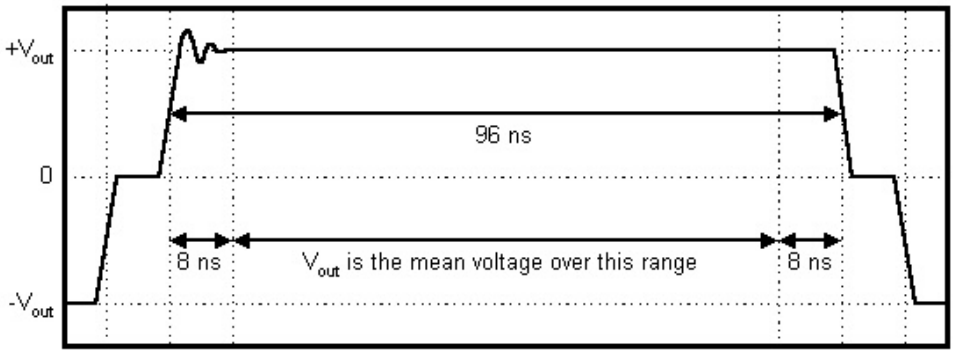


Figure 25.1.1-1: Differential output voltage reference waveform

For UTP support, the magnitude of V_{out} shall be between 950mV and 1050mV. The signal amplitude symmetry, defined as the ratio of the magnitudes of $+V_{out}$ and $-V_{out}$ shall be within the limits:

$$98\% \le \left| \frac{+V_{out}}{-V_{out}} \right| \le 102\%$$

Test Setup: Refer to Appendix 25.A.

Procedure:

1. Configure the DUT for 100BASE-TX operation. Ensure that the DUT is sending scrambled, MLT-3 encoded /I/ code-groups.
2. Configure the DSO to capture the waveform depicted in figure 25.1.1-1. Measure $+V_{out}$.
3. For enhanced accuracy, repeat step 2 multiple times and average the voltages measured at each point.
4. Configure the DSO to capture the waveform depicted in figure 25.1.1-1 but with opposite polarity. Measure $-V_{out}$.
5. For enhanced accuracy, repeat step 4 multiple times and average the voltages measured at each point.
6. Compute the signal amplitude symmetry.

Observable Results:

a. The magnitude of V_{out} shall be between 950mV and 1050mV.
b. The signal amplitude symmetry shall be between 98% and 102%.

Possible Problems: None.

Test #25.1.2 – Rise and Fall Times

Purpose: To verify that the response times of the device under test (DUT) are within the conformance limits.

References:

[1] IEEE Std 802.3-2005, clause 25
[2] ANSI X3.263-1995, section 9.1.6

Resource Requirements: Refer to Appendix 25.A

Last Modification: November 10, 2003 (Version 2.5)

Discussion:

Reference [1] describes the operation of the physical medium dependent (PMD) sublayer for 100Base-Tx devices. This clause incorporates ANSI X3.263-1995, by reference, with the exceptions listed in 25.4. Reference [2] defines the rise and fall times at the Active Output Interface (AOI).

Signal rise is defined as a transition from the baseline voltage to either $+V_{out}$ or $-V_{out}$. Signal fall is defined as a transition from either $+V_{out}$ or $-V_{out}$ to the baseline voltage. The signal rise and fall times are defined to be the time difference between the points where the signal transition crosses 10% and 90% of V_{out}.

The standard does not define a reference waveform for rise and fall time measurements. The reference waveform is chosen to be the longest pulse that follows and is followed by at least two consecutive symbols at the baseline voltage. A waveform generated in the course of transmitting scrambled, MLT-3 encoded /I/ code-groups that meets these requirements is depicted in figure 25.1.2-1. This waveform will have amplitude V_{out} as measured in test 25.1.1 and will have signal rise and fall that is minimally affected by inter-symbol interference.

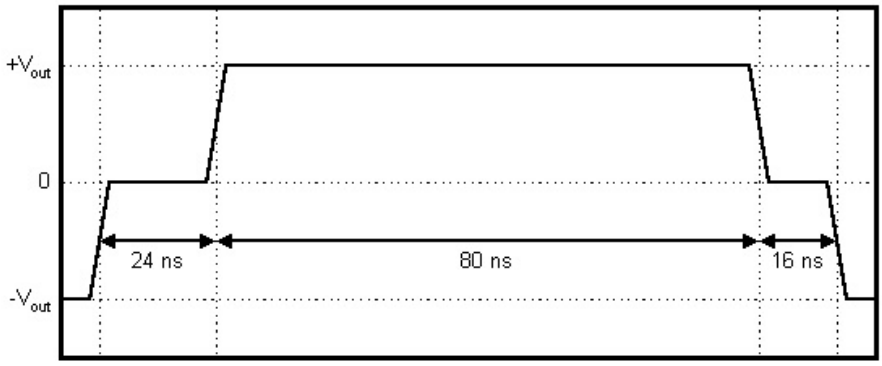


Figure 25.1.2-1: Rise and fall time reference waveform.

All measured rise and fall times shall be between 3ns and 5ns. Furthermore, the differences between all measured rise and fall times, the rise and fall time symmetry, shall not exceed 0.5ns.

Test Setup: Refer to Appendix 25.A.

Procedure:

1. Configure the DUT for 100BASE-TX operation. Ensure the DUT is transmitting scrambled, MLT-3 encoded /I/ code-groups.
2. Configure the DSO to capture the waveform depicted in figure 25.1.2-1. Measure the rise and fall times of the pulse.
3. For enhanced accuracy, repeat step 2 multiple times and average the values measured for each edge.
4. Configure the DSO to capture the waveform depicted in figure 25.1.2-1 but with opposite polarity. Measure the rise and fall times of the pulse.
5. For enhanced accuracy, repeat step 4 multiple times and average the values measured at each edge.
6. Compute the differences between all measured rise and fall times.

Observable Results:

a. All measured rise and fall times shall be between 3ns and 5ns.
b. The rise and fall time symmetry shall not exceed 0.5ns.

Possible Problems: None.

Test #25.1.3 – Duty Cycle Distortion

Purpose: To verify that the duty cycle distortion of the device under test (DUT) is below the conformance limit.

References:

[1] IEEE Std 802.3-2005, clause 25
[2] ANSI X3.263-1995, section 9.1.8

Resource Requirements: Refer to Appendix 25.A

Last Modification: November 10, 2003 (Version 2.5)

Discussion:

Reference [1] describes the operation of the physical medium dependent (PMD) sublayer for 100Base-Tx devices. This clause incorporates ANSI X3.263-1995, by reference, with the exceptions listed in 25.4. Reference [2] defines the duty cycle distortion (DCD) at the Active Output Interface (AOI).

The reference waveform for the DCD measurement is depicted in figure 25.1.3-1 (indicated pulse widths are nominal values). DCD shall be measured at the points where the four successive MLT-3 transitions generated by a 01010101 NRZ bit sequence cross 50% of V_{out}. While the 01010101 NRZ sequence occurs several times in a stream of scrambled /I/ code-groups, the MLT-3 sequence that follows and is followed by at least two consecutive symbols at the baseline voltage is chosen as the reference. This minimizes any inter-symbol interference that would affect signal rise and fall.

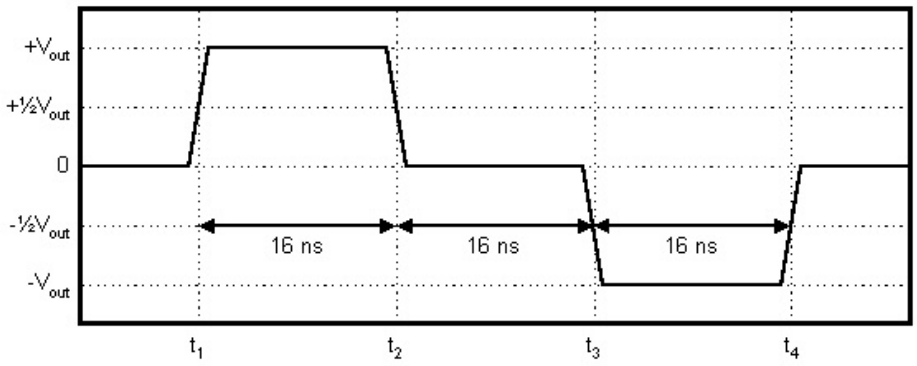


Figure 25.1.3-1: DCD reference waveform

The deviations of the 50% crossing times from a best fit grid of 16ns spacing shall not exceed ±0.25ns. This requirement is easily verified in terms of a peak-to-peak specification. Given the 50% crossing times t_n (refer to figure 25.1.3-1), compute e_m.

$e_1 = t_2 - t_1 - 16ns$
$e_2 = t_3 - t_2 - 16ns$
$e_3 = t_4 - t_3 - 16ns$
$e_4 = t_3 - t_1 - 32ns$
$e_5 = t_4 - t_2 - 32ns$
$e_6 = t_4 - t_1 - 48ns$

The peak magnitude of e_m is the peak-to-peak DCD. The peak-to-peak DCD shall not exceed 0.5ns.

Test Setup: Refer to Appendix 25.A.

Procedure:

1. Configure the DUT for 100BASE-TX operation. Ensure the DUT is transmitting scrambled, MLT-3 encoded /I/ code-groups.
2. Configure the DSO to capture the waveform depicted in figure 25.1.3-1. Measure the times at which the signal transitions cross 50% of V_{out}.
3. Compute e_1 through e_6.
4. For enhanced accuracy, repeat steps 2 and 3 multiple times and average the voltages measured at each point.
5. Compute the peak-to-peak DCD.

Observable Results: The peak-to-peak DCD shall not exceed 0.5ns.

Possible Problems: None.

Test #25.1.4 – Transmit Jitter

Purpose: To verify that the total transmit jitter of the device under test (DUT) is below the conformance limit.

References:
[1] IEEE Std 802.3-2005, clause 25
[2] ANSI X3.263-1995, sections 9.1.9
[3] ANSI X3.263-1995, annex J

Resource Requirements: Refer to Appendix 25.A.

Last Modification: November 10, 2003 (Version 2.5)

Discussion:

Reference [1] describes the operation of the physical medium dependent (PMD) sublayer for 100Base-Tx devices. This clause incorporates ANSI X3.263-1995, by reference, with the exceptions listed in 25.4. Reference [2] defines the transmit jitter at the Active Output Interface (AOI).

The ANSI standard states that the transmit jitter measurement shall be performed on scrambled, MLT-3 encoded /H/ code-groups. The transmit jitter measured, including contributions from duty cycle distortion and baseline wander, shall not exceed 1.4ns peak-to-peak. Note the subclause 25.4.5 states that the transmit jitter measurement may also be performed on scrambled, MLT-3 encoded /I/ code-groups.

Even though a reference pattern and a peak-to-peak value are defined, the transmit jitter specification is not complete. Jitter is a statistical phenomenon and a peak-to-peak value is meaningless unless it is related to some probability, usually the bit error rate (BER). Since neither the ANSI standard nor clause 25 specify a target BER for 100BASE-TX, a BER of 10^{-8} is assumed.

Also, it is not clear whether the transmit clock or a recovered clock is to be used as the timing reference. The principal difference between the two is the amount of the low frequency jitter that appears in the measurement. The recovered clock is typically generated by a phase-locked loop (PLL) which tracks jitter below its bandwidth. This is equivalent to measuring the jitter at the output of a high-pass filter. As the bandwidth of the PLL decreases, the difference between the transmit clock and the recovered clock also decreases. It is assumed that the reference for this measurement is the transmit clock. If the transmit clock is not available, a very narrow bandwidth PLL shall be used to generate the timing reference.

There are a variety of instruments and techniques that can be used to measure jitter. A DSO-based approach that does not require access to the transmit clock is presented in appendix 25.B. A popular method of visualizing jitter on the waveform is the eye mask, defined in [3]. A plot is included in the report, and while the eye diagram is a good indicator of the jitter, the value seen in the report is the peak-to-peak value, which is not obtained simply by looking at the eye diagram. In fact, the eye diagram may fail while the peak-to-peak value passes, and vice versa.

Test Setup: Refer to Appendix 25.A

Procedure:
1. Configure the DUT for 100BASE-TX operation. Ensure that the DUT is sending scrambled, MLT-3 encoded /I/ code-groups.
2. Measure the peak-to-peak transmit jitter at a BER of 10^{-8} using the method presented in appendix 25.B.

Observable Results: The peak-to-peak transmit jitter shall not exceed 1.4ns at a BER of 10^{-8}.

Possible Problems: None.

Test #25.1.5 – Waveform Overshoot

Purpose: To verify that the waveform overshoot of the device under test (DUT) is below the conformance limit.

References:
[1] IEEE Std 802.3-2005, clause 25
[2] ANSI X3.263-1995, section 9.1.3

Resource Requirements: Refer to Appendix 25.A.

Last Modification: November 10, 2003 (Version 2.5)

Discussion:

Reference [1] describes the operation of the physical medium dependent (PMD) sublayer for 100Base-Tx devices. This clause incorporates ANSI X3.263-1995, by reference, with the exceptions listed in 25.4. Reference [2] defines the waveform overshoot at the Active Output Interface (AOI).

The waveform overshoot is defined as the percentage excursion of the differential signal transition beyond its final adjusted value, V_{out}, during the symbol interval (8ns) following the signal transition. While no reference waveform is defined for the measurement, the same waveform used to measure V_{out} (refer to test 25.1.1) is assumed.

Note that the end of the signal transition may be difficult to accurately determine. A more straightforward approach is adopted which measures the peak excursion in the symbol interval following the point where the signal rise crosses 50% of V_{out}. The peak excursion is called V_{peak}.

The waveform overshoot shall not exceed 5%. In terms of V_{peak}, the following inequality shall be satisfied.

$$5\% \geq \frac{V_{peak} - V_{out}}{V_{out}} \times 100\%$$

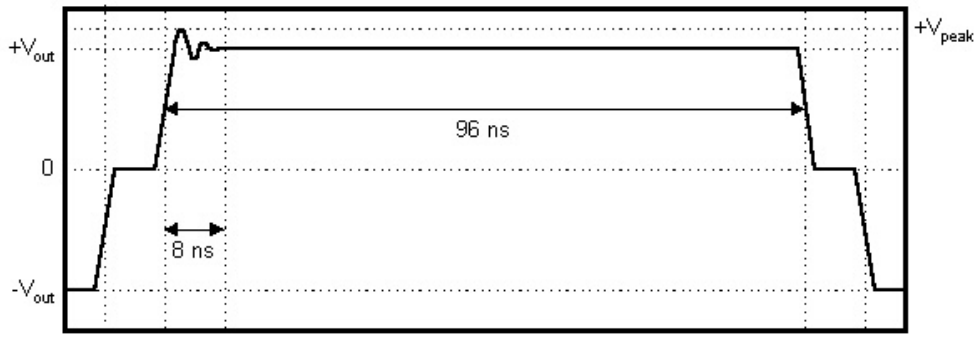


Figure 25.1.5-1: Waveform overshoot reference waveform

Test Setup: Refer to Appendix 25.A.

Procedure:

1. Configure the DUT for 100BASE-TX operation. Ensure that the DUT is sending scrambled, MLT-3 encoded /I/ code-groups.
2. Configure the DSO to capture the waveform depicted in figure 25.1.5-1. Measure $+V_{peak}$. Compute the waveform overshoot.
3. For enhanced accuracy, repeat step 2 multiple times and average the peak voltages measured.
4. Configure the DSO to capture the waveform depicted in figure 25.1.5-1 but with opposite polarity. Measure $-V_{peak}$. Compute the waveform overshoot.
5. For enhanced accuracy, repeat step 4 multiple times and average the peak voltages measured.

Observable Results: The waveform overshoot shall not exceed 5%.

Possible Problems: None.

Test #25.1.6 – Transmitter Return Loss

Purpose: To verify that the return loss at the transmitter of the device under test (DUT) is above the conformance limit.

References:

[1] IEEE Std 802.3-2005, clause 25
[2] ANSI X3.263-1995, section 9.1.5

Resource Requirements: Refer to Appendix 25.A.

Last Modification: November 10, 2003 (Version 2.5)

Discussion:

Reference [1] describes the operation of the physical medium dependent (PMD) sublayer for 100Base-Tx devices. This clause incorporates ANSI X3.263-1995, by reference, with the exceptions listed in 25.4. Reference [2] defines the return loss at the Active Output Interface (AOI).

The ANSI standard states that the return loss at the AOI shall be above the limit line depicted in figure 25.1.6-1. Return loss, as defined in test 25.2.1, is the magnitude of the reflection coefficient expressed in decibels. The reflection coefficient, Γ, is the ratio of the voltage in the reflected wave to the voltage in the incident wave. In this case, the observed reflection is the sum of the actual reflection and the voltage generated by the transmitter of the DUT. This additional voltage introduces an error into the measured reflection coefficient, Γ_e:

$$\Gamma_e = \frac{V_R + V_T}{V_I} = \Gamma + \frac{V_T}{V_I}$$

Note that V_R is the voltage in the reflected wave and V_T is the voltage transmitted by the DUT. V_I is the voltage in the incident wave. The ratio of V_T to V_I is the error in the reflection coefficient measurement. It can be shown that the resulting error in the return loss calculation is:

$$e(dB) = -20 \cdot \log_{10}\left(1 + \frac{V_T}{V_I} \cdot \frac{1}{\Gamma}\right) = -20 \cdot \log_{10}(1 + r)$$

Table 25.1.6-1 shows e as a function of r. Figure 25.1.6-1 shows that the minimum conformant return loss is 10dB, which corresponds to a reflection coefficient of 0.32. In order to assure the error in the return loss measurement does not exceed 0.5dB for any conformant return loss, the ratio of V_T to V_I must be less than $\Gamma \cdot r = 0.32 \cdot 0.05 = 0.016$. This is easily achieved for V_I greater than 100mV.

Table 25.1.6-1: Error in the return loss calculation as a function of r.

r	0.05	0.06	0.07	0.08	0.09	0.1	0.2	0.3	0.4
e (dB)	-0.42	-0.51	-0.59	-0.67	-0.75	-0.83	-1.58	-2.28	-2.92

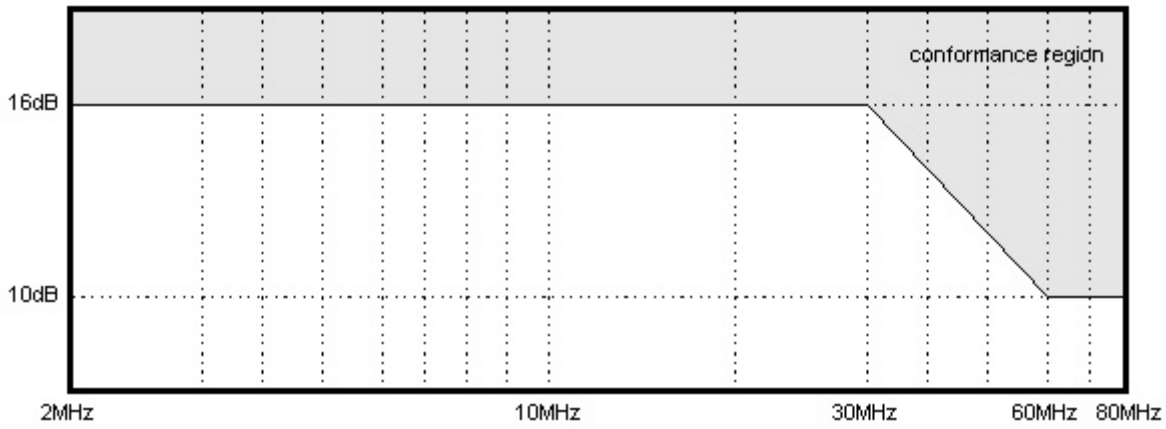


Figure 25.1.6-1: Return loss limit as a function of frequency.

As mentioned in test 25.2.1, return loss cannot be computed without a specified source impedance Z_S. Z_S is defined to be 100Ω ± 15Ω. Z_S is primarily resistive with a phase angle magnitude less than 3° in the frequency range of 2MHz to 80MHz.

Test Setup: Refer to Appendix 25.A.

Procedure:

1. Configure the DUT for 100BASE-TX operation. Ensure that the DUT is sending scrambled, MLT-3 encoded /I/ code-groups.
2. Measure the reflection coefficient at the transmitter in the frequency range of 2MHz to 80MHz.
3. Compute the return loss for a Z_S of 85Ω and a Z_S of 115Ω. Assume Z_S to be completely resistive.

Observable Results: The return loss at the AOI shall not fall below the limit line depicted in figure 25.1.6-1.

Possible Problems: None.

Test #25.1.7 – Transmitter Open Circuit Inductance

Purpose: To verify that the open circuit inductance at the transmitter of the device under test (DUT) is above the conformance limit.

References:

[1] IEEE Std 802.3-2005, clause 25
[2] ANSI X3.263-1995, section 9.1.7
[3] ANSI X3.263-1995, figure 9-2

Resource Requirements: Refer to Appendix 25.A.

Last Modification: November 10, 2003 (Version 2.1)

Discussion:

Reference [1] describes the operation of the physical medium dependent (PMD) sublayer for 100Base-Tx devices. This clause incorporates ANSI X3.263-1995, by reference, with the exceptions listed in 25.4. Reference [2] defines the open circuit inductance (OCL) at the Active Output Interface (AOI).

The ability of a 100BASE-TX receiver to track baseline wander is dependent on the worst case droop allowed by the transmitter sending the stream. This droop is a function of the OCL of the transmitter. The value of the OCL varies with bias current, temperature, and manufacturing distributions. A worst case baseline wander frame creates a DC bias in the transformer of the AOI. A minimum OCL must be maintained in the presence of this bias current, so that the change in the droop of the data frames is minimized. The standard specifies that the OCL must be at least 350 μH for any DC bias current between 0 and 8 mA.

A test setup is described in [3]. However, an alternate test setup has been devised using available equipment. Reference [3] specifies that the measurement be made with an impedance analyzer producing a 100 mV_{rms} test signal at 100 kHz. This has been substituted with an inductance meter, which takes its measurements using a 715 μA_{rms} signal at 862 Hz. As this meter is a current source, it has a significantly higher impedance than the transformer magnetics, and thus does not require the capacitor shown in [3] to block the DC bias current.

The OCL of the transformer decreases with increased bias current. Thus, it is only necessary to test conformance with a bias current of 8 mA. The current source is realized using a DC voltage supply and a current mirror.

Test Setup: Refer to Appendix 25.A.

Procedure:

1. Turn the DUT off.
2. Adjust the DC current source until the bias current through the AOI is 8.0 mA.
3. Record the OCL as measured by the inductance meter.

Observable Results: The OCL at the AOI shall be at least 350 μH when measured with an 8 mA DC bias current.

Possible Problems:

The value of the OCL is known to have some temperature dependency. In order to account for this, it is suggested that the DUT to be powered for fifteen minutes before testing to allow it to reach an operating temperature.

Test #25.1.8 – Transmit Clock Frequency

Purpose: To verify that the frequency of the Transmit Clock is within the conformance limits

References:
[1] IEEE Std 802.3-2005, clause 25
[2] Ibid., subclause 24.2.3.4, Timers

Resource Requirements: Refer to Appendix 25.A.

Last Modification: November 10, 2003 (Version 1.0)

Discussion:

Reference [1] describes the operation of the physical medium dependent (PMD) sublayer for 100Base-Tx devices. This clause incorporates ANSI X3.263-1995, by reference, with the exceptions listed in 25.4. Reference [2] defines the frequency of the fixed frequency oscillator for 100Base-Tx devices.

The reference clock used in this case is the recovered clock, which is the same one used during test 25.1.4, Transmit Jitter. After this clock has been recovered from the signal, its frequency is determined, and compared to a 125 MHz reference. The difference between the two is the deviation in the transmit clock.

The frequency of the recovered clock shall have a base frequency of 125 MHz ± 6.25 kHz.

Test Setup: Refer to Appendix 25.A.

Procedure:
1. Configure the DUT for 100BASE-TX operation. Ensure that the DUT is sending scrambled, MLT-3 encoded /I/ code-groups.
2. Measure the frequency of the clock derived from the transmitted IDLE signal and compare to 125 MHz.
3. For enhanced accuracy, repeat step 2 multiple times and average the frequencies measured.

Observable Results: The transmit clock generated by the DUT shall be 125 MHz ± 6.25 kHz

Possible Problems: None

GROUP 2: ACTIVE INPUT INTERFACE (AII)

Overview:

This group of tests verifies the integrity of the Device Under Tests' Active Input Interface. This is done by using various frame reception and physical characterization tests.

Scope:

All of the tests described in this section have been implemented and are currently active at the University of New Hampshire InterOperability Lab.

Test #25.2.1 – Differential Input Impedance

Purpose: To verify that the return loss at the receiver of the device under test (DUT) is above the conformance limit.

References:

[1] IEEE Std 802.3-2005, clause 25
[2] ANSI X3.263-1995, section 9.2.2
[3] Ibid., section 11.1.1
[5] EIA/TIA TSB-36, section 4.2

Resource Requirements: Refer to Appendix 25.A

Last Modification: November 10, 2003 (Version 2.5)

Discussion:

Reference [1] describes the operation of the physical medium dependent (PMD) sublayer for 100Base-Tx devices. This clause incorporates ANSI X3.263-1995, by reference, with the exceptions listed in 25.4. Reference [2] defines the differential input impedance at the Active Input Interface (AII).

The differential input impedance is specified in terms of return loss which is a function of Γ, the reflection coefficient. The reflection coefficient is the ratio of the voltage in a wave reflected by a load, Z_L, to the voltage in the wave incident on that load. If the source of the incident wave has an impedance Z_S, Γ is:

$$\Gamma = \frac{Z_L - Z_S}{Z_L + Z_S}$$

Since both Z_L and Z_S are complex numbers, Γ is complex. The return loss (RL) is the magnitude of Γ expressed in decibels:

$$RL(dB) = 20 \cdot \log_{10}\left|\frac{1}{\Gamma}\right|$$

Note that Γ is inverted to make the return loss greater than or equal to zero.

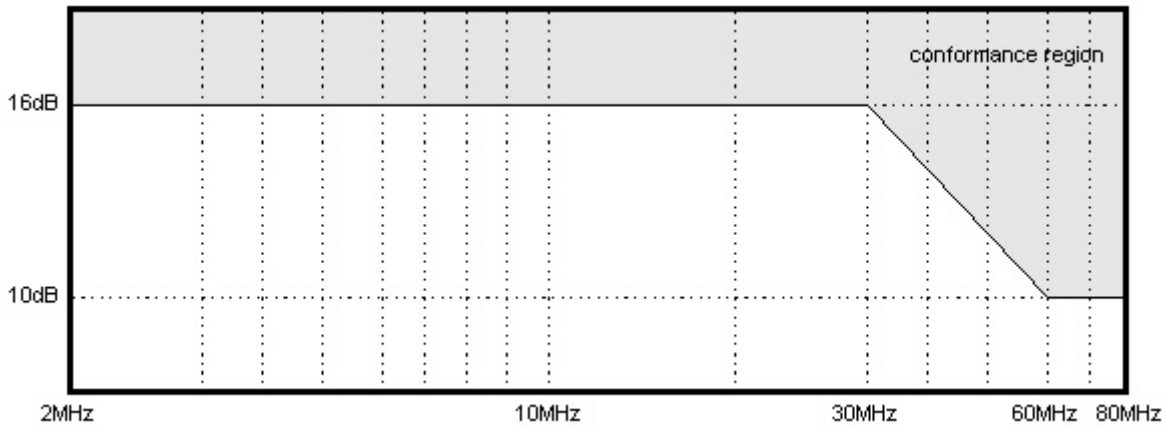


Figure 25.2.1-1: Return loss limit as a function of frequency.

The ANSI standard states that the differential input impedance shall be such that the return loss is above the limit line depicted in figure 25.2.1-1. The source impedance, Z_S, for the return loss measurement is defined to be the characteristic impedance of a twisted pair as specified in [3]. Reference [3] refers to EIA/TIA TSB-36 for the definition of category 5 unshielded twisted pair (UTP). Reference [4] states that the characteristic impedance shall be 100Ω ± 15%. Therefore, the return loss measurement is performed for both a Z_S of 85Ω and a Z_S of 115Ω. Z_S is assumed to be completely resistive.

Test Setup: Refer to Appendix 25.A.

Procedure:

1. Configure the DUT for 100BASE-TX operation.
2. Measure the impedance, Z_L, at the receiver in the frequency range of 2MHz to 80MHz.
3. Compute the return loss for a Z_S of 85Ω and a Z_S of 115Ω. Assume Z_S to be completely resistive.

Observable Results: The return loss at the AII shall not fall below the limit line depicted in figure 25.2.1-1.

Possible Problems:

In some cases, it is not possible to disable auto-crossover on the DUT. On these devices, the differential input impedance cannot be measured.

Test #25.2.2 – Adaptive Equalization

Purpose: To verify that, under worst-case operating conditions, the device under test (DUT) correctly compensates for the wide range of attenuation and phase distortion introduced by cable.

References:

[1] IEEE Std. 802.3-2005, clause 25
[2] ANSI X3.263-1995, section 9.2.1
[3] Ibid., Annex A, section A.1
[4] TIA/EIA-568-A-1995, Annex E (informative)

Resource Requirements: Refer to Appendix 25.A

Last Modification: November 10, 2003 (Version 1.1)

Discussion:

Reference [1] describes the operation of the physical medium dependent (PMD) sublayer for 100Base-Tx devices. This clause incorporates ANSI X3.263-1995, by reference, with the exceptions listed in 25.4. Reference [2] defines a set of differential input signals that must be accepted by the Active Input Interface (AII).

The differential input signals are defined to be the outputs of the test channels defined in [3]. Each test channel is driven by a differential transmitter that meets or exceeds the specifications of the section 9.1 (Active Output Interface). Five test channels are defined that represent 5, 25, 50, 75, and 100% of the maximum attenuation expected in the application environment. The NEXT loss of each test channel is defined to keep the attenuation-to-crosstalk ratio consistent among the channels.

The intention of the five test channels is to ensure that the AII correctly compensates for the wide range of attenuation and phase distortion introduced by cable. This test expands upon the differential input signals concept and addresses the problems with the specified test channels and methodology.

The first problem lies in the test channel definitions. The application environment for 100BASE-TX is expected to be category 5 cable installed according to TIA/EIA-568-A. However, a compliant TIA installation could have higher attenuation than what is represented in the worst-case test channel. The difference is due to the following factors:

a. The worst-case test channel assumes 3 category 5 connectors while TIA/EIA-568-A allows up to 4. It is interesting to note that section 11.1.8 of ANSI X3.263 also states that the channel may contain up to 4 connectors which conflicts with the worst-case channel definition given in the same standard.
b. The worst-case test channel assumes a 0.3% increase in attenuation per degree Celsius above room temperature (20^{o}C). TIA/EIA-568-A allows up to 0.4% per degree Celsius.

This test steps the attenuation from 5% to 100% of the worst-case TIA/EIA-568-A attenuation in 5% increments. Note that this test does not attempt to maintain a consistent attenuation-to-crosstalk ratio. The NEXT loss of each channel is set to the worst-case NEXT loss allowed by TIA.

The second problem is that the target bit error rate for the AII is not specified. The intention of this test is to find what levels of attenuation, if any, result in severe under- or over-equalization. Since such failures are expected to result in high error rates, this test will attempt to prove that the BER is greater than 10^{-8} for each iteration. Based on the analysis given in appendix 25.D, if more than 7 errors are observed in $3x10^{8}$ bits (about 470,000 64-byte packets), it can be concluded that the error rate is greater than 10^{-8} with less than a 5% chance of error. Note that if no errors are observed, it can be concluded that the BER is no more than 10^{-8} with less than a 5% chance of error.

This test is repeated for transmitter response times of 3 and 5ns. A response time of 3ns maximizes the signal bandwidth while a response time of 5ns results in the worst-case quantization error for digital implementations.

Table 25.2.2-1 summarizes the model parameters used in this test in the context of the link model defined in appendix 25.C.

Table 25.2.2-1: Summary of model parameters for test #25.2.2

Parameter	Description	Value	Units
J_{pp}	Peak-peak jitter	1.4	ns
t_r	Response time	3 (5)	ns
%OS	Waveform overshoot	5	%
R_S	Transmitter source impedance	100	Ω
R_L	Receiver load impedance	100	Ω
L_1	Transmitter open circuit inductance	350	μH
L_2	Receiver open circuit inductance	350	μH
R_{WG}	Waveform generator source impedance	100	Ω
R_{DUT}	DUT load impedance	100	Ω
L_{DUT}	DUT open circuit inductance	measured in test #25.1.7	μH
l	Cable length	5 to 100 in increments of 5	m
T	Temperature	60	°C
V_{out}	Differential output voltage	950	mV
C	Number of connectors in the channel	4	—
M	Flat loss margin	0.3	dB
N_B	Reference NEXT loss (at 16MHz)	40.5	dB
N_M	NEXT loss scale	16.6	$^{dB}/_{decade}$

Test Setup: Refer to Appendix 25.A.

Procedure:

1. Configure the link simulator to use the model parameters in table 25.2.2-1 with a response time of 3ns and cable length of 5m. The link simulator will send 500,000 64-byte packets and the monitor will count the number of packet errors.
2. Repeat step 1, incrementing the cable length by 5m with each iteration, until the cable length reaches 100m.
3. Repeats steps 1 and 2 for a response time of 5ns.

Observable Results: There shall be no more than 7 errors for any iteration.

Possible Problems:

The rate at which the device under test can process incoming packets may make the test duration prohibitive. In such cases, fewer packets may be sent resulting in a lower confidence that a bit error rate of 10^{-8} is being met.

Test #25.2.3 – Baseline Wander Correction

Purpose: To verify that the device under test (DUT) can correct worst-case baseline wander events.

References:

[1] IEEE Std. 802.3-2005, clause 25
[2] ANSI X3.263-1995, section 9.2.1
[3] Ibid., Annex A, section A.1
[4] Ibid., Annex A, section A.2
[5] TIA/EIA-568-A-1995, Annex E (informative)

Resource Requirements: Refer to Appendix 25.A

Last Modification: November 10, 2003 (Version 1.1)

Discussion:

The operation of the 100BASE-TX PMD sublayer is defined in [1]. Clause 25 incorporates ANSI X3.263 by reference with the exceptions listed in subclause 25.4. Reference [2] defines a set of differential input signals that must be accepted by the Active Input Interface (AII).

The differential input signals specification is intended to ensure that the AII correctly compensates for the wide range of attenuation and phase distortion introduced by cable. The test expands upon the differential input signals concept by verifying that the AII also corrects worst-case baseline wander events.

As the baseline wander model in appendix 25.C shows, the order of the channel's low frequency response is a function of cable length. The channel response is first-order highpass for a cable length of zero and second-order highpass for cable lengths greater than zero. This test applies the extreme cases of 0m and 100m cable lengths.

For each cable length, two baseline wander patterns are applied to the AII. Note that these patterns will generate the worst-case baseline wander event if, at the first bit of the pattern, the scrambler seed is 390 and the MLT-3 output symbol is 0.

Test Pattern #1: This pattern is given in annex A, section A.2 of ANSI X3.263 but has been truncated to fit in a 1,518-byte packet. It creates a worst-case unidirectional baseline wander event.

Test Pattern #2: This is a modified version of test pattern 1 which has been altered to flip the polarity of the baseline wander at one-quarter and three-quarters of the pattern length. This creates the worst-case bi-directional baseline wander event.

There is no specification for the bit error rate that the AII is expected to maintain in the presence of worst-case baseline wander events. It is expected that incorrect compensation will result in a high error rate and that a rigorous BER measurement is not required. This test will attempt to prove that the BER is greater than 10^{-8} for each iteration. Based on the analysis given in appendix 25.D, if more than 7 errors are observed in $3x10^{8}$ bits (about 20,000 1518-byte packets), it can be concluded that the error rate is greater than 10^{-8} with less than a 5% chance of error. Note that if no errors are observed, it can be concluded that the BER is no more than 10^{-8} with less than a 5% chance of error.

Each test is repeated for transmitter response times of 3 and 5ns. A response time of 3ns maximizes the signal bandwidth while a response time of 5ns results in the worst-case quantization error for digital implementations.

Table 25.2.3-1 summarizes the model parameters used in this test in the context of the link model defined in appendix 25.C.

Table 25.2.3-1: Summary of model parameters for first and second order high-pass responses.

Parameter	Description	1st Order	2nd Order	Units
J_{pp}	Peak-peak jitter	1.4	1.4	ns
t_r	Response time	3 (5)	3 (5)	ns
%OS	Waveform overshoot	5	5	%
R_S	Transmitter source impedance	100	100	Ω
R_L	Receiver load impedance	100	100	Ω
L_1	Transmitter open circuit inductance	350	350	μH
L_2	Receiver open circuit inductance	350	350	μH
R_{WG}	Waveform generator source impedance	100	100	Ω
R_{DUT}	DUT load impedance	100	100	Ω
L_{DUT}	DUT open circuit inductance	measured in test #25.1.7		μH
l	Cable length	0	100	m
T	Temperature	60	60	°C
V_{out}	Differential output voltage	950	950	mV
C	Number of connectors in the channel	0	4	—
M	Flat loss margin	0.3	0.3	dB
N_B	Reference NEXT loss (at 16MHz)	40.5	40.5	dB
N_M	NEXT loss scale	16.6	16.6	$^{dB}/_{decade}$

Test Setup: Refer to Appendix 25.A.

Procedure:

1. Configure the link simulator to use the model parameters given in table 25.2.3-1 (1st order column) with a response time of 3ns.
2. The link simulator will send 20,000 1,518-byte packets containing test pattern #1. The monitor will count the number of packet errors.
3. The link simulator will send 20,000 1,518-byte packets containing test pattern #2. The monitor will count the number of packet errors.
4. Repeat steps 1 through 3 after configuring the link simulator to use the model parameters given in table 25.2.3-1 (2nd order column) with a response time of 3ns.
5. Repeat steps 1 through 4 with a response time of 5ns.

Observable Results: There shall be no more than 7 errors for any iteration.

Possible Problems:

The rate at which the device under test can process incoming packets may make the test duration prohibitive. In such cases, fewer packets may be sent resulting in a lower confidence that a bit error rate of 10^{-8} is being met.

Test #25.2.4 – Bit Error Rate Verification

Purpose: To verify that the device under test (DUT) can maintain low bit error rate even in the presence of the worst-case input signal-to-noise ratio.

References:

[1] IEEE Std. 802.3-2005, clause 25
[2] ANSI X3.263-1995, section 9.2.1
[3] Ibid., Annex A, section A.1
[4] TIA/EIA-568-A-1995, Annex E (informative)

Resource Requirements: Refer to Appendix 25.A

Last Modification: November 10, 2003 (Version 1.1)

Discussion:

The operation of the 100BASE-TX PMD sublayer is defined in [1]. Clause 25 incorporates ANSI X3.263 by reference with the exceptions listed subclause 25.4. Reference [2] defines a set of differential input signals that must be accepted by the Active Input Interface (AII).

The differential input signals specification is intended to ensure that the AII correctly compensates for the wide range of attenuation and phase distortion introduced by cable. While test 25.2.2 performs a thorough evaluation of the adaptive equalizer circuit, it only verifies a relatively high bit error rate. This test attempts to verify a much lower bit error rate in the presence of poor signal-to-noise ratio. Specifically, the bit error rate is verified for cable lengths of 75 and 100m.

Note that the bit error rate target for 100BASE-TX is not specified in either IEEE Std. 802.3-2005 or ANSI X3.263. This test will attempt to prove that the BER is greater than 10^{-11} for each iteration. Based on the analysis given in appendix 25.D, if more than 7 errors are observed in $3x10^{11}$ bits (about 19,770,000 1,518-byte packets), it can be concluded that the error rate is greater than 10^{-11} with less than a 5% chance of error. Note that if no errors are observed, it can be concluded that the BER is no more than 10^{-11} with less than a 5% chance of error.

This test is repeated for transmitter response times of 3 and 5ns. A response time of 3ns maximizes the signal bandwidth while a response time of 5ns results in the worst-case quantization error for digital implementations.

Table 25.2.4-1 summarizes the model parameters used in this test in the context of the link model defined in appendix 25.C.

Table 25.2.4-1: Summary of model parameters for test #25.2.4

Parameter	Description	Value	Units
J_{pp}	Peak-peak jitter	1.4	ns
t_r	Response time	3 (5)	ns
%OS	Waveform overshoot	5	%
R_S	Transmitter source impedance	100	Ω
R_L	Receiver load impedance	100	Ω
L_1	Transmitter open circuit inductance	350	μH
L_2	Receiver open circuit inductance	350	μH
R_{WG}	Waveform generator source impedance	100	Ω
R_{DUT}	DUT load impedance	100	Ω
L_{DUT}	DUT open circuit inductance	measured in test #25.1.7	μH
l	Cable length	75 and 100	m
T	Temperature	60	°C
V_{out}	Differential output voltage	950	mV
C	Number of connectors in the channel	4	—
M	Flat loss margin	0.3	dB
N_B	Reference NEXT loss (at 16MHz)	40.5	dB
N_M	NEXT loss scale	16.6	$^{dB}/_{decade}$

Test Setup: Refer to Appendix 25.A.

Procedure:

1. Configure the link simulator to use the model parameters defined in table 25.2.4-1 with a response time of 3ns and a cable length of 75m.
2. The link simulator shall send 20,000,000 1,518-byte packets and the monitor will count the number of packet errors.
3. Repeat steps 1 and 2 for a cable length of 100m.
4. Repeat steps 1 through 3 for a response time of 5ns.

Observable Results: There shall be no more than 7 errors for any iteration.

Possible Problems:

The rate at which the device under test can process incoming packets may make the test duration prohibitive. In such cases, fewer packets may be sent resulting in a lower confidence that a bit error rate of 10^{-11} is being met.

TEST SUITE APPENDICES

Overview:

The appendices contained in this section are intended to provide additional low-level technical details pertinent to specific tests defined in this test suite. Test suite appendices often cover topics that are beyond the scope of the standard, but are specific to the methodologies used for performing the measurements covered in this test suite. This may also include details regarding a specific interpretation of the standard (for the purposes of this test suite), in cases where a specification may appear unclear or otherwise open to multiple interpretations.

Scope:

Test suite appendices are considered informative, and pertain only to tests contained in this test suite.

Appendix 25.A – Test Setup Implementation Examples

Purpose: To present an example of the test setups and connecting hardware that may be used to implement the 100BASE-TX PMD test suite.

References:

[1] IEEE Std 802.3-2005, clause 25
[2] ANSI X3.263-1995, section 9.1

Resource Requirements:

- Digital storage oscilloscope, Tektronix TDS7104 or equivalent
- Vector Network Analyzer, HP 8753C or equivalent
- Test Jigs #1, #2, #3
- 100Base-Tx Idle Source
- DC Power Supply (1A)
- DC Current Meter
- Inductance Meter
- Netcom Systems Smartbits
- Controlling software (MATLAB)

Last Modification: May 16, 2005 (Version 1.2)

Discussion:

25.A.1 – Introduction

This appendix describes of the implementation of the 100BASE-TX PMD test suite used by the University of New Hampshire. This description is intended to be an example for those that wish to implement the test suite in their own lab.

Note that in the cases where specific equipment models are specified, any piece of equipment with similar capabilities may be substituted. Also note that the length of the unshielded twisted pair (UTP) cable used to connect the device under test (DUT) to the test jig should be kept as short as possible (less than a foot). If longer lengths are necessary, the impact of the cable on the measurement must be evaluated and steps taken to remove its effect.

25.A-2 – Test Setup Examples

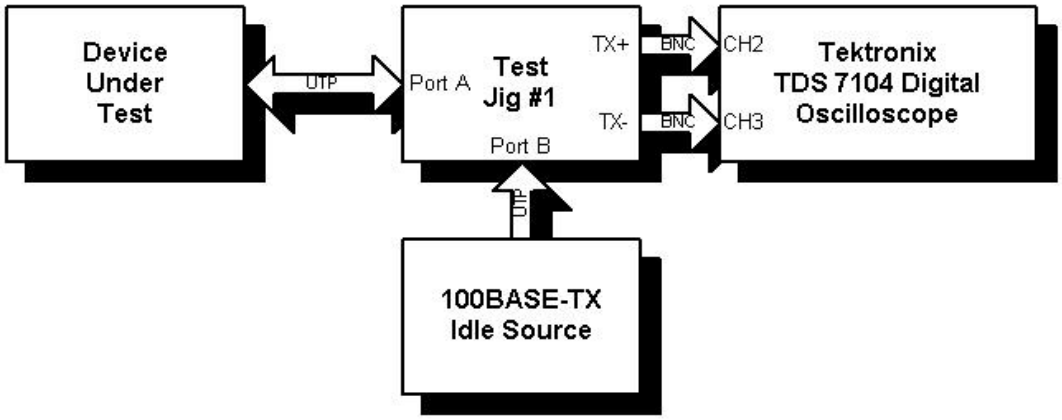


Figure 25.A-1: Example test setup for tests 25.1.1 through 25.1.5 (pulse parameters and transmit jitter).

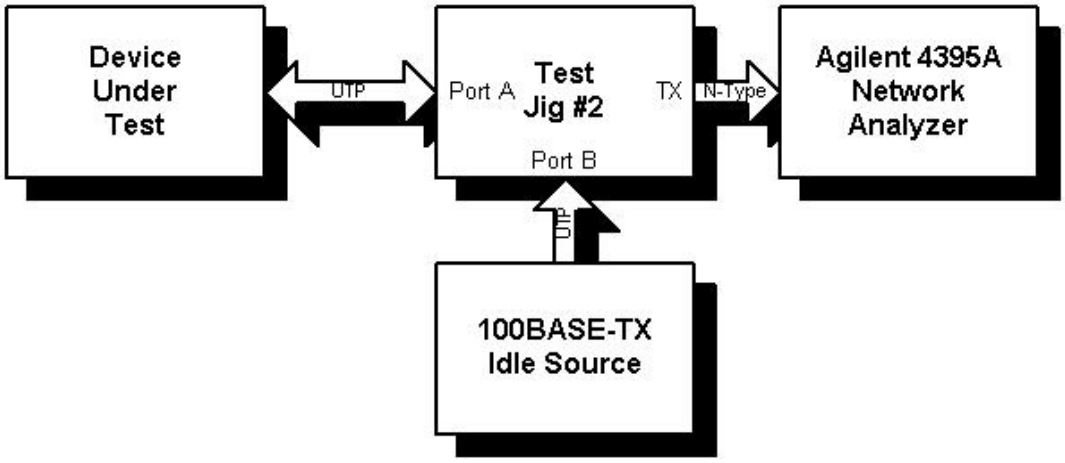


Figure 25.A-2: Example test setup for tests 25.1.6 and 25.2.1 (return loss).

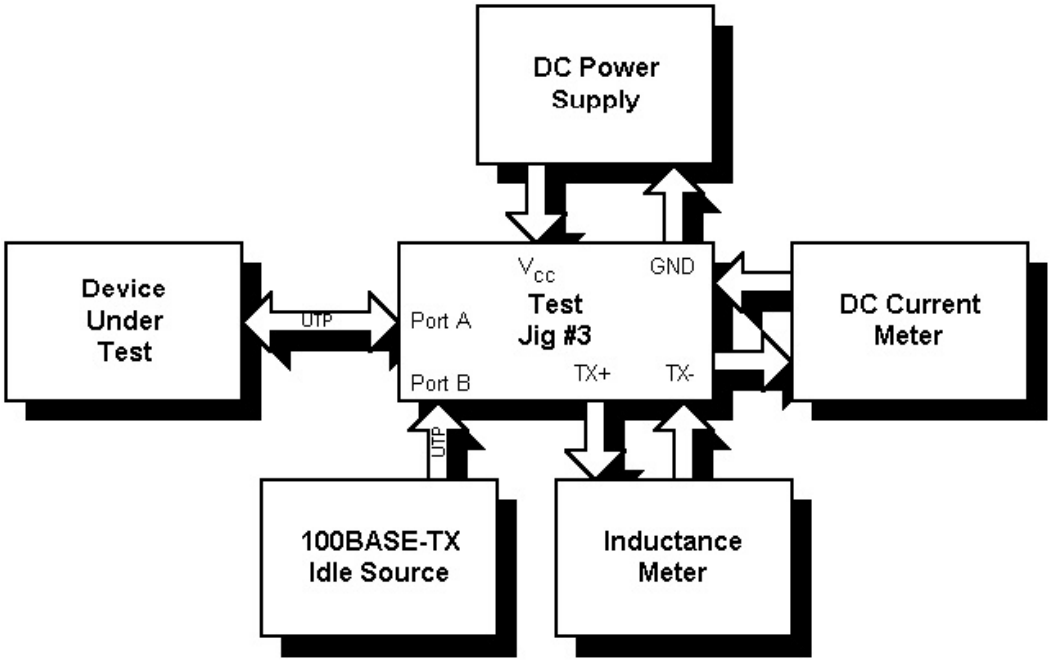


Figure 25.A-3: Example test setup for test 25.1.7 (transmitter open circuit inductance).

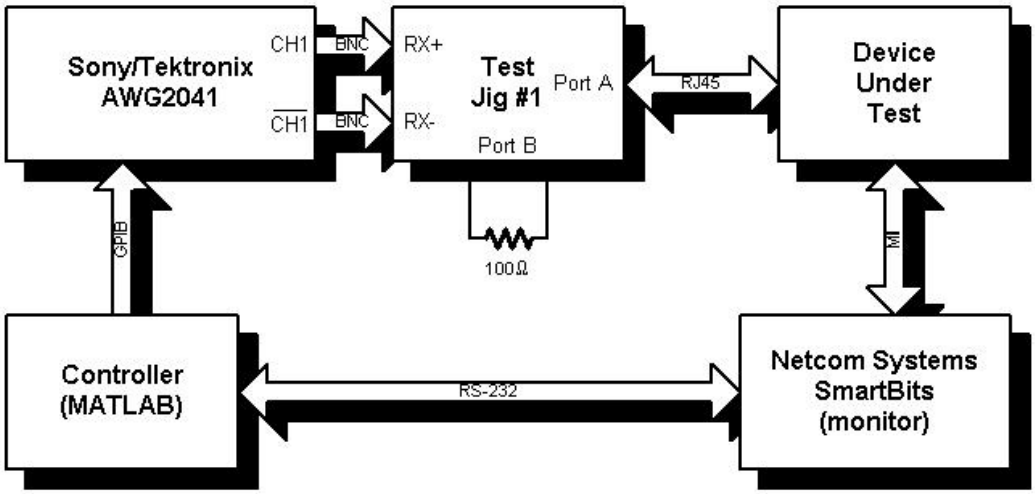


Figure 25.A-4: Example test setup for tests 25.2.2 through 25.2.4 (Active Input Interface tests, DUT is an MII transceiver).

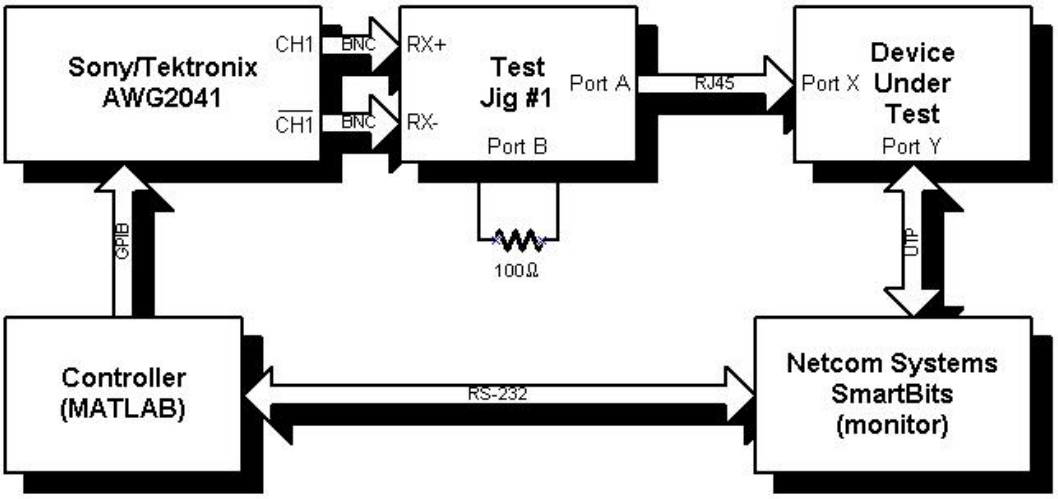


Figure 25.A-5: Example test setup for tests 25.2.2 through 25.2.4 (Active Input Interface tests, DUT is a repeater, switch, router or other packet forwarding device).

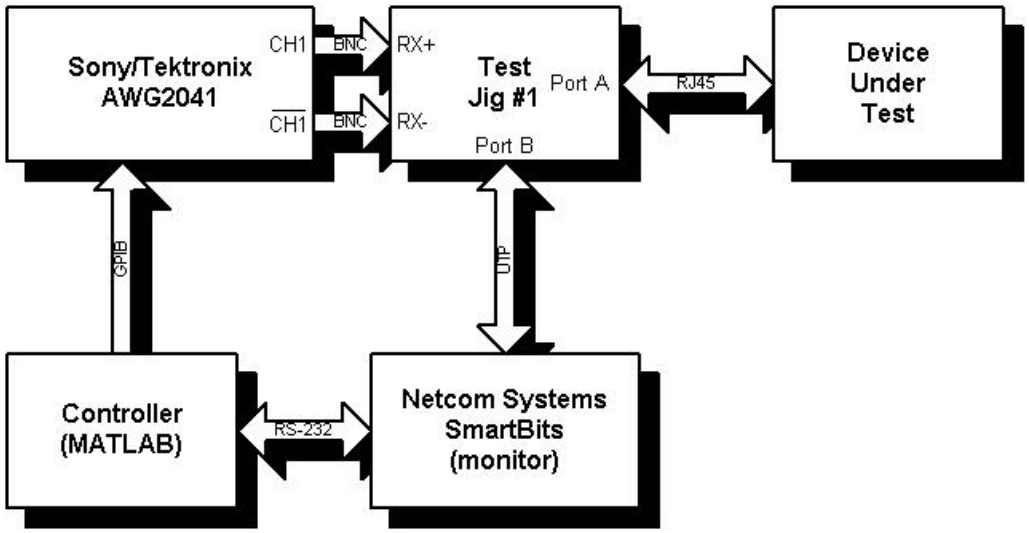


Figure 25.A-6: Example test setup for tests 25.2.2 through 25.2.4 (Active Input Interface tests, DUT is a workstation or other single port device).

25.A.3 – Example connecting hardware for test setups (test jigs)

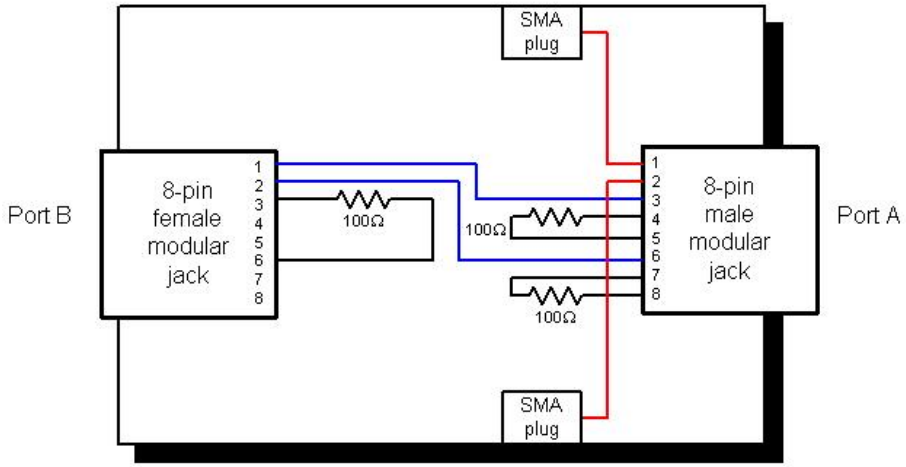


Figure 25.A-7: Test jig #1

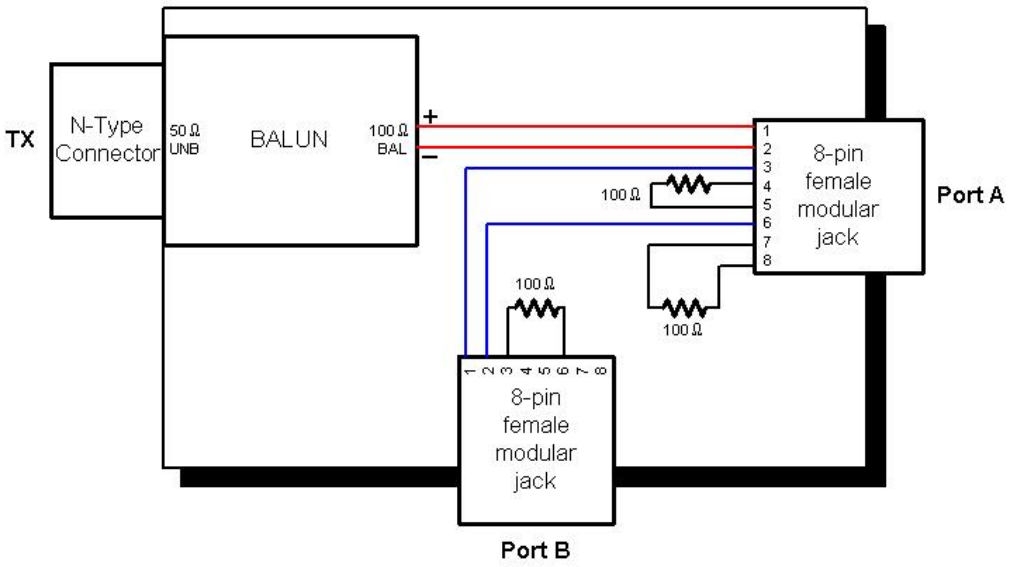


Figure 25.A-8: Test jig #2

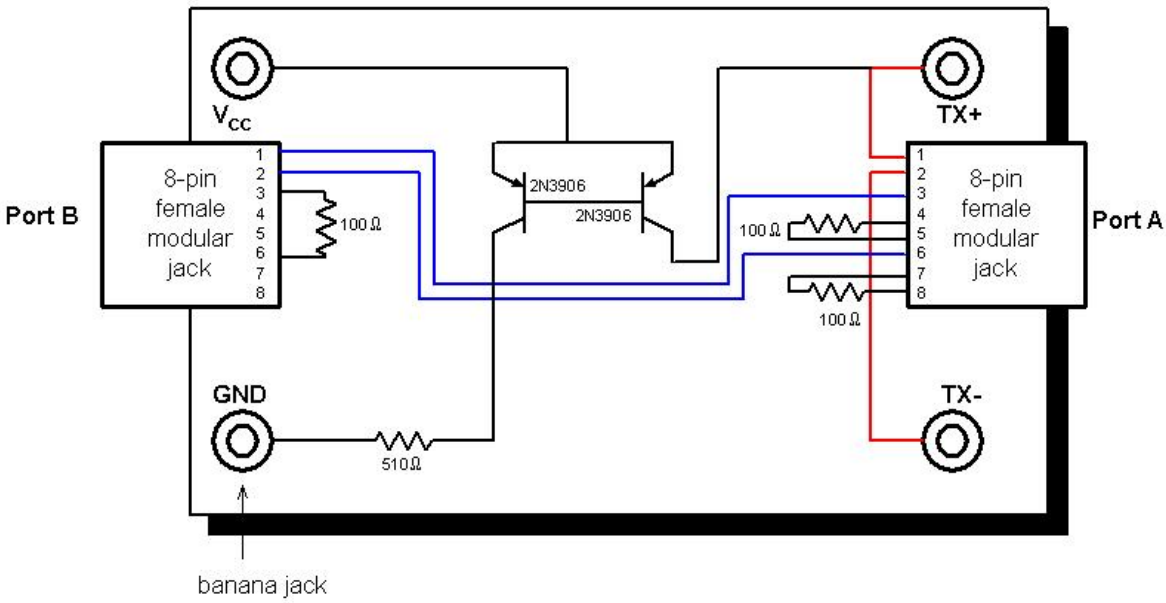


Figure 25.A-9: Test jig #3

Appendix 25.B – Transmit Jitter Measurement

Purpose: To present a method of jitter measurement that does not require access to the transmit clock.

References:

[1] IEEE Std. 802.3-2005, subclause 24.2.3.4 – Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) Sublayer, type 100BASE-X, Timers.
[2] IEEE Std. 802.3-2005, clause 25 – Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-TX.
[3] ANSI X3.263-1995, section 9.1.9 – Jitter.
[4] T11.2/Project 1230/Revision 7.0 – Methodology for Jitter Specification.

Last Modification: February 15, 1999 (Version 1.0)

Discussion:

25.B.1 – Introduction

Jitter is the difference between the time that an event was expected to occur and the time that the event actually occurred. In the context of a digital communications link, jitter is the offset between the expected position of a signal transition and the actual position of the transition. The magnitude of these offsets must be limited in order to limit the chances of an error on the link.

To measure jitter, the expected position of the signal transition must be known. The reference clock provides an indication of where a transition is supposed to occur. In a typical jitter measurement, the clock input to the transceiver under test is used as the reference clock. However, this signal is not always available. This appendix presents a reliable method of jitter measurement that derives the reference clock directly from the MLT-3 symbol sequence.

25.B.2 – Transmit Jitter Model

Jitter can be thought of as phase modulation of the MLT-3 symbol sequence. The modulation function has independent deterministic and random components. Deterministic jitter is attributed to inter-symbol interference (ISI), duty cycle distortion, and sinusoidal frequency modulation. ISI describes the pulse distortions caused by the bandwidth limitations of the system. The distortion is a function of the pulses that precede and follow pulse of interest and thus is often referred to as data-dependent jitter (DDJ).

Duty cycle distortion (DCD), as measured in test 25.1.3, is peak-to-peak deviation of the measured symbol interval from its expected value. While all jitter components alter the measured symbol interval, DCD is a static deviation that is a function of difference between the propagation of signal rise and fall. The distribution of DDJ is influenced by DCD.

Further modulation of the baseband signal is caused by the coupling of sinusoidal signals into the phase-locked loop circuit. Usually this modulation is from low frequency signals that sneak in through the power supply. Since there is no clear relationship between this form of jitter and the MLT-3 symbol sequence, it is typically referred to as uncorrelated deterministic jitter (UDJ).

Random jitter is modeled as white noise. An offset whose amplitude is picked from a zero-mean normal distribution is applied to each signal transition. The offsets are assumed to be independent, that is, the amplitude of the current offset is not influenced by the amplitudes of the preceding or following offsets. Random jitter is typically characterized by the standard deviation of the distribution from which the amplitudes are drawn. Note that a peak-to-peak value for the random jitter cannot be computed without first setting the probability that the given

value will be exceeded. Given that probability, the peak-to-peak random jitter is a function of the standard deviation.

Given the probabilistic nature of random jitter, it is useful to also model deterministic jitter with a distribution function. The total jitter distribution then becomes the convolution of the deterministic and random distributions. This concept is illustrated in figure 25.B-1.

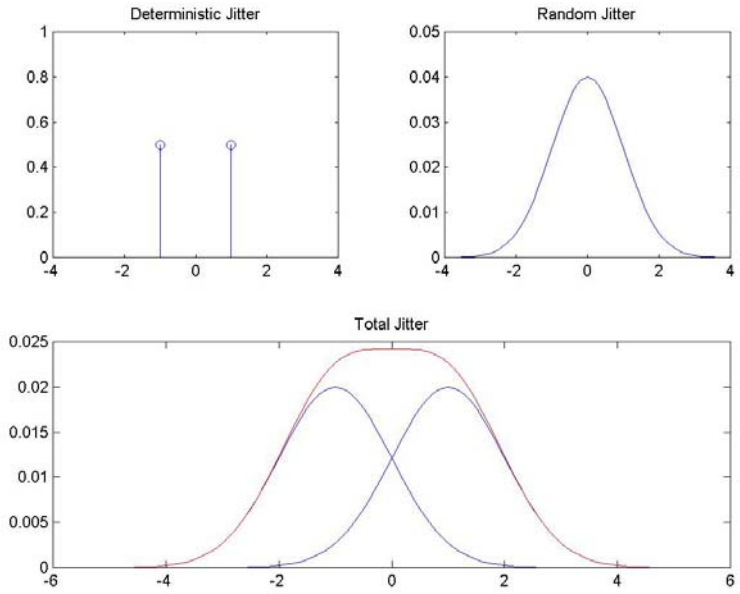


Figure 25.B-1: The total jitter distribution is the convolution of the deterministic and random distributions.

The measurement technique presented in this appendix assumes that the dominant contributions to the deterministic jitter are data-dependent jitter and duty cycle distortion. This implies that for a repeating sequence of N MLT-3 symbols, there can be no more than N distinct values for the deterministic jitter. Since the random jitter distribution is assumed to be zero-mean, the deterministic jitter value for a given signal transition is the mean jitter observed in that transition. The deterministic jitter distribution is simply a histogram of the N deterministic jitter values.

25.B.3 – Derivation of Reference Clock

The reference clock indicates where a signal transition is supposed to occur. The period of the reference clock is referred to as the unit interval (UI) and it is the duration of one MLT-3 symbol. This measurement technique derives the unit interval directly from the symbol sequence. The derivation assumes that the UI is constant over the interval of estimation.

Refer to figure 25.B-2. Let t_n be the time a signal transition crosses 50% of the differential output voltage, V_{out}. If t_1 is the position of the first signal transition, then the subscript n can be computed using equation 25.B-1.

$$n = \text{round}\left(\frac{t_n - t_1}{8\text{ns}}\right) \qquad \text{(Equation 25.B-1)}$$

Note that 8ns is the nominal unit interval. Equation 25.B-1 is incorrect if $(t_n – t_1)/(n–1)$ differs from the nominal unit interval by more than 4ns. Such a difference is caused by deviation of the actual unit interval from the

nominal value and the difference between the jitter in the first and n[th] transitions. The actual UI of a conformant device will not deviate from the nominal value by more than 0.005%. Assuming that the difference between the jitter in the first and n[th] transitions is less than 1.4ns, the worst-case UI will make equation 25.B-1 invalid for n less than 6,500.

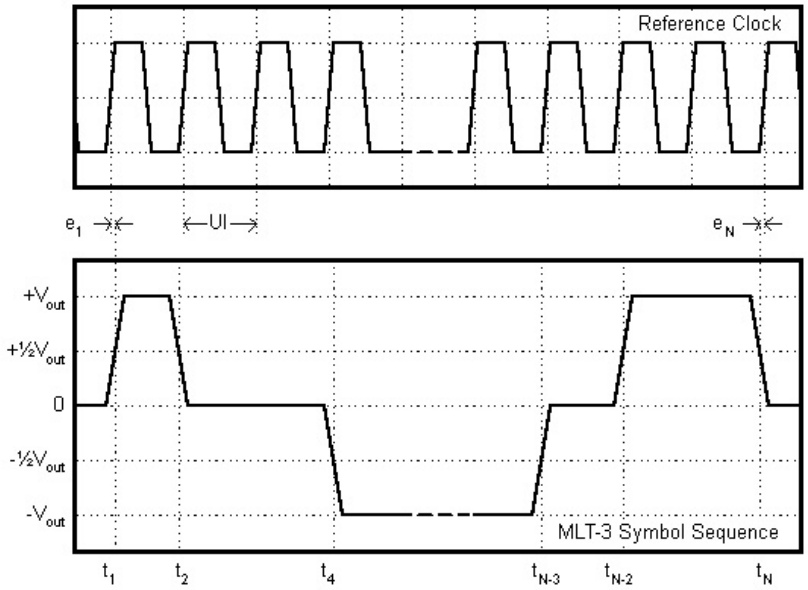


Figure 25.B-2: MLT-3 symbol sequence and corresponding reference clock.

Let N be the last signal transition in the record. Assuming that N is less than 6,500, the difference between the positions of the first and N[th] transitions is given as equation 25.B-2.

$$t_N - t_1 = (N-1)UI + e_N - e_1 \qquad \text{(Equation 25.B-2)}$$

Divide equation 25.B-2 by (N–1) to produce equation 25.B-3.

$$\frac{t_N - t_1}{N-1} = UI + \frac{e_N - e_1}{N-1} \qquad \text{(Equation 25.B-3)}$$

Thus, we have produced an estimate of the unit interval whose error is proportional to the difference between the jitter in the first and N[th] transitions. The estimate is formally stated in equation 25.B-4.

$$UI_{est} = \frac{t_N - t_1}{N-1} = UI + \frac{e_N - e_1}{N-1} \qquad \text{(Equation 25.B-4)}$$

25.B.4 – Computation of the Timing Error

An estimate of the time offset at each signal transition, $e_{n,est}$, is given in equation 25.B-5.

$$e_{n,est} = t_n - (n-1)UI_{est} \qquad \text{(Equation 25.B-5)}$$

Substituting equation 25.B-4 into equation 25.B-5 gives us equation 25.B-6.

$$e_{n,est} = t_n - (n-1)UI - (n-1)\frac{e_N - e_1}{N-1}$$ (Equation 25.B-6)

Manipulating equation 25.B-3 and making is applicable to all n, we produce equation 25.B-7.

$$t_n - (n-1)UI = t_1 + e_n - e_1$$ (Equation 25.B-7)

Substituting back into equation 25.B-6 gives us equation 25.B-8.

$$e_{n,est} = t_1 + e_n - e_1 - (n-1)\frac{e_N - e_1}{N-1}$$ (Equation 25.B-8)

Thus, the estimate of the jitter in the n^{th} signal transition contains an error term that is a linear function of n. Figure 25.B-3 shows $e_{n,est}$ as a function of n. In the figure, the error slope $(e_N–e_1)/(N–1)$ is labeled m and the error intercept $(t_1–e_1)$ is labeled b.

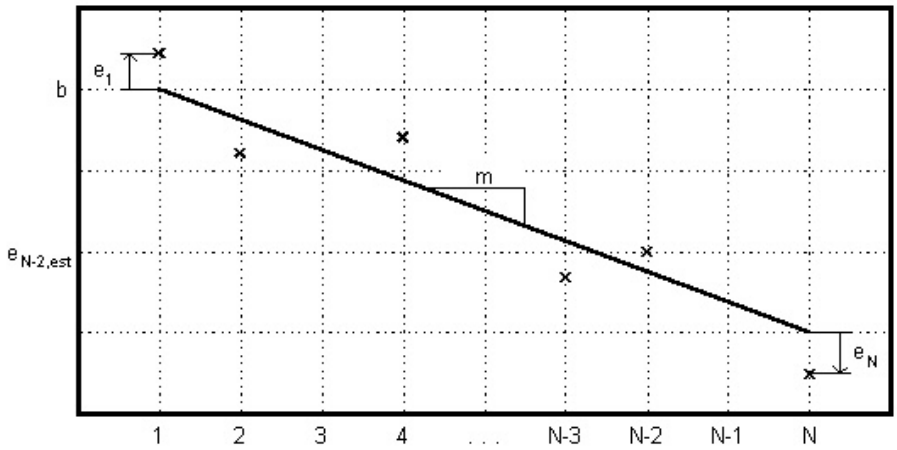


Figure 25.B-3: Estimated jitter as a function of n.

The slope and intercept of the error term are functions of the unknowns e_1 and e_N. Assuming that the total jitter distribution has a mean value of zero, m and b may be found by performing a least squares line fit to the estimated jitter. Given m and b, the actual jitter in the nth transition can be computed using equation 25.B-9.

$$e_n = e_{n,est} - b + (n-1)m$$ (Equation 25.B-9)

25.B.5 – Jitter Statistics

For each value of n, the mean and standard deviation of the jitter are estimated. The mean is the value of the deterministic jitter for that signal transition. The standard deviation completely characterizes the random jitter for that transition. If K samples of e_n are taken, the mean value of e_n can be estimated using equation 25.B-10.

$$m_n = \frac{1}{K}\sum_{k=1}^{K} e_{n,k}$$ (Equation 25.B-10)

The variance, which is the standard deviation squared, can be estimated using equation 25.B-11.

$$s_n^2 = \frac{1}{(K-1)} \sum_{k=1}^{K} (e_{n,k} - m_n)^2$$ (Equation 25.B-11)

25.B.6 – Computation of Total Transmit Jitter

The reference pattern for the transmit jitter measurement is scrambled, MLT-3 encoded, /I/ code-groups. This pattern repeats once every 8,188 symbols and it contains 4,092 signal transitions. This implies that there are no more than 4,092 distinct values for data-dependent jitter. It has been assumed that data-dependent jitter and duty cycle distortion are the dominant contributors to deterministic jitter. If this is the case, then there are no more than 4,092 distinct values for deterministic jitter.

Thus, a deterministic jitter distribution can be constructed by measuring the mean at each of the MLT-3 transitions in the pattern and building a histogram. The total jitter distribution is the convolution of this histogram and a zero-mean normal distribution function. The standard deviation of the normal distribution is the value estimated from one of the signal transitions.

Since the jitter has a random component, a peak-to-peak total jitter value cannot be computed without specifying the probability that the value will be exceeded. Referring to figure 25.B-4, the probability that a given peak-to-peak value will be exceeded is the area under the tails of the distribution (the shaded regions).

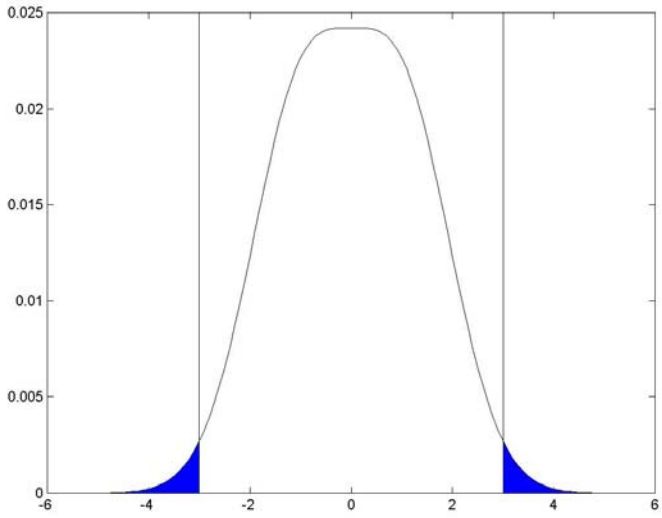


Figure 25.B-4: Peak-to-peak total jitter.

Appendix 25.C – Link Model

Purpose: To define comprehensive models of the TP-PMD transmitter and channel.

References:

[1] ANSI X3.263-1995, section 9.1.7 – Worst Case Droop of Transformer.
[2] Ibid., section 9.1.10 – Characteristics of Active Output Interface.
[3] Ibid., section 11.1.2 – Insertion Loss Definitions.
[4] Ibid., section 11.1.3 – Crosstalk Definitions.
[5] Ibid., section 11.1.4 – Reference Insertion Loss and Reference Crosstalk Attenuation Values.
[6] Ibid., Annex A.1 (normative) – Test channel requirements (twisted pair model)
[7] ANSI/TIA/EIA-568-A-1995, section 10.2.4.1 – DC Resistance (Horizontal UTP Cable).
[8] Ibid., section 10.2.4.6 – Attenuation (Horizontal UTP Cable).
[9] Ibid., section 10.2.4.7 – Near End Crosstalk (NEXT) Loss (Horizontal UTP Cable).
[10] Ibid., section 10.4.4.1 – Attenuation (Connecting Hardware for UTP Cable).
[11] Ibid., section 10.4.4.2 – NEXT Loss (Connection Hardware for UTP Cable).
[12] Ibid., section 10.5.4.1 – Attenuation (UTP Patch Cords and Cross-Connect Jumpers).
[13] Ibid., Annex E (informative) – UTP Channel Performance.

Last Modification: May 16, 2005 (Version 1.1)

Discussion:

25.C.1 – Introduction

Figure 25.C-1 shows a block diagram of the link model used in test #25.2.2 – Adaptive Equalization, test #25.2.3 – Baseline Wander Correction, and test #25.2.4 – Bit Error Rate Verification. Each component of the block diagram is described below.

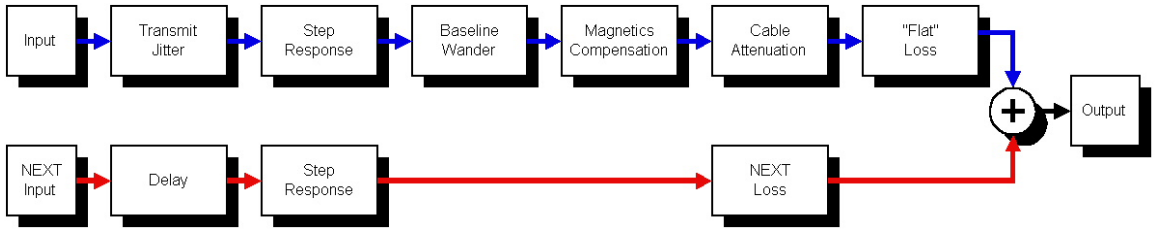


Figure 25.C-1: Link model block diagram

25.C.2 – Transmit Jitter

The transmit jitter model applies a random timing offset to each MLT-3 transition. The amplitude of the offset is chosen from zero-mean uniform probability distribution function. While jitter is typically modeled with a normal distribution function, this model uses a uniform distribution so that larger amplitudes are chosen more frequently.

A sequence of numbers, **x**, produced by a uniform random number generator can be converted to a sequence of suitable timing offsets, **e**, using equation 25.C-1.

$$\mathbf{e} = J_{pp} \frac{\mathbf{x} - \text{mean}(\mathbf{x})}{\max(\mathbf{x}) - \min(\mathbf{x})}$$ (Equation 25.C-1)

Equation 25.C-1 guarantees that the transmit jitter will have zero mean and a peak-peak value of J_{pp}. Note that J_{pp} is specified to be less than 1.4ns [2].

25.C.3 – Transmitter Step Response

The step response of an MLT-3 line driver is modeled as a second-order lowpass filter. The transfer function of this filter is given in equation 25.C-2.

$$H_{lp} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$ (Equation 25.C-2)

Note that s is shorthand for $j2\pi f$ where j is the square root of –1 and f is frequency in Hertz. The parameter ζ is referred to as the damping ratio and is related to the percent overshoot of the step response. The relationship is given in equation 25.C-3.

$$\%OS = \exp\left(-\pi \frac{\zeta}{\sqrt{1-\zeta^2}}\right)$$ (Equation 25.C-3)

There is no precise analytical relationship between ζ and the response time, t_r. However, for a given ζ, there is a relationship between t_r and ω_n. To understand this relationship, consider the filter's step response (underdamped case) given in equation 25.C-4.

$$h_{lp}(t) = 1 - Ce^{-\zeta\omega_n t}\cos\left(\frac{\omega_n t}{C} + \varphi\right)$$
$$C = \frac{1}{\sqrt{1-\zeta^2}}$$
$$\varphi = \tan^{-1}(C\zeta)$$ (Equation 25.C-4)

Recall that the response time is the time difference between the points where the step crosses 10% and 90% of its steady state voltage. Given ζ, iterative methods can be used to solve $h_{lp}(t) = 0.1$ and $h_{lp}(t) = 0.9$ for $\omega_n t$. The difference between these two solutions is $\omega_n t_r$ from which ω_n can be easily derived for a given t_r.

Note that the waveform overshoot is specified to be less than 5% and the response time is specified to be between 3 and 5ns [2].

25.C.4 – Baseline Wander

The baseline wander model is intended to duplicate the DC rejection properties of the channel. The low frequency response is determined by the magnetics at the transmitter, the cable, and the magnetics at the receiver. This model assumes that the frequencies being considered are low enough to model the cable as a lumped

resistance. This model also assumes that the magnetics at the transmitter and receiver are both ideal transformers with ideal coupling and a 1:1 turns ratio. The equivalent circuit of the channel is given in figure 25.C-2.

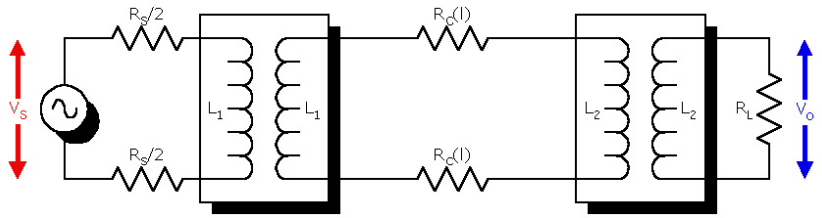


Figure 25.C-2: Baseline wander circuit model

The tran sfer function V_o/V_s is given in equation 25.C-5.

$$H_{hp}(s) = \frac{V_o}{V_s} = \frac{b_2 s^2}{a_2 s^2 + a_1 s + a_0}$$
$$b_2 = L_1 L_2 R_L$$
$$a_2 = L_1 L_2 (R_S + 2R_C R_L)$$
$$a_1 = R_S R_L (L_1 + L_2) + 2R_C (R_S L_2 + L_1 R_S)$$
$$a_0 = 2R_C R_S R_L$$

(Equation 25.C-5)

Note that the transfer function is a second-order highpass filter. The parameter R_C, which is the resistance of each conductor in the twisted pair wire, is a function of the cable length, l. R_C is specified to be no more than 9.38Ω per conductor for 100m of cable at 20°C [7]. Assuming a linear increase in R_C per unit length, R_C is given in equation 25.C-6.

$$R_C = 0.0938 \cdot l$$

(Equation 25.C-6)

It is also assumed that R_C will increase 0.4% per degree Celsius above 20°C. Note that as the length of the cable approaches zero, R_C also approaches zero. As R_C approaches zero, the transfer function approaches a first-order highpass response. This transfer function is given in equation 25.C-7.

$$H_{hp}(s)\Big|_{R_C=0} = \frac{sL_1 L_2 R_L}{sL_1 L_2 (R_S + R_L) + R_S R_L (L_1 + L_2)}$$

(Equation 25.C-7)

Note that the self inductance of the transformer coils, L1 and L2, is specified to be at least 350μH [1].

25.C.5 – DUT Magnetics Compensation

The baseline wander model includes the receive magnetics and line termination. However, these components are also embedded in the device under test (DUT). To eliminate this duplicity, a filter is constructed that compensates for the magnetics in the DUT and allows the baseline wander model to completely define the channel's low frequency response.

Consider the typical test configuration in which a waveform generator is connected to the DUT. An equivalent circuit for this configuration is shown in figure 25.C-3.

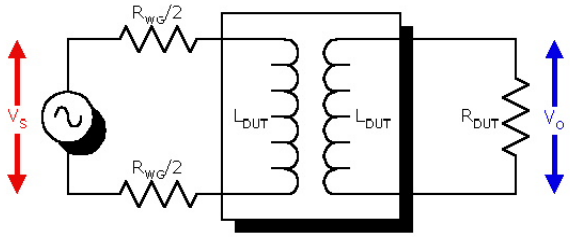


Figure 25.C-3: Test setup equivalent circuit.

The magnetics compensation filter is defined by the transfer function V_s/V_o which is given in equation 25.C-8.

$$H_{DUT}(s) = \frac{V_S}{V_o} = \frac{sL_{DUT}(R_{DUT} + R_{WG}) + R_{DUT}R_{WG}}{sL_{DUT}R_{DUT}} \qquad \text{(Equation 25.C-8)}$$

25.C.6 – Cable Attenuation

Cable attenuation is typically assumed to be a pure "skin effect" loss. The skin effect describes the tendency of AC currents to ride along the surface of a conductor. Higher frequencies correspond to a thinner skin and a higher loss. The transfer function of a pure skin effect loss is given in equation 25.C-9.

$$H_{skin}(s) = \frac{V_o}{V_i} = e^{-kl\sqrt{f}}e^{-jkl\sqrt{f}} \qquad \text{(Equation 25.C-9)}$$

In equation 25.C-9, l denotes the length of the cable in meters, f is the frequency in Hertz, and k is a constant that will be derived from the standard for category 5 cable. The upper bound on attenuation in decibels for 100m of category 5 cable at 20°C is given in equation 25.C-10 [8].

$$Attenuation(f) = 1.967\times10^{-3}\cdot\sqrt{f} + 2.3\times10^{-8}\cdot f + \frac{5\times10^{3}}{\sqrt{f}} \qquad \text{(Equation 25.C-10)}$$

Equation 25.C-10 is valid for frequencies in the range of 0.772 to 100MHz. Note that this expression is a skin effect loss, $f^{1/2}$, with two correction terms. The linear term is a high frequency correction that has a significant impact on the cable attenuation (i.e. greater than 2dB at 100MHz). The $f^{-1/2}$ term is a low frequency correction that has little impact (i.e. less than 0.1dB) on the attenuation for frequencies greater than 0.772MHz and approaches an arbitrarily large value as f approaches zero. The pure skin effect model is modified to incorporate the high frequency correction and the baseline wander model is left to define the low frequency response. The transfer function for the modified cable model is given in equation 25.C-11.

$$H_{cable}(f) = e^{-(k_1 l\sqrt{f} + k_2 lf)}e^{-jk_1 l\sqrt{f}} \qquad \text{(Equation 25.C-11)}$$

The values of k_1 and k_2 can be derived from equation 25.C-10 assuming a linear increase in loss per unit length. These values are given in table 25.C-1.

Table 25.C-1: Cable attenuation model parameters

Parameter	Value
k_1	2.265×10^{-6}
k_2	2.648×10^{-11}

Note that k_1 and k_2 are also allowed to increase up to 0.4% per degree Celsius above room temperature (20^oC) [8].

25.C.7 – Flat Loss

Losses in transmission path that are not attributed to the skin effect are referred to as "flat". Flat losses can cause problems for equalizer strategies that assume a pure skin effect loss and use peak detection to determine the required equalization level. Four sources of flat loss are identified: transmit magnetics, PC card "dongles", connectors, and receive magnetics.

Transmit Magnetics

The insertion loss of the transmit magnetics affects the amplitude of the signal launched into the channel. While this loss is not known, the amplitude of the signal at the 8-pin modular jack, V_{out}, is specified to be between 950 and 1050mV [2]. This can be translated to a flat loss (gain) relative to a nominal 1000mV transmit amplitude.

PC Card "Dongles"

The thin PC card is not able to accommodate an 8-pin modular jack so a "dongle" is typically used to map the standard interface to a more compatible interface. The dongle typically consists of an 8-pin modular jack, a short length of cable, and the mate to the connector provided by the PC card. While the dongle does introduce some flat loss, the transmit amplitude at the 8-pin modular jack must still be between 950 and 1050mV. Therefore, the flat loss of the dongle is not included in this model.

Connectors

Each connector in the transmit path adds to the flat loss. The connector at the transmitter is accounted for in the transmit amplitude specification. The connector at the receiver is built into the device under test and does not need to be modeled. However, up to four connectors are allowed in the cable infrastructure [13]. While the insertion loss of a category 5 connector is specified as a function of frequency [10], a simple uniform loss model is adopted. This model assumes that each connector adds 0.2dB of loss at all frequencies.

Receive Magnetics

The magnetics at the receiver are built into the device under test and do not need to be modeled. However, the insertion loss of the magnetics will vary from package to package due to process variations and multiplicity of vendors. An additional flat loss margin of 0.4dB is introduced to account for this variation.

The transfer function for the total flat loss is given in equation 25.C-12. In equation 25.C-12, C denotes the number connectors in the cable infrastructure and M is the flat loss margin.

$$H_{flat}(f) = \frac{V_{out}}{1V} \cdot 10^{\frac{-0.2 \cdot C}{20}} \cdot 10^{\frac{-M}{20}} \qquad \text{(Equation 25.C-12)}$$

25.C.8 – NEXT Loss

Time varying currents in one wire tend to induce time varying currents in nearby wires. This coupling is referred to as crosstalk. When the currents generated by the local transmitter induce currents on the receive channel, the coupling is referred to as near-end crosstalk (NEXT). NEXT coupling increases the additive noise at the receiver and thereby degrades the signal-to-noise ratio. The specifications of NEXT performance are typically given in terms of the NEXT loss which is the inverse of the NEXT coupling.

The lower bound on the NEXT loss in decibels for 100m of category 5 cable is given in equation 25.C-13 [9].

$$NEXT_{cable}(f) = 64\,\text{dB} - 15 \cdot \log_{10}\left(\frac{f}{0.772\,\text{MHz}}\right) \quad \text{(Equation 25.C-13)}$$

Equation 25.C-13 is valid for frequencies in the range of 0.772 to 100MHz. The lower bound on the NEXT loss in decibels for a category 5 connector is given in equation 25.C-14 [11].

$$NEXT_{c}(f) = 56\,\text{dB} - 20 \cdot \log_{10}\left(\frac{f}{16\,\text{MHz}}\right) \quad \text{(Equation 25.C-14)}$$

Equation 25.C-14 is valid for frequencies in the range of 1 to 100MHz[1]. Assuming that all contributions to the total NEXT coupling have unit amplitude sources and that all the contributions add in phase, the total NEXT loss of the channel can be computed as a simple voltage sum. This sum is given in equation 25.C-15.

$$NEXT_{channel}(f) = 20 \cdot \log_{10}\left(\sum_{i} 10^{\frac{-NEXT_i(f)}{20}}\right) \quad \text{(Equation 25.C-15)}$$

In equation 25.C-15, $NEXT_i(f)$ denotes the contribution of the i^{th} component. It is assumed that the dominant contributions to the NEXT loss of the channel are the cable and nearest two connectors [13]. Therefore, the sum would have three terms.

A model is adopted that duplicates the NEXT loss of equation 25.C-15 but is more easily scaled. This model is given in equation 25.C-16.

$$NEXT(f) = N_B - N_M \log_{10}\left(\frac{f}{16\,\text{MHz}}\right) \quad \text{(Equation 25.C-16)}$$

The parameters N_B and N_M in equation 25.C-16 are derived from a least mean squares curve fit to the data derived from equation 25.C-15. The values of these parameters are given in table 25.C-2.

Table 25.C-2: NEXT loss model parameters

Parameter	Value
N_B	40.5 dB
N_M	16.6 dB/decade

The NEXT loss values derived from this model do not deviate from the values derived from equation 25.C-15 by more than 0.5dB for frequencies in the range of 1 to 100MHz.

At this point, all that remains is a definition for the input to the NEXT loss model. Since the NEXT function is essentially a highpass filter, the coupled voltage is maximized by making the response time as fast as possible and the transmit amplitude as large as possible. To this end, the input is given a response time of 3ns, a

[1] Note that the absolute minimum NEXT loss of a category 5 connector is specified to be 65dB [10]. However, this specification seems to be ignored in the computation of the total NEXT loss for the channel [13]. This model also ignores this absolute minimum limit because the NEXT coupling must approach 0 as f approaches 0, i.e. there is no NEXT coupling at DC.

differential output voltage of 1050mV, and a waveform overshoot of 5%. Furthermore, the input to the NEXT model is delay modulated so that the peak value of the NEXT function sweeps across the bit interval.

25.C.9 – Summary of Model Parameters

Table 25.C-3: Summary of model parameters

Parameter	Description	Minimum	Maximum	Units
J_{pp}	Peak-peak jitter	0	1.4	ns
t_r	Response time	3	5	ns
%OS	Waveform overshoot	0	5	%
R_S	Transmitter source impedance		100	Ω
R_L	Receiver load impedance		100	Ω
L_1	Transmitter open circuit inductance		350	μH
L_2	Receiver open circuit inductance		350	μH
R_{WG}	Waveform generator source impedance		100	Ω
R_{DUT}	DUT load impedance		100	Ω
L_{DUT}	DUT open circuit inductance	measured in test #25.1.7		μH
l	Cable length	0	100	m
T	Temperature	20	60	°C
V_{out}	Differential output voltage	950	1050	mV
C	Number of connectors in the channel	0	4	—
M	Flat loss margin	0	0.4	dB
N_B	Reference NEXT loss (at 16MHz)	40.5	—	dB
N_M	NEXT loss scale	—	16.6	$^{dB}/_{decade}$

Appendix 25.D – Bit Error Rate Measurement

Purpose: To develop a procedure for bit error rate measurement through the application of statistical methods.

References:

[1] Miller, Irwin and John E. Freund, Probability and Statistics for Engineers (Second Edition), Prentice-Hall, 1977, pp. 194-210, 240-245.

Last Modification: January 22, 1999 (Version 1.0)

Discussion:

25.D.1 – Introduction

One key performance parameter for all digital communication systems is the bit error rate (BER). The bit error rate is the probability that a given bit will be received in error. The BER may also be interpreted as the average number of errors that would occur in a sequence of n bits.

While the bit error rate concept is quite simple, the measurement of this parameter poses some significant challenges. The first challenge is deciding the number of bits, n, that must be sent in order to make a reliable measurement. For example, if 10 bits were sent and no errors were observed, it would be foolish to conclude that the bit error rate is zero. However, common sense tells us that the more bits that are sent without error, the more reasonable this conclusion becomes. In the interest of keeping the test duration as short as possible, we want to send the smallest number of bits that provides us with an acceptable margin of error.

This brings us to the second challenge of BER measurement. Given that we send n bits, what reasonable statements can be made about the bit error rate based on the number of errors observed? Returning to the previous example, if 10 bits are sent and no errors are observed, it is unreasonable to say that the BER is zero. However, it may be more reasonable to say that the BER is 10^{-1} or better. Furthermore, you are absolutely certain that the bit error rate is not 1.

In this appendix, two statistical methods, hypothesis testing and confidence intervals, are applied to help us answer the questions of how many bits we should be sent and what conclusions can be made from the test results.

25.D.2 – Statistical Model

A statistical model for the number of errors that will be observed in a sequence of n bits must be developed before we apply the aforementioned statistical methods. For this model, we will assume that every bit received is an independent Bernoulli trial. A Bernoulli trial is a test for which there are only two possible outcomes (i.e. a coin toss). Let us say that p is the probability that a bit error will occur. This implies that the probability that a bit error will not occur is (1-p).

The property of independence implies that the outcome of one Bernoulli trial has no effect on the outcomes of the other Bernoulli trials. While this assumption is not necessarily true for all digital communications systems, it is still used to simplify the analysis.

The number of successful outcomes, k, in n independent Bernoulli trials is taken from a binomial distribution. The binomial distribution is defined in equation 25.D-1.

$$b(k;n,p) = C_{n,k}\, p^k (1-p)^{n-k} \qquad \text{(Equation 25.D-1)}$$

Note that in this case, a successful outcome is a bit error. The coefficient $C_{n,k}$ is referred to as the binomial coefficient or "n-choose-k". It is the number of combinations of k successes in n trials. Returning to coin toss

analogy, there are 3 ways to get 2 heads from 3 coin tosses: (tails, heads, heads), (heads, tails, heads), and (heads, heads, tails). Therefore, $C_{3,2}$ would be 3. A more precise mathematical definition is given in equation 25.D-2.

$$C_{n,k} = \frac{n!}{k!(n-k)!} \quad \text{(Equation 25.D-2)}$$

This model reflects the fact that for a given probability, p, a test in which n bits are sent could yield many possible outcomes. However, some outcomes are more likely than others and this likelihood principle allows us to make conclusions about the BER for a given test result.

25.D.3 – Hypothesis Test

The statistical method of hypothesis testing will allow us to establish a value of n, the number of bits to be sent, for the BER measurement. Naturally, the test begins with a hypothesis. In this case, we will hypothesize that the probability of a bit error, p, for the system is less than some target BER, P_0. This hypothesis is stated formally in equation 25.D-3.

$$H_0 : p \le P_0 \quad \text{(Equation 25.D-3)}$$

We now construct a test for this hypothesis. In this case, we will take the obvious approach of sending n bits and counting the number errors, k. We will interpret the test results as shown in table 25.D-1.

Table 25.D-1: Acceptance and rejections regions for H_0

Test Result	**Conclusion**
k = 0	H_0 is true
k > 0	H_0 is false

We now acknowledge the possibility that our conclusion is in error. Statisticians define two different categories of error. A type I error is made when the hypothesis is rejected even though it is true. A type II error is made when the hypothesis is accepted even though it is false. The probability of a type I and a type II error are denoted as α and β respectively. Table 25.D-2 defines type I and type II errors in the context of this test.

Table 25.D-2: Definitions of type I and type II errors

Type I Error	k > 0 even though p ≤ BER
Type II Error	k = 0 even though p > BER

A type II error is arguably more serious and we will define n so that the probability of a type II error, β, is acceptable. The probability of a type II error is given in equation 25.D-4.

$$\beta = (1-p)^n < (1-P_0)^n \quad \text{(Equation 25.D-4)}$$

Equation 25.D-4 illustrates that the upper bound on the probability of a type II error is a function of the target bit error rate and n. By solving this equation for n, we can determine the minimum number of bits that need to sent in order to verify that p is less than a given P_0 for a given probability of type II error.

$$n > \frac{\ln(\beta)}{\ln(1-P_0)} \quad \text{(Equation 25.D-5)}$$

Let us now examine the probability of a type I error. The definition of α is given in equation 25.D-6.

$$\alpha = 1 - (1 - p)^n \leq 1 - (1 - P_0)^n \qquad \text{(Equation 25.D-6)}$$

Equation 25.D-6 shows that while we increase n to make β small, we simultaneously raise the upper bound on α. This makes sense since the likelihood of observing a bit error increases with the number of bits that you send, no matter how small bit error rate is. Therefore, while the hypothesis test is very useful in determining a reasonable value for n, we must be very careful in interpreting the results. Specifically, if we send n bits and observe no errors, we are confident that p is less than our target bit error rate (our level of confidence depends on how small we made β). However, if we do observe bit errors, we cannot be quick to assume that the system did not meet the BER target since the probability of a type I error is so large. In the case of k > 0, a confidence interval can be used to help us interpret k.

25.D.4 – Confidence Interval

The statistical method of confidence intervals will be used to establish a lower bound on the bit error rate given that k > 0. A confidence interval is a range of values that is likely to contain the actual value of some parameter of interest. The interval is derived from the measured value of the parameter, referred to as the point estimate, and the confidence level, (1-α), the probability that the parameter's actual value lies within the interval.

A confidence interval requires a statistical model of the parameter to be bounded. In this case, we use the statistical model for k given in equation 25.D-1. If we were to compute the area under the binomial curve for some interval, we would be computing the probability that k lies within that interval. This concept is shown in figure 25.D-1.

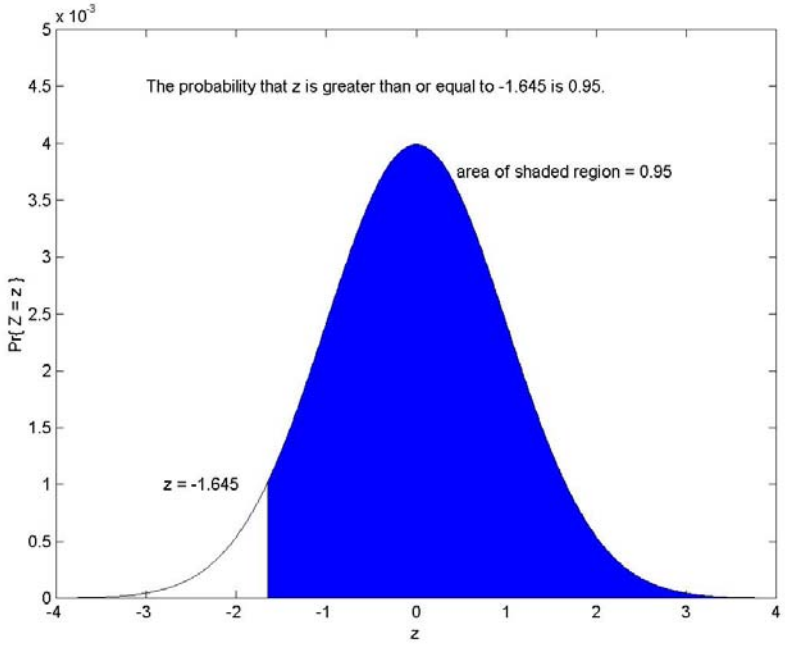


Figure 25.D-1: Computing the probability that z ≥ -1.645 (standard normal distribution).

To compute the area under the binomial curve, we need a value for the parameter p. To compute a confidence interval for k, you assume that k/n, the point estimate for p, is the actual value of p.

Note that figure 25.D-1 illustrates the computation of the lower tolerance bound for k, a special case where the confidence interval is $[k_l, +\infty]$. A lower tolerance bound implies that in a percentage of future tests, the value of

k will be greater than k_l. In other words, actual value of k is greater than k_l with probability equal to the confidence level. Therefore, if k_l/n is greater than P_0, we can say that the system does not meet the target bit error rate with probability (1-α). By reducing α, we reduce the probability of making a type I error.

To determine the value of k_l, it is useful to assume that the binomial distribution can be approximated by a normal (Gaussian) distribution when n is large. The mean and variance of this equivalent distribution are the mean and variance of the corresponding binomial distribution (given in equations 25.D-7 and 25.D-8).

$$\mu_K = np \quad \text{(Equation 25.D-7)}$$

$$\sigma_K^2 = np(1-p) \quad \text{(Equation 25.D-8)}$$

Now, let α be the probability that $Z \le z_\alpha$ where Z is a standard normal random variable. A standard random variable is one whose mean is zero and whose variance is one. The random variable K can be standardized as shown in equation 25.D-9.

$$Z = \frac{K - \mu_K}{\sigma_K} \quad \text{(Equation 25.D-9)}$$

Note that Z is greater than z_α with probability (1-α), the confidence level. We apply this inequality to equation 25.D-9 and solve for K to get equation 25.D-10.

$$K > \mu_K + z_\alpha \sigma_K$$
$$K > np + z_\alpha \sqrt{np(1-p)} \quad \text{(Equation 25.D-10)}$$

As mentioned before, we assume that p is k/n. We can now generate an expression for k_l, the value that K will exceed with probability (1-α). This expression is given in equation 25.D-11.

$$k_l = k + z_\alpha n \sqrt{\frac{(k/n)(1-k/n)}{n}} \quad \text{(Equation 25.D-11)}$$

Finally, we argue that if K exceeds k_l, then the actual value of p must exceed k_l/n. Therefore, we can generate an expression for p_l, the value that p will exceed with probability (1-α), and compare it to the target bit error rate. By applying this comparison (given in equation 25.D-12) the probability of a type I error can be greatly reduced. For example, by setting z_α to –1.645, the probability of a type I error is reduced to 5%.

$$P_0 \ge p_l = \frac{k_l}{n} = \frac{k}{n} + z_\alpha \sqrt{\frac{(k/n)(1-k/n)}{n}} \quad \text{(Equation 25.D-12)}$$

25.D.5 – Sample Test Construction

We now compress the theory presented in sections 25.D-2 through 25.D-4 into two inequalities that may be used to construct a bit error rate test. First, we take equation 25.D-5 and assume that $\ln(1-P_0)$ is $-P_0$ (valid for P_0 much less than one). The result is equation 25.D-13.

$$n > \frac{-\ln(\beta)}{P_0} \quad \text{(Equation 25.D-13)}$$

Second, we examine equation 25.D-12. Assuming that (1-k/n) is very close to 1 and substituting $-\ln(\beta)/P_0$ for n, we get equation 25.D-14.

$$-\ln(\beta) \geq k + z_\alpha \sqrt{k}$$ (Equation 25.D-14)

The largest value of k that satisfies equation 25.D-14 is k_l. The benefit of these two equations is that a bit error rate test is uniquely defined by β and α and that the test scales with P_0. Table 25.D-3 defines n and k_l in terms of β and α.

Table 25.D-3: n and k_l as a function of β and α.

β	–ln(β)	n	α	z_α	k_l
0.10	2.30	$2.30/P_0$	0.10	–1.29	5
0.10	2.30	$2.30/P_0$	0.05	–1.65	6
0.05	3.00	$3.00/P_0$	0.05	–1.65	7
0.05	3.00	$3.00/P_0$	0.01	–2.33	10
0.01	4.60	$4.60/P_0$	0.05	–1.65	9
0.01	4.60	$4.60/P_0$	0.01	–2.33	13

As an example, let us construct a test to determine if a given system is operating at a bit error rate of 10^{-12} or better. Given that a 5% chance of a type I error is acceptable, the test would take the form of sending $3x10^{12}$ bits and counting the number of errors. If no errors are counted, we are confident that the BER was 10^{-12} or better.

Given that a 5% chance of a type II error is acceptable, we find that k_l is 7. If more than 7 errors are counted, we are confident that the bit error rate is greater than 10^{-12}. However, what if between 1 and 7 errors are counted? These cases may be handled several different ways. One option is to make a statement about the bit error rate (whether it is less than or greater than 10^{-12}) at a lower level of confidence. Another option would be to state that the test result is success since we cannot establish with an acceptable probability of error that the BER is greater than 10^{-12}. Such a statement implies that we failed to meet the burden of proof for the conjecture that the BER exceed 10^{-12}. Of course, the burden of proof could be shifted to the device under test which would imply that any outcome other than k = 0 would correspond to failure (the device under test failed to prove to us that the BER was no more than 10^{-12}). If neither of these solutions are acceptable, it is always an option to perform a more vigorous bit error rate test in order to clarify the result.

25.D.6 – Packet Error Rate Measurement

It is often easier to measure packet errors than it is to measure bit errors. In these cases, it is helpful to have some linkage between the packet error rate and the bit error rate. To make this linkage, we assume that the bit error rate is low enough and the packet size is small enough so that each packet error contains exactly one bit error.

To complete the linkage, some care must be taken regarding how many packets to send. A bit error is only detectable in the region of the packet that is covered by the cyclic redundancy check (CRC). In the context of Ethernet, this region is the first bit of the destination address to the last bit of the CRC. There is no guarantee that errors in the preamble, start-of-frame delimiter, and inter-packet gap will be detected. Therefore, we must translate n from the number of bits are sent to the number of "observable" bits that are sent. This will increase the test duration since a portion of the time will be spent sending unobservable bits.

For packets of length x bits, at least n/x packets must be sent to perform the equivalent bit error rate test. If no packet errors are observed, the conclusion is that the bit error rate is less than P_0. If more than k_l packet errors are observed, the conclusion is that the bit error rate is greater than P_0.

Note that x is the length of the packet after encoding. In other words, in a 4B5B encoding environment, a 64-byte packet is 640 bits in length after encoding. Also note that to reinforce the assumption that there is only one bit error per packet error, a test should be run with the shortest possible packets. However, if extremely low bit

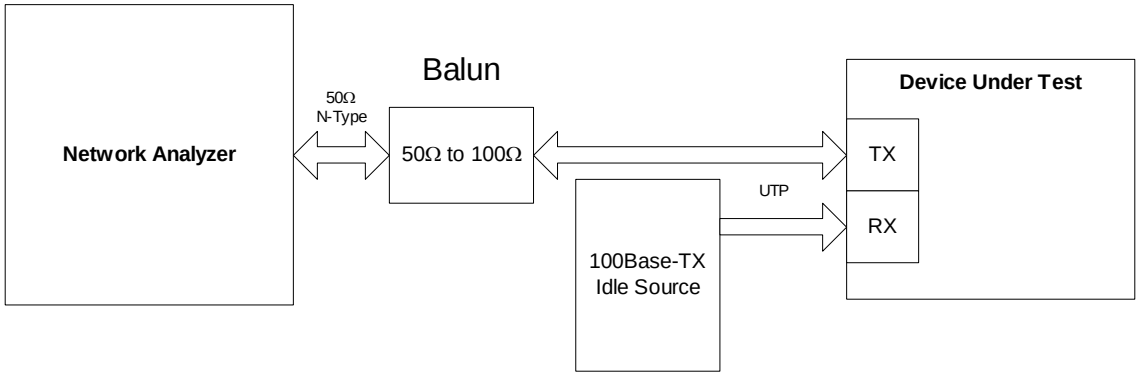
error rates are to be verified, it may be favorable to use long packets to increase the percentage of observable bits and reduce the test duration.

Appendix 25.E – Return Loss Incident Wave Power Calculations

Purpose: In order to do return loss measurements on 100BASE-TX devices and 1000BASE-T devices, the device under test (DUT) must be acting the way it would during normal operation. This means the DUT must be sourcing IDLE from the port during the test. The power which is being transmitted from the DUT will cause an error in the measurements seen by the network analyzer measuring the port. In this document, an explanation is given for why a 0dBm incident wave power is used.

Last Modification: February 12, 2004

Test Setup:



Discussion:

In order to assure that the return loss measurement has an error which is less than 0.5dB, the incident wave power sourced by the network analyzer needs to be significantly larger than the power sourced by the DUT. In order to find how much larger, the calculations shown in test 25.1.6 – Transmitter Return Loss are used. This requires us to know the voltage transmitted by the DUT (V_T). This is however, not as simple as the peak to peak voltage of the IDLE stream. The network analyzer works by sweeping across the frequencies of interest and measuring the power which is reflected by the interface of the device. In order to get an accurate V_T, we must look at the voltage per hertz contained in the IDLE stream. The maximum value of this will cause the worst case error in the return loss measurement. Once this worst case voltage has been found, the incident wave voltage can be set to meet the 0.5dB error margin specified in the test.

By using an FFT, the frequency domain voltages can be found for the spectrum of a full sequence of MLT-3 IDLE. This requires having 8188 symbols of the idle sequence. This will allow us to find the spectrum of the IDLE using one full period of the sequence.

An important item to consider when finding the maximum of V_T is that the network analyzer does not look at a single frequency. All frequencies which are within the IF bandwidth of the network analyzer must be considered. Typically, the IF bandwidth of the network analyzer is set to 100Hz. This means that the value of V_T will be the sum of the frequencies in a 100Hz window around the test tone. For this reason, the FFT is taken using 100Hz wide bins of frequency. The maximum amplitude bin is used to calculate the required incident voltage.

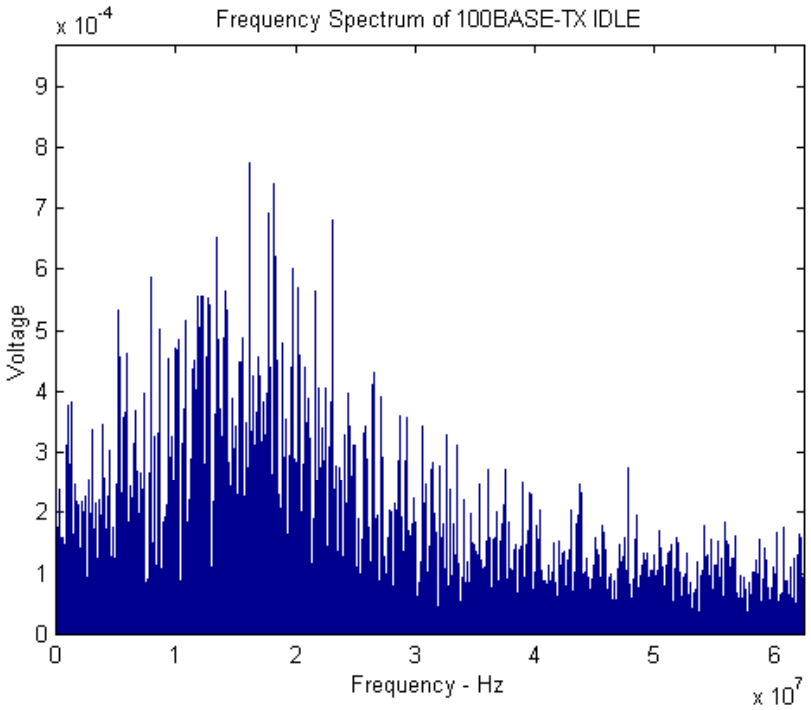


Figure 25.E-1 – Frequency Spectrum of 100Base-Tx IDLE

Using the maximum value in the plot above, we can calculate what the minimum incident voltage must be.

$$V_I \geq V_T/.016 \rightarrow V_I \geq (8x10^{-4})/.016 \rightarrow V_I \geq .05 \text{ volts}$$

This is the voltage required at the 100Ω side of the balun. Since the impedance transform is 50Ω to 100Ω, the required voltage at the 50Ω side of the balun will be:

$$V_I \geq .05/\text{sqrt}(2) \rightarrow V_I \geq .0354 \text{ volts}$$

During regular testing, an incident wave with a power level of 0dBm is used. This translates to a voltage of 224mV when driving into a 50Ω load. This far surpasses the minimum incident wave voltage required to have less than 0.5dB of error in the return loss measurement.