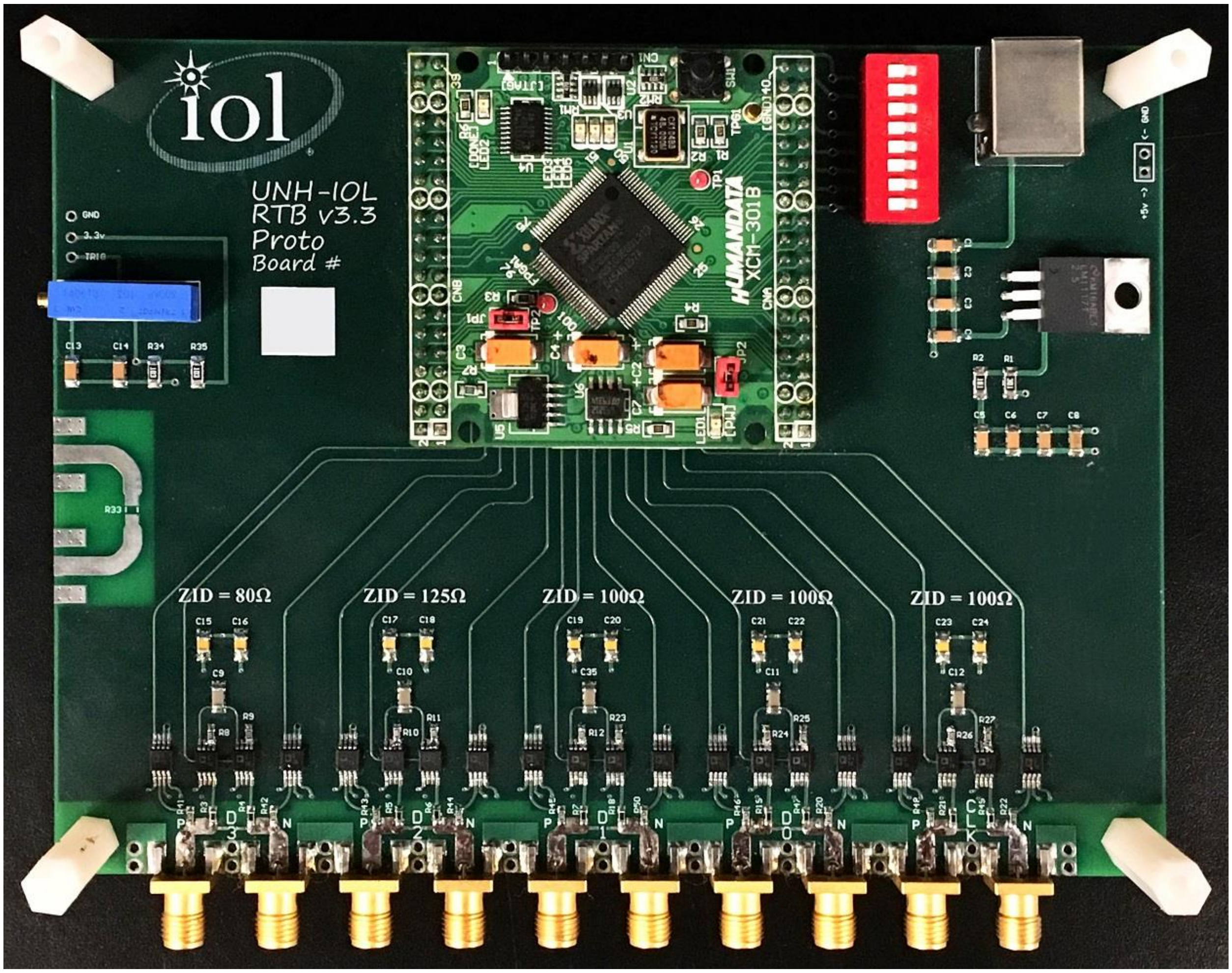
MIPI D-PHY
REFERENCE TERMINATION BOARD (RTB)
OVERVIEW AND DATASHEET



Abstract:

This document serves as the primary documentation for the MIPI D-PHY Reference Termination Board (RTB), which is a reference termination test fixture used for performing MIPI D-PHY transmitter physical layer signaling measurements. (It is also used for measuring and calibrating the output of a reference signal source used for performing D-PHY receiver tolerance testing.) An overview of the features and general theory of operation of the board is discussed. Schematics are included, as well as typical performance characteristics in the form of

S-Parameters, which are plotted against the MIPI D-PHY RX requirements to show the amount of margin.

Introduction:

The MIPI D-PHY Reference Termination Board (RTB) is a reference test fixture that is designed to emulate 'ideal' best-case and worst-case reference D-PHY receiver termination characteristics. Measurement data included in this document shows the D-PHY RTB is appropriate for testing products with bit rates up to 2.5 Gbps. It is implemented in the form of an actively-controlled HS resistive load, which is enabled and disabled with the appropriate timings via FPGA control, according to the MIPI D-PHY LP signaling protocol. The fixture enables the measurement of most HS voltage and timing parameters using a single measurement setup, and the board is designed with very precisely controlled impedance and termination characteristics, in order to present a consistent, repeatable, termination environment to D-PHY transmitters for the purpose of performing MIPI-D-PHY transmitter physical layer conformance testing (and also for calibrating the output of lab signal sources when performing D-PHY receiver tolerance testing.) The board is meant to be used in conjunction with a real-time DSO and the necessary probing, accessories, and analysis software required for performing D-PHY measurements. The Reference Termination Board, along with other boards offered at the UNH-IOL, were developed by the UNH-IOL's MIPI D-PHY consortium which offers conformance and interoperability testing for MIPI Cameras, Displays, and Panels. For more information about general D-PHY test equipment requirements, as well as test definitions, setups, services, and procedures, please contact UNH-IOL at mipilab@iol.unh.edu.

Background:

Unlike many other high-speed serial technologies that utilize a static, 100-ohm differential reference termination environment, MIPI D-PHY is somewhat unique in that one of the key power-saving aspects of D-PHY is it's the fact that the link utilizes a dynamic, switchable resistive termination at the receiver, which is enabled during the High-Speed (HS) mode of operation, and disabled to present an open termination environment during Low-Power (LP) mode. The HS and LP modes utilize different signaling schemes, with different voltage levels. The LP mode of operation is designed such that data can still be communicated between the two ends of the link, but at a much lower speed (20Msymbols/sec max) than in HS mode, which is designed for operation between 80 and approximately 800 Mbps. This dual-mode functionality requires different receiver architecture than that typically found in other high-speed serial technologies. A simplified diagram of an example receiver implementation is shown in Figure 1 below (which has been reproduced from the D-PHY specification.)

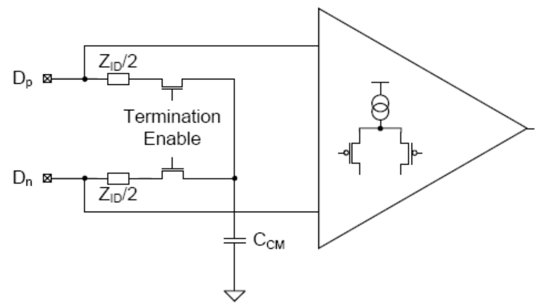


Figure 1: Example D-PHY Receiver Termination Diagram

In LP mode, all wires are operated single-ended, and are unterminated at the receiver. In this mode, minimal current flows between the two ends of the link (due to the lack of an RX termination), which reduces power consumption. In HS mode, the link utilizes differential signaling, but with a lower amplitude level than most other high-speed serial technologies, and also with a common-mode DC offset (whereas most other high-speed serial technologies are AC-coupled, and use DC-balanced signaling levels in conjunction with 8B/10B encoding).

D-PHY devices switch between HS and LP modes via communication of a special LP state sequence, which signals an intent to transition to HS mode. When a receiver detects this mode it will enable its High-Speed (HS) line termination, which prepares the line for HS operation. The transmitter is then able to transmit data at the HS line rate for a period of time, after which a different control sequence is sent, which initiates a return to the LP mode of operation (whereby the receiver disconnects its HS termination at the appropriate time). This act of switching in and out of HS mode is typically called HS 'burst mode' operation.

In most other high-speed serial technologies that utilize a static, 100-ohm differential termination environment with DC-balanced signaling, it is common to use the test equipment input ports as the reference termination load for measurements, as the front end inputs of most pieces of test equipment are 50-ohm terminated, which effectively looks like a 50-ohm resistance to ground. By splitting the differential signal into two halves, and terminating each half into 50 ohms, a 100-ohm differential termination is achieved. This is typically the approach used for technologies like SATA, SAS, PCI Express, XAUI, 10GBASE-CX4, etc. For all of these standards, the test equipment basically provides a common, reference termination environment which is relatively consistent between different pieces of test equipment, as the termination specifications for the inputs of lab test equipment are typically very tightly controlled.

D-PHY however, presents a somewhat unique challenge, as there are two main factors that prevent using the test equipment (oscilloscope in this case) as the reference termination. The first is simply the presence of the switching open/100-ohm receiver termination, which no standard test instrument is capable of duplicating. The second factor is the fact that the HS mode of D-PHY expects the receiver to be AC coupled to ground, so that a DC common-mode offset may be applied to the HS signal. If the HS differential signal is split and sent into two 50-ohm input ports of a DSO, the transmitter's common mode signal component does not see an AC-coupled path to ground, but rather a 25-ohm DC path to ground (created by the two 50-ohm input resistances in parallel.) This is not the termination for which the transmitter was designed, and thus prevents this type of measurement setup from being used.

Another measurement approach that is used to measure high-speed serial signals is to terminate the desired signal with an external termination load, and then probe the signal at that termination point using a high-impedance active differential probe. These high-performance probes use active circuitry to observe the signal under test without disturbing the signal itself, or causing excessive additional loading to the transmitter.

In this environment, the quality of the signal observed depends heavily on the electrical characteristics and quality of the external termination element used to terminate the line, as well as the quality of the means used to physically attach the termination element (typically a resistor) to the line. Hand-soldering of discrete components to a transmitter output port is typically not precise enough to produce consistent, repeatable results. Furthermore, this still does not address the switching nature of the D-PHY termination environment. Because of these issues, and the need to demonstrate accurate, repeatable physical layer measurements for D-PHY, there arose a need for a specialized, laboratory-grade termination solution for D-PHY test purposes.

The Solution:

To meet the need for a single common reference termination solution for D-PHY, the D-PHY Reference Termination Board (RTB) was developed, and is intended to serve as a common reference test fixture to facilitate consistent and repeatable conformance measurements of MIPI D-PHY signaling, for both conformance and characterization purposes.

A detailed image of the RTB is shown in the figure below, with icons highlighting several of the key features, which are described in further detail below.

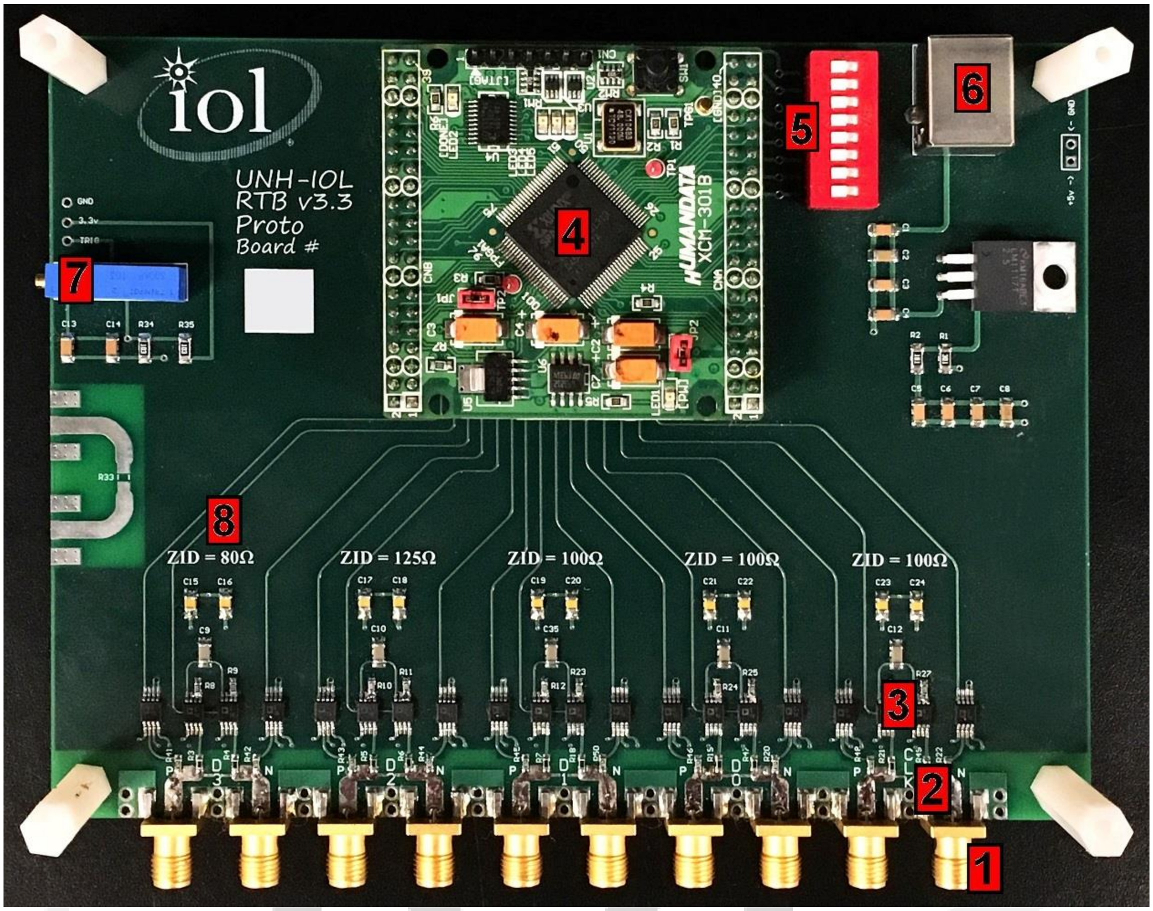


Figure 2: Detailed View of RTB (Top Side)

Features:

Several key features of the RTB highlighted in Figure 2 above are:

1 1) SMA Inputs with Recommended Spacing and Lane Ordering:

The RTB uses standard SMA RF connectors. This is the means by which the RTB is connected to the Device Under Test (DUT). The RTB supports up to five D-PHY Lanes (1 Clock + 4 Data), and uses a common SMA spacing and Lane pinout recommended by UNH IOL for D-PHY test board designs, commonly known as the Test Vehicle Board (TVB) recommendations. The purpose of specifying a common spacing and Lane ordering is to allow devices that implement the TVB spacing and pinout to be mated directly to one another using only SMA male-to-male couplers. This eliminates the need for additional SMA cables for connecting devices together, and provides the best possible quality signal path between devices.

The spacing of the SMA connectors is 500-mil, center-to-center, for all connectors. The Lane ordering is (reading right to left in Figure 2 above): ClkN, ClkP, Data0N, Data0P, Data1N, Data1P, Data2N, Data2P, Data3N, Data3P.

Note that the recommended Lane ordering is optimized for testing peripheral devices (e.g., Camera Sensors or Displays), however the RTB can also be used for testing Host DUTs, by simply flipping the RTB upside-down, which reverses the pinout. The recommended lane ordering is shown graphically below, for both Hosts and Peripherals.

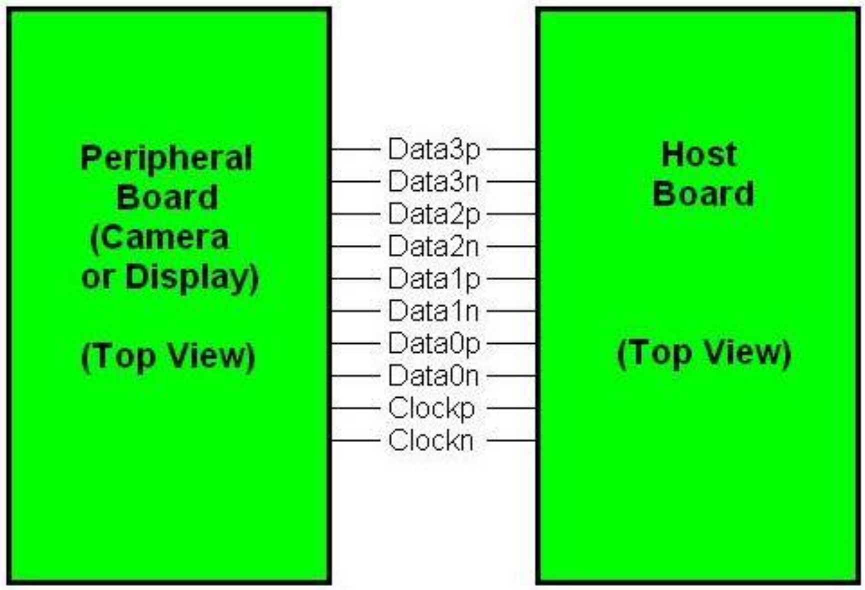


Figure 3: Recommended Lane Ordering for DUT Evaluation Boards

2 2) Controlled-Impedance SMA Launches:

In order to optimize the connection path between devices, care must be taken to minimize impedance discontinuities that can occur at and around the SMA connectors of test boards. The area where the signal transitions from the pin of the SMA connector into the PCB trace is commonly called the **launch**. Poor quality SMA connectors, and/or poor PCB launch design can result in impedance discontinuities that will cause reflections to occur, resulting in reduced signal integrity, and other signaling artifacts, which are not acceptable when trying to make accurate measurements. The RTB uses a specially designed launch, customized for the specific SMA connector used, which minimizes the impedance discontinuity introduced by the SMA connectors. By using controlled launches on both the RTB and the DUT's evaluation PCB, signals can pass through the SMA interface between boards with minimal degradation.

3 3) Active-Switching Termination Structure:

The small components seen just after the launch structure make up the HS termination structure. The structure for each Lane consists of two ADG8611 Ultrafast 4ns Single-Supply

Comparators (which buffer the signal and are used to determine the high/low state of the line in LP mode), and two ADG902 Wideband 1GHz CMOS Switches, which perform the actual switching of the HS termination resistor (commonly referred to as ZID in the D-PHY specification), which is also implemented as part of the termination structure (see the small SMD resistors located between the switches/comparators, and the SMA launches).

The termination structures are specifically designed to be located as near to the SMA launches as possible, in order to minimize the excess trace length, and hence the capacitive loading seen by the DUT transmitter.

4 4) FPGA for Termination Control and Timing:

The termination switch structure alone is not sufficient to accomplish the switching operation. The purpose of the ADG8611 comparators is actually to sense the line and determine the LP line state during regular DUT operation. The output of the comparators is sent to the inputs of the FPGA, which is programmed to understand the LP signaling protocol, and looks for the proper 'HS-entry' sequence of LP states (LP-11/LP-01/LP-00), at which point it triggers the ADG902 switches to close and enable the HS termination resistor (ZID), in preparation for HS mode.

Once HS mode is enabled, the FPGA is programmed to look for the end of the HS burst (signaled by a return to the LP-11 state), at which point it disconnects the HS termination by deactivating the ADG902 switches.

5 5) Manual Override Dipswitches:

Because there are cases where it may be necessary to force the HS termination on or off (for example, in the case of a CSI-2 transmitter that supports Continuous Clocking, in which case LP signaling is not used on the Clock Lane, as the HS clock is transmitted continuously and does not return to LP mode between bursts), the dipswitches (SW1) on the RTB may be used to override the FPGA control, and manually force the HS terminations on or off.

The dipswitches allow independent control of the Clock Lane and the group of four Data Lanes, and work as follows:

DIPSW8: **ON : CLK Lane Termination always ON**

DIPSW7: **ON: CLK Lane Termination always OFF**

DIPSW6: **ON: DATA0/1/2/3 Lane Termination always ON**

DIPSW5: ON: DATA0/1/2/3 Lane Termination always OFF

For example, if you want to force the Clock Lane termination ON (for a continuous-clocking DUT), then you would turn DIPSW8 to ON, and rest of switches to OFF

6 6) Power Supply (USB):

The RTB receives power via a standard USB connection to any USB host port. (Note the USB connection is only used to supply power, and does not perform data transfer of any kind.)

The 5V supply voltage from the USB port is stepped down to 3.3V via the LM1117T regulator, which supplies power to all of the other active components on the board.

7 7) Comparator Reference Level Adjustment:

The two comparators per Lane are used to buffer the incoming signals, and effectively make a digital copy of each single-ended LP signal, which is sent back to the FPGA. The comparators compare the observed line level against a reference voltage level, and output a logic 1 or 0 if the line level is higher or lower than the reference voltage, respectively.

The comparator reference level is set to 0.6V by default, as this is approximately one-half of the typical nominal LP signaling level of 1.2V. The FPGA is programmed to enable the HS termination at a specific time after the last falling LP edge of the HS entry sequence (LP-11/LP-10/LP-00). In rare cases where the FPGA does not appear to be enabling the HS termination at the proper time, it may be possible to adjust this value by modifying the comparator's reference voltage level, which may have some effect if the LP edges of the DUT have an especially slow fall time. (Again, this should never really be necessary under typical conditions.) The comparator reference level can be measured using a voltmeter between vias marked 'GND' and 'TRIG', located near the blue potentiometer. The level can then be adjusted with the blue potentiometer, using a small screwdriver.

8 8) Worst-Case ZID Values (Lanes Data2 and Data3):

The final feature of the RTB worth noting is the fact that the RTB does not use the same ZID resistance value for all Lanes.

The D-PHY specification requires several of the HS-TX signaling requirements to be met, 'for all possible values of ZID'. This includes the HS rise/fall times, as well as VCMTX, VOD, and VOHHS. For the purpose of measuring these values under the 'worst-case' ZID values (i.e., the maximum and minimum values defined in the spec), the Data2 and Data3 Lanes of the RTB are designed with ZID values of 125 and 80 ohms, respectively (while the Clock, Data0, and Data1 Lanes all designed with ZID = 100 ohms by default). These Lanes can be used to terminate individual DUT Lanes for the purpose of these amplitude-specific measurements.

(Note that in these cases the Clock Lane of the RTB will not mechanically align to the Clock Lane of the DUT, however depending on the measurement software being used, a Clock Lane signal may not be required to perform the amplitude-specific measurements that require being tested with the worst-case ZID values.

Note also that the standard RTB configuration is optimized for DUT's having up to 2 Data Lanes. For DUTs with 3 or 4 Data Lanes, it may be necessary to use short SMA cables to remap the DUT's Data Lanes 3 and 4 to the RTB's Data Lanes 0 and 1 for some HS measurements, where both Clock and Data Lane signals need to be measured simultaneously into ZID values of 100 ohms (e.g., clock-to-data skew). In these cases the SMA cables should be as short as possible, and should also be matched in terms of electrical length, to minimize additional skew.

One additional note regarding the ZID resistor values: All Lanes of the RTB are functionally identical, and independently controlled by the FPGA. The only real difference is the ZID values for the Data2 and Data3 Lanes. Technically it would be possible to modify/remap the ZID values for any lane to any value or combination/order of values, by simply changing the two ZID resistors per lane (which are each approximately ZID/2, but are actually 1-2 ohms lower than this to account for the added resistance of the switches, which are effectively in series with the ZID resistors). Again, this should not need to be done under normal circumstances, but it is mentioned here for informative purposes only.

Also, the common-mode termination capacitance (Ccm) is controlled by a single capacitor per Lane, and is designed with a value of 47pF for all Lanes, as this produces the optimal common-mode return loss characteristics (see S-Parameter data, in the last section of this document). This value can also technically be modified via a component change on the RTB, but again this should not be required under normal circumstances.

Schematics:

The schematics for the RTB are shown below. (Note that only the full circuit for the Clock Lane is shown, as the other four Lanes are identical, except for the values of the ZID resistors.)

(Also note that a copy of the termination circuit schematic is also printed on the bottom silkscreen of the actual RTB PCB, for convenience.)

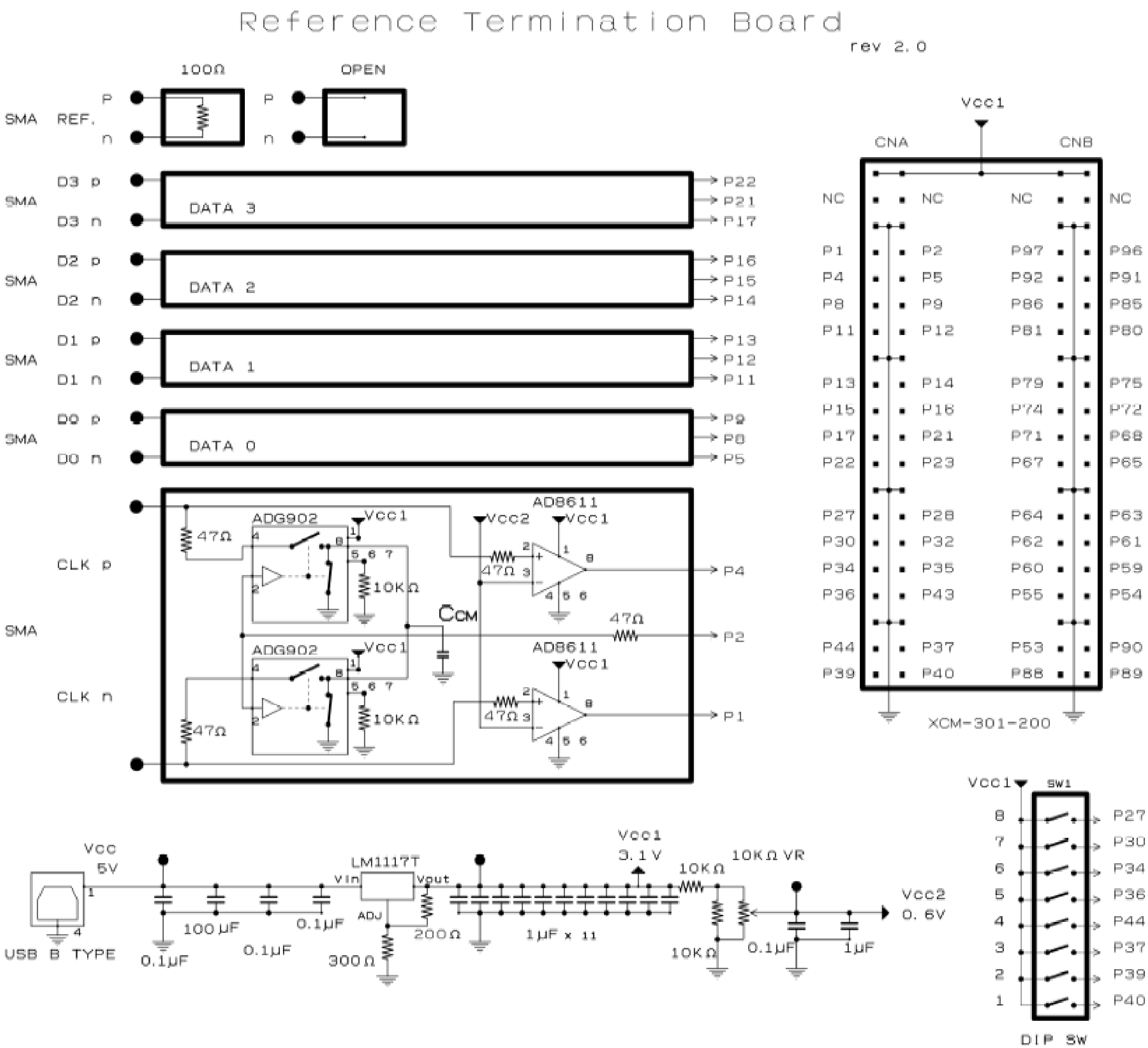


Figure 4: RTB Schematics

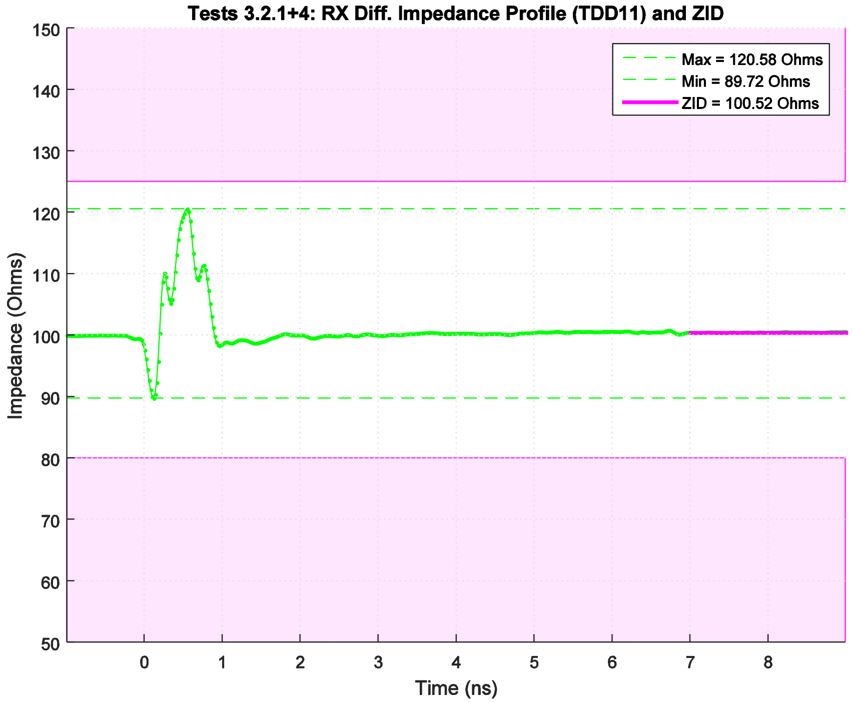
Impedance and S-Parameter Data:

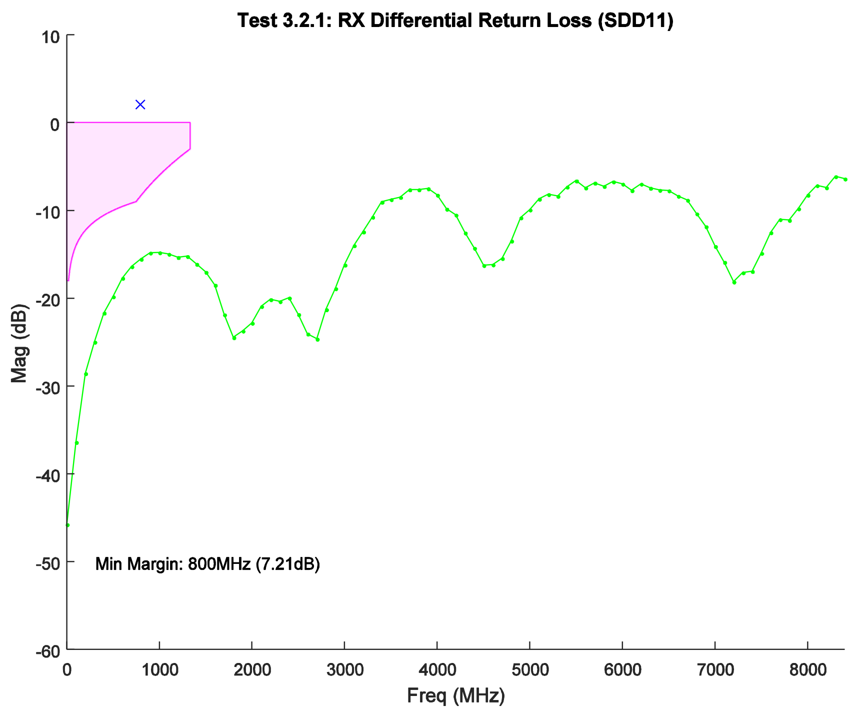
The following pages contain impedance profile data and S-Parameter return loss data for the different Lanes of the RTB. Where applicable, the values are plotted against the D-PHY HS-RX S-Parameter requirements (i.e., the data is presented as if the RTB were tested as an actual D-PHY receiver device.)

Data is presented for three Lanes: Clock, Data2, and Data3. The characteristics for Data Lanes 0 and 1are not shown because they are identical to the Clock Lane (i.e., ZID = 100 ohms for the Clock, Data0, and Data1 Lanes.)

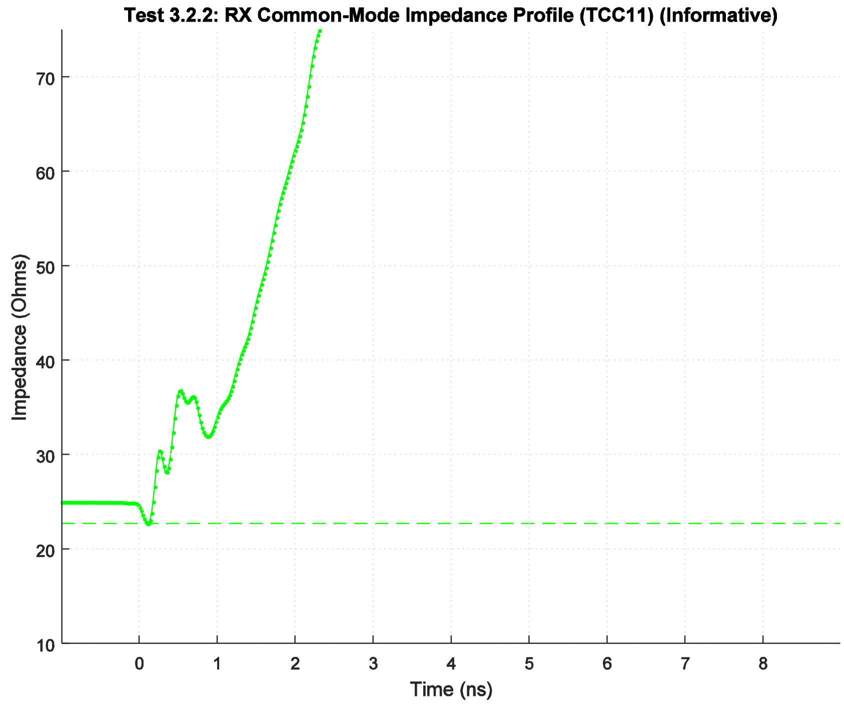
Note: The raw S-Parameter data source files used to generate these plots are available (for simulation purposes, etc), and can be obtained by contacting UNH-IOL at mipilab@iol.unh.edu.

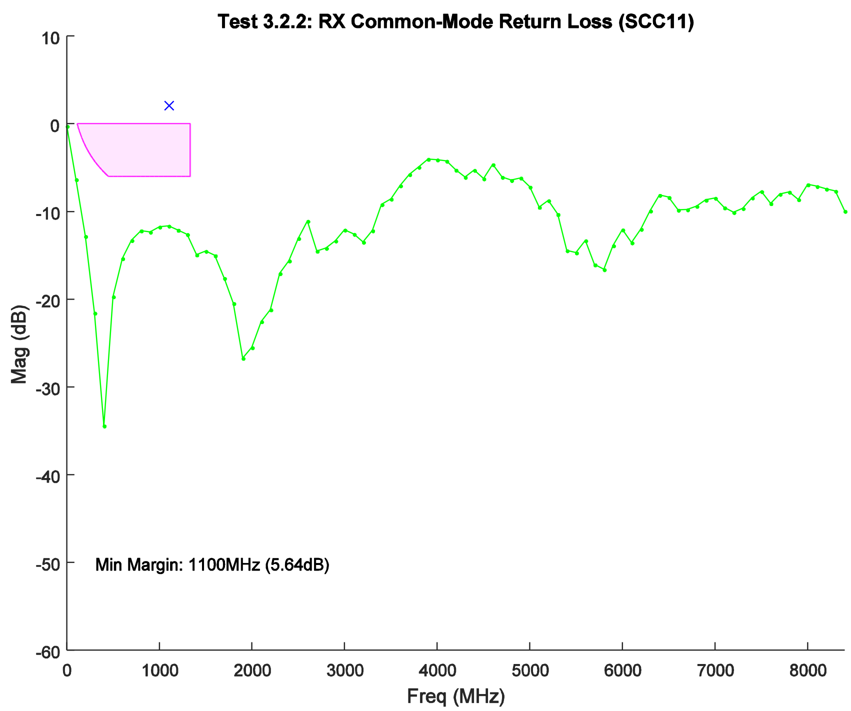
Clock Lane: Differential Impedance Profile and Return Loss (ZID = 100 ohms) (1499 Mbps, 150ps t_R)



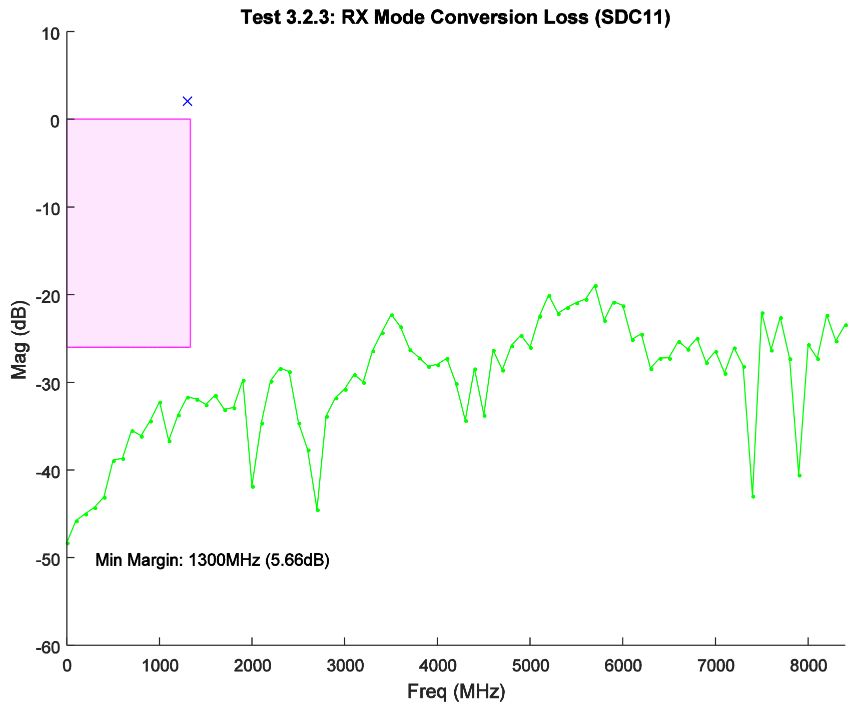


Clock Lane: Common-Mode Impedance Profile and Return Loss (1499 Mbps, 150ps t_R)

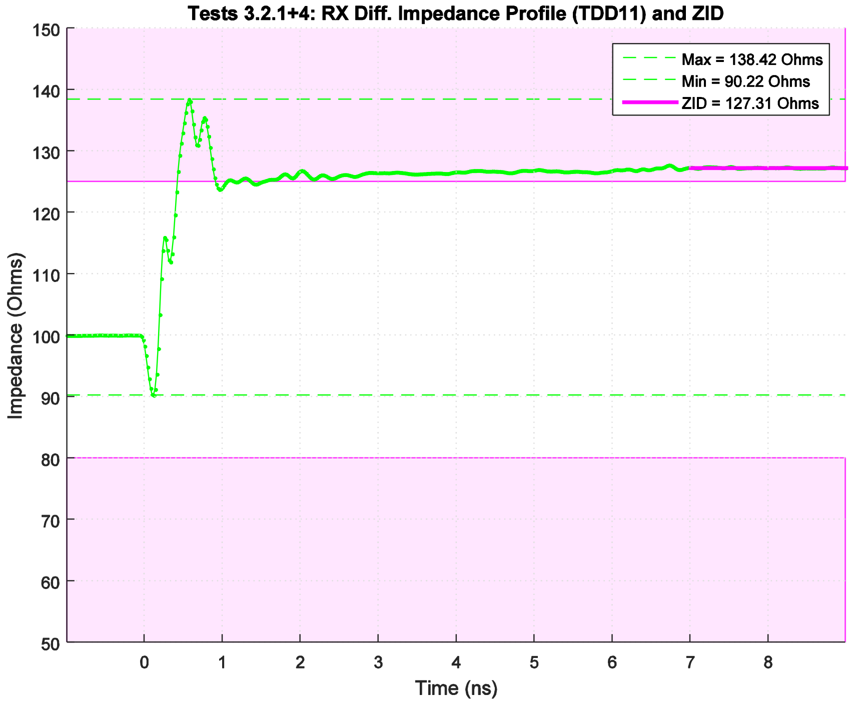


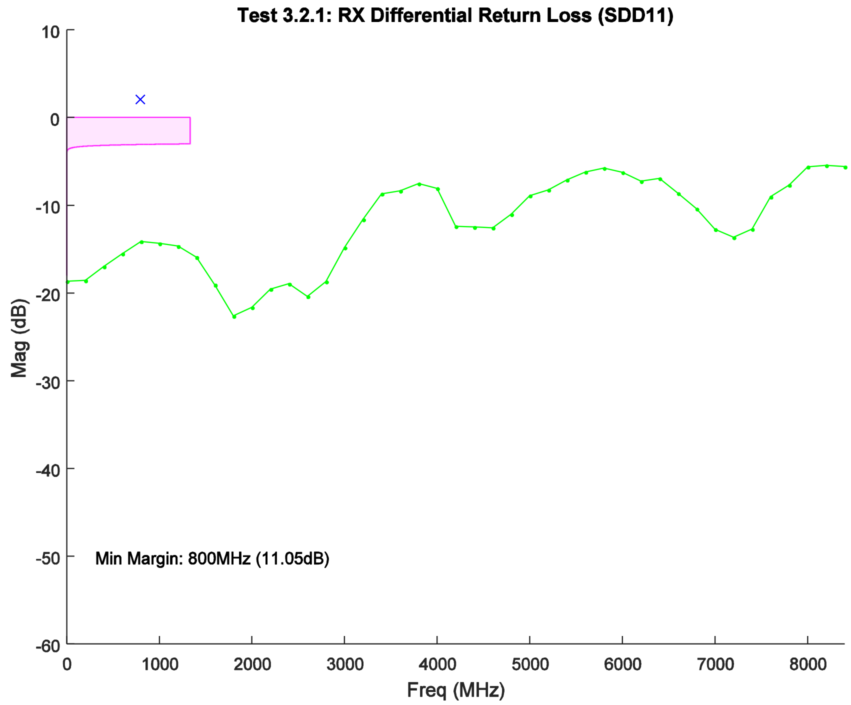


Clock Lane: Differential Impedance Imbalance (1499 Mbps, 150ps t_R)

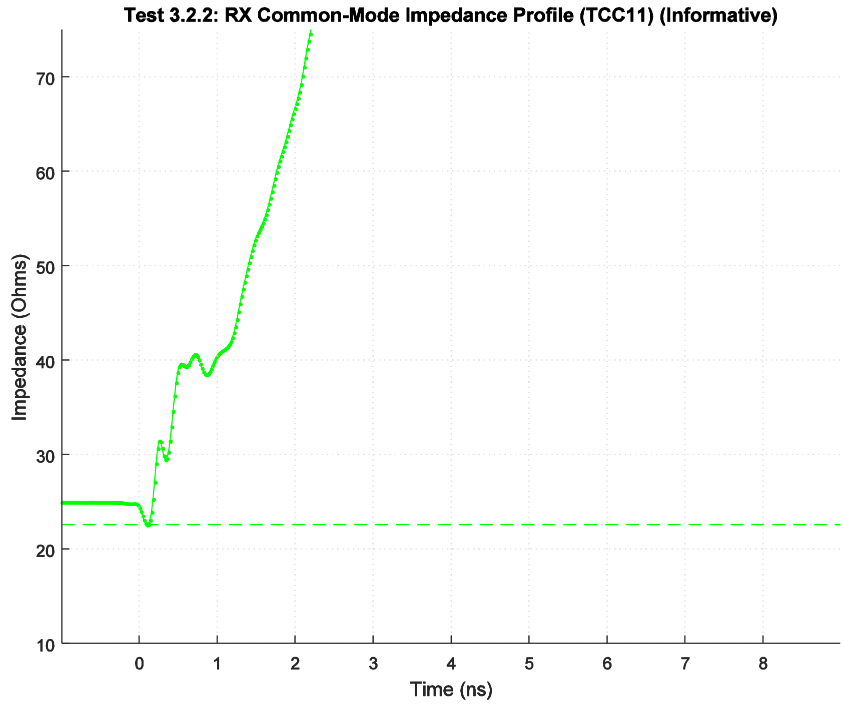


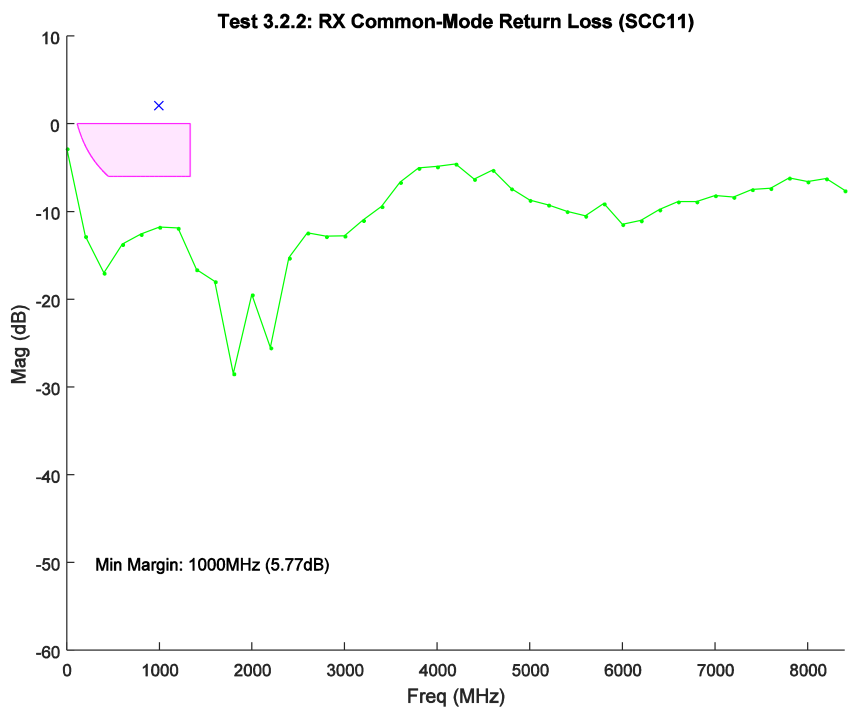
Data Lane 2: Differential Impedance Profile and Return Loss (ZID = 125 ohms) (1499 Mbps, 150ps t_R)



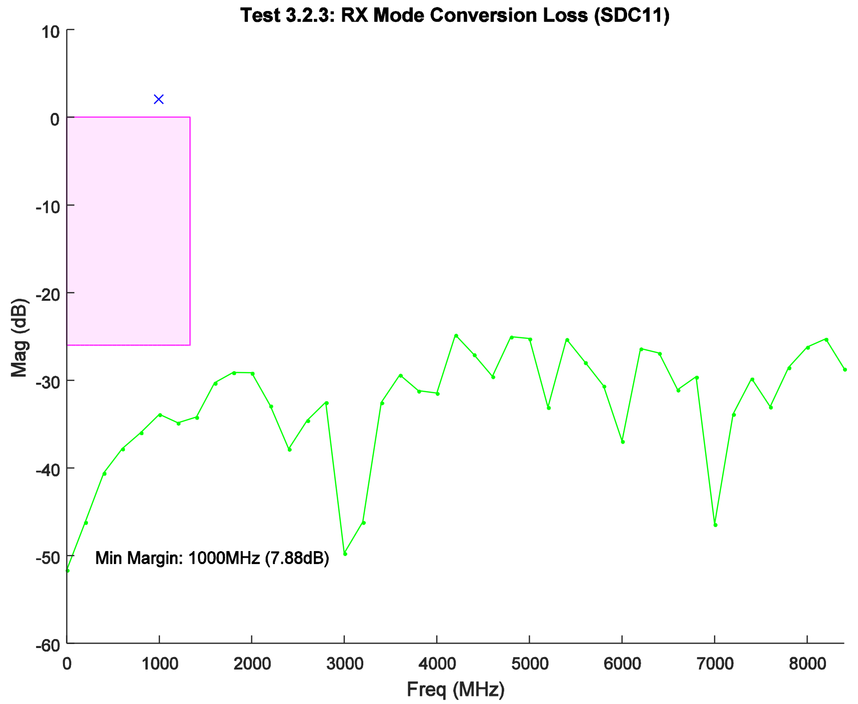


Data Lane 2: Common-Mode Impedance Profile and Return Loss (1499 Mbps, 150ps t_R)

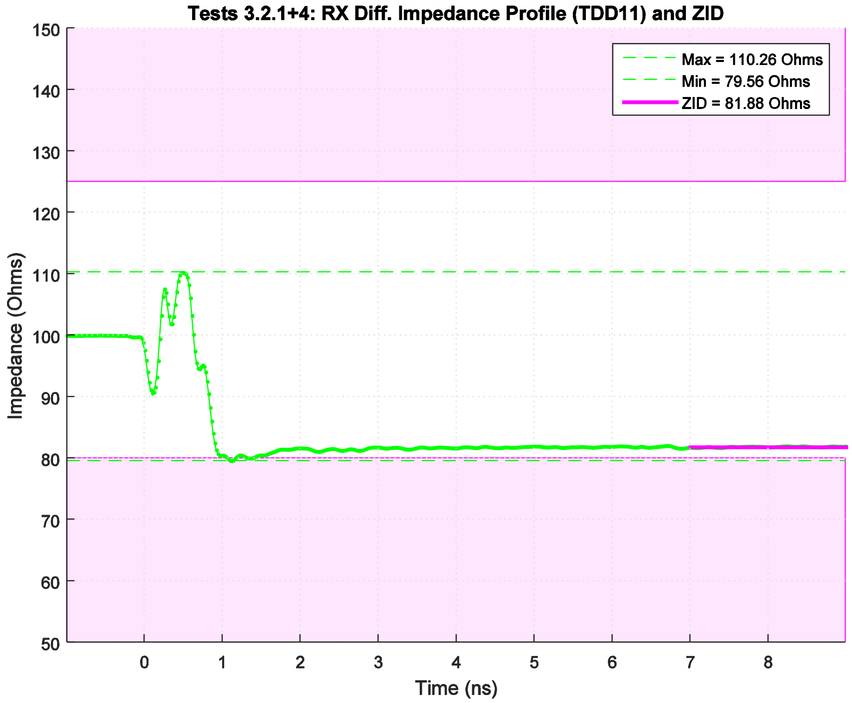


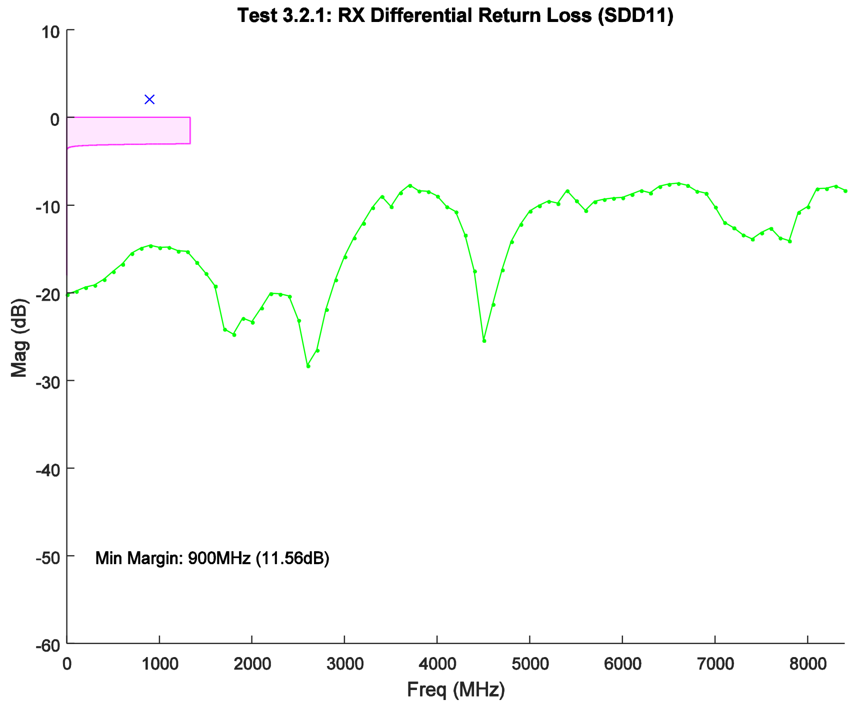


Data Lane 2: Differential Impedance Imbalance (1499 Mbps, 150ps t_R)

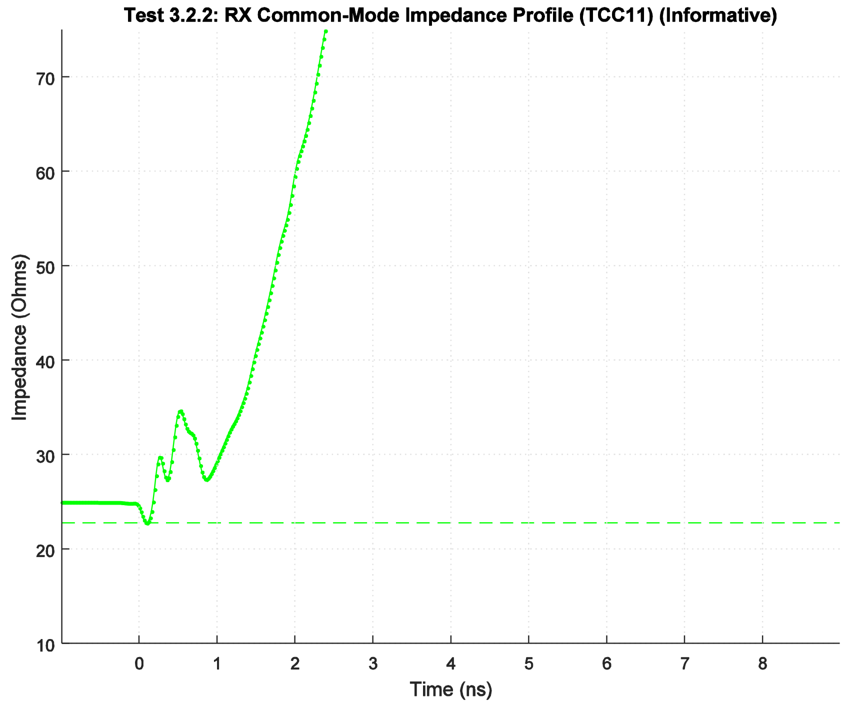


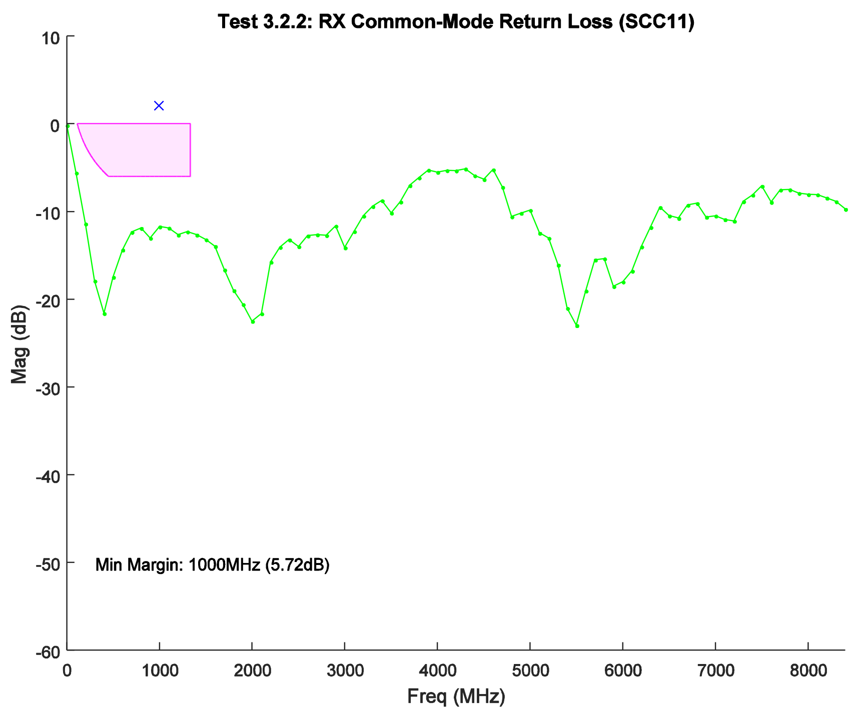
Data Lane 3: Differential Impedance Profile and Return Loss (ZID = 80 ohms) (1499 Mbps, 150ps t_R)



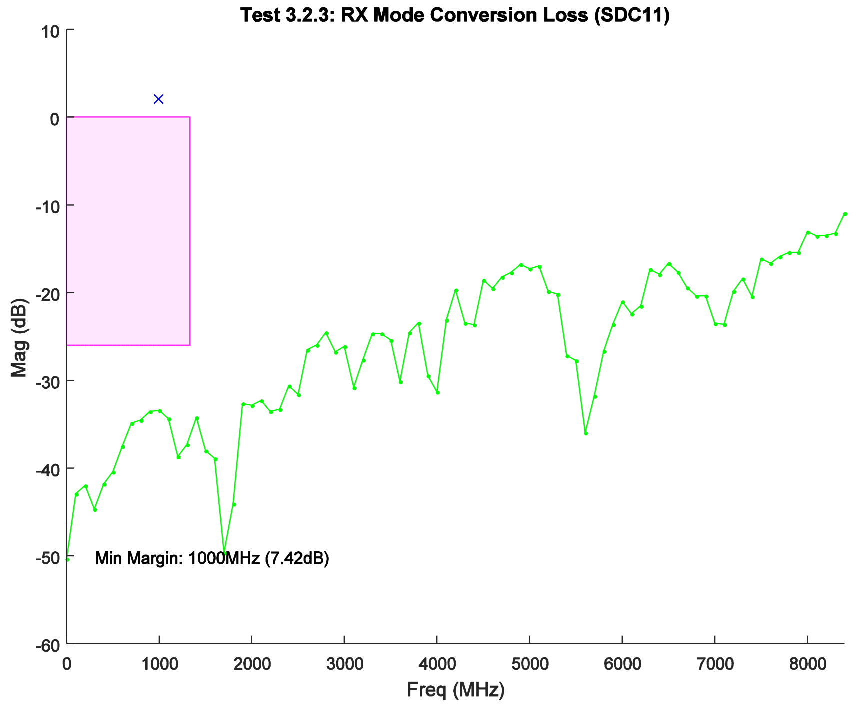


Data Lane 3: Common-Mode Impedance Profile and Return Loss (1499 Mbps, 150ps t_R)

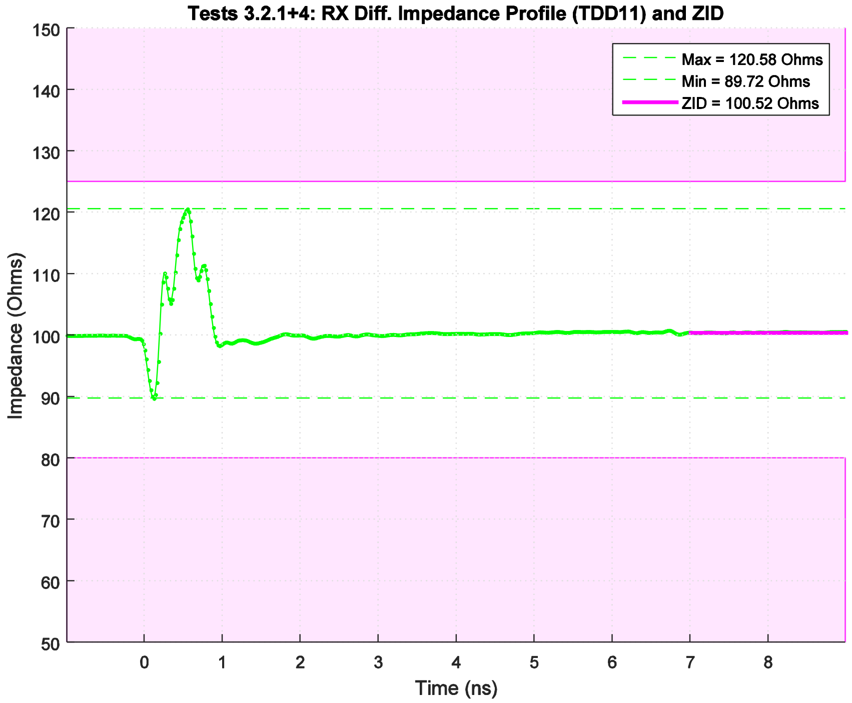


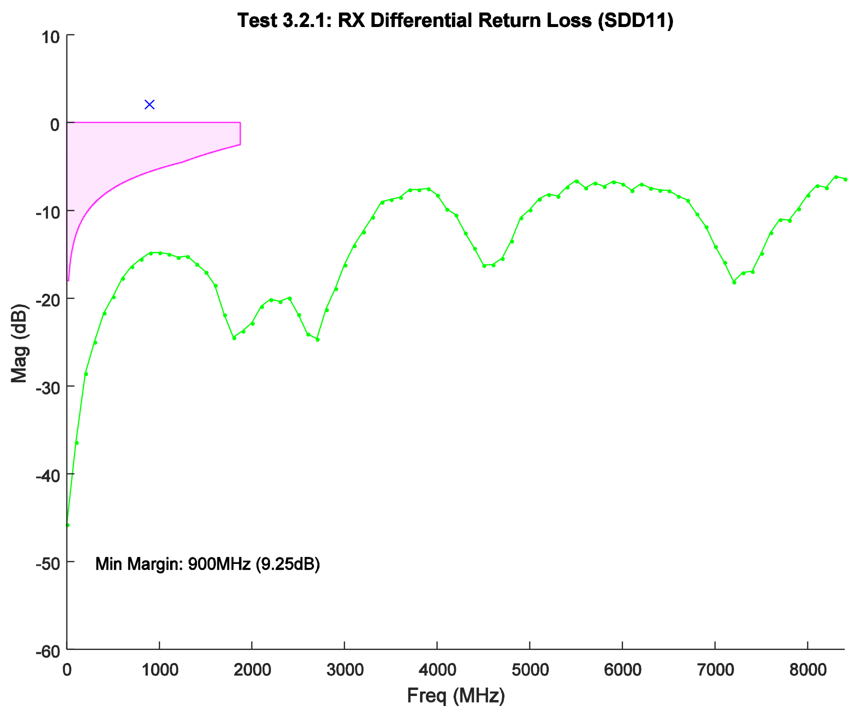


Data Lane 3: Differential Impedance Imbalance (1499 Mbps, 150ps t_R)

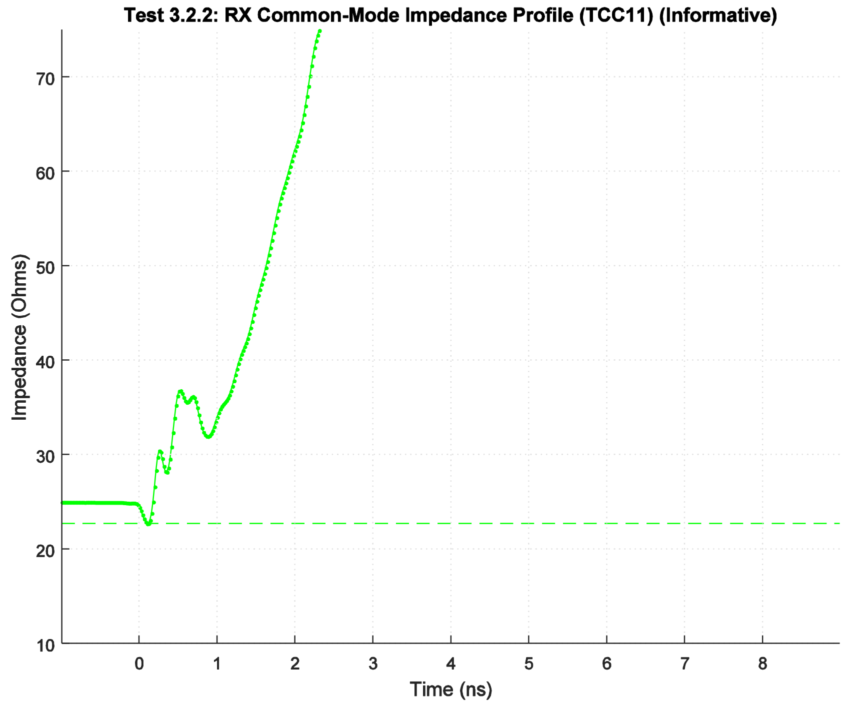


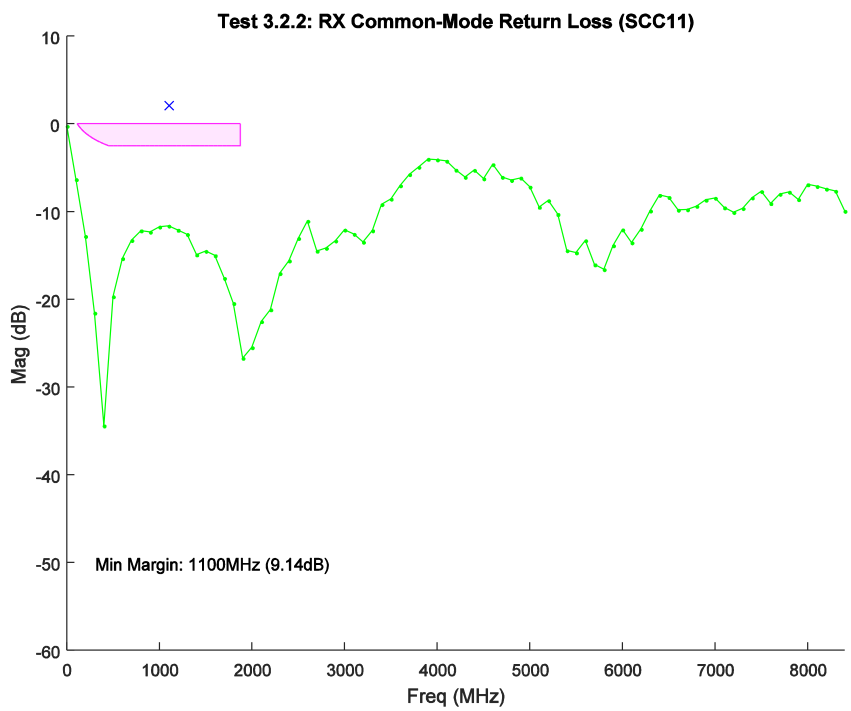
Clock Lane: Differential Impedance Profile and Return Loss (ZID = 100 ohms) (2500 Mbps, 50ps t_R)



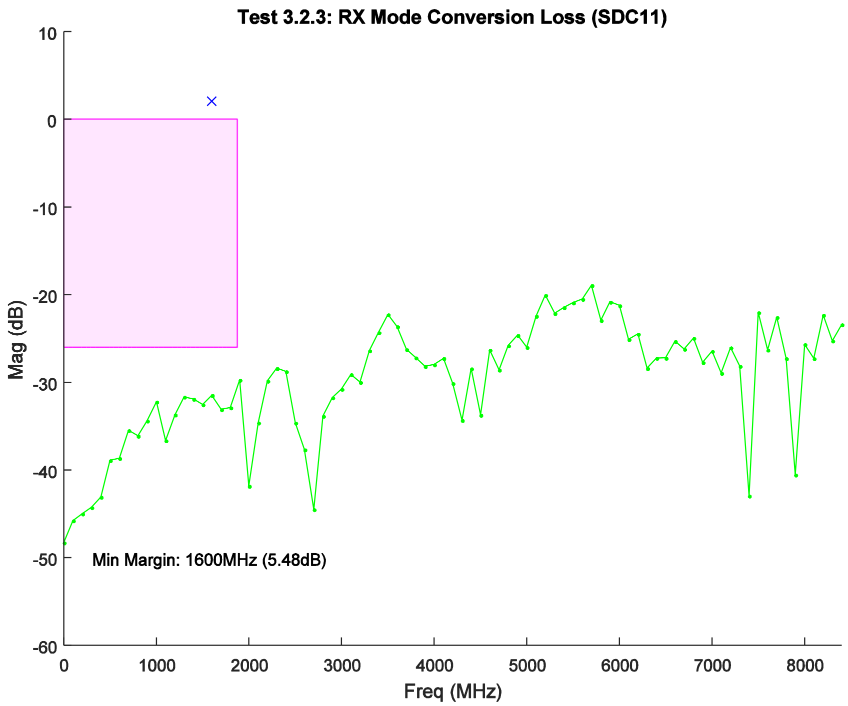


Clock Lane: Common-Mode Impedance Profile and Return Loss (2500 Mbps, 50ps t_R)

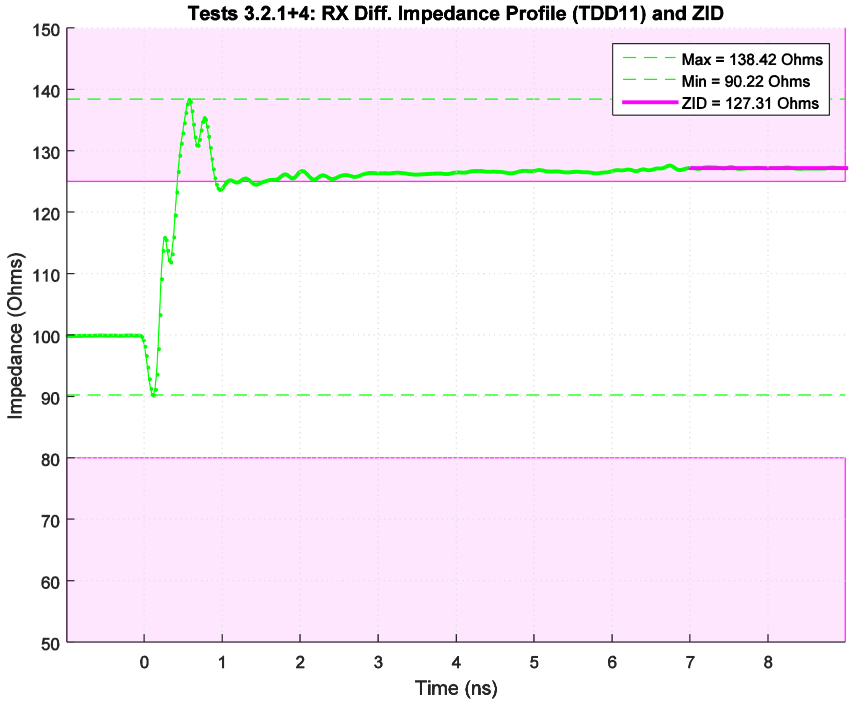


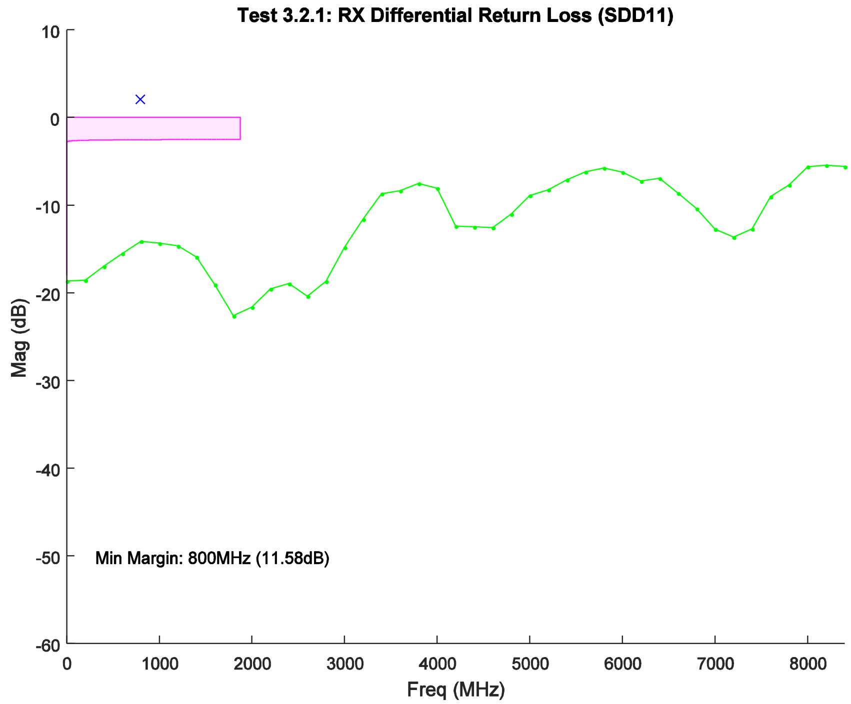


Clock Lane: Differential Impedance Imbalance (2500 Mbps, 50ps t_R)

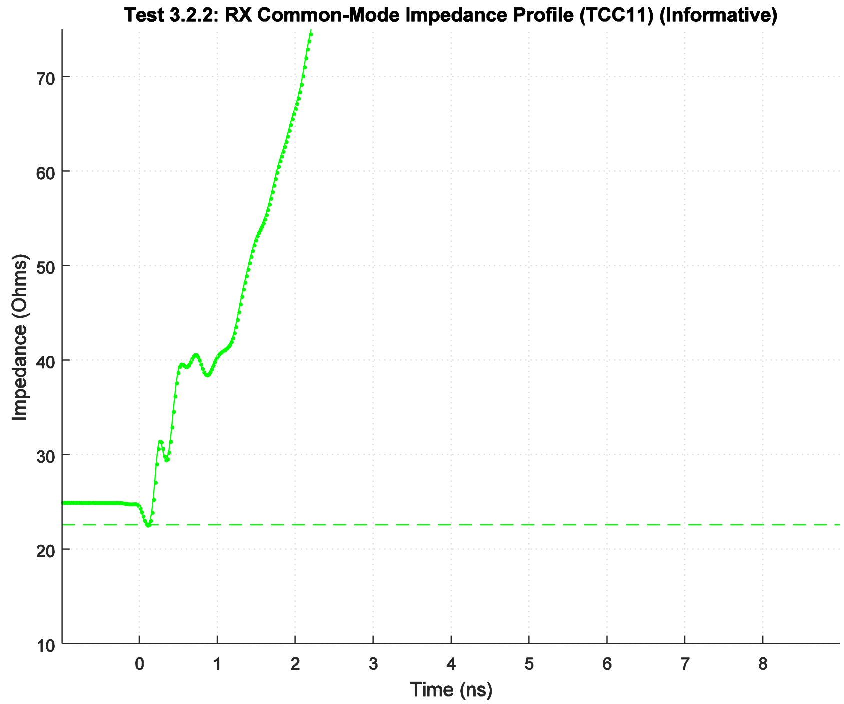


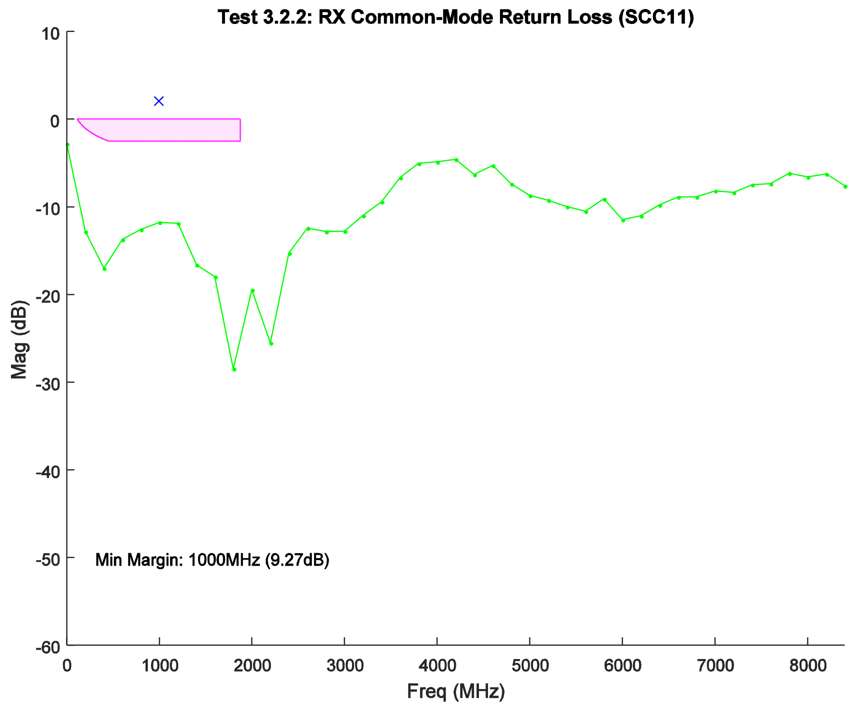
Data Lane 2: Differential Impedance Profile and Return Loss (ZID = 125 ohms) (2500 Mbps, 50ps t_R)



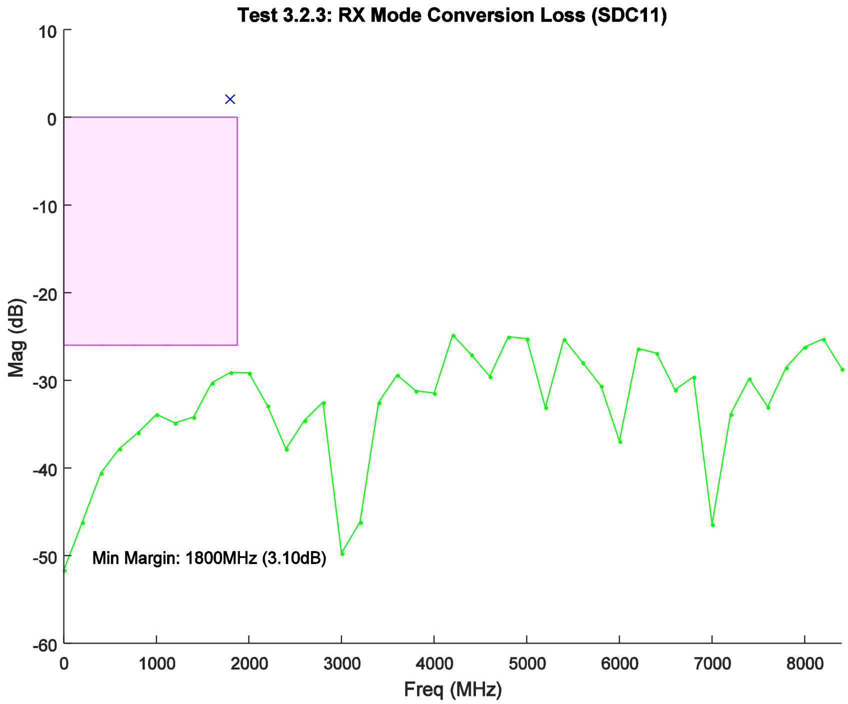


Data Lane 2: Common-Mode Impedance Profile and Return Loss (2500 Mbps, 50ps t_R)

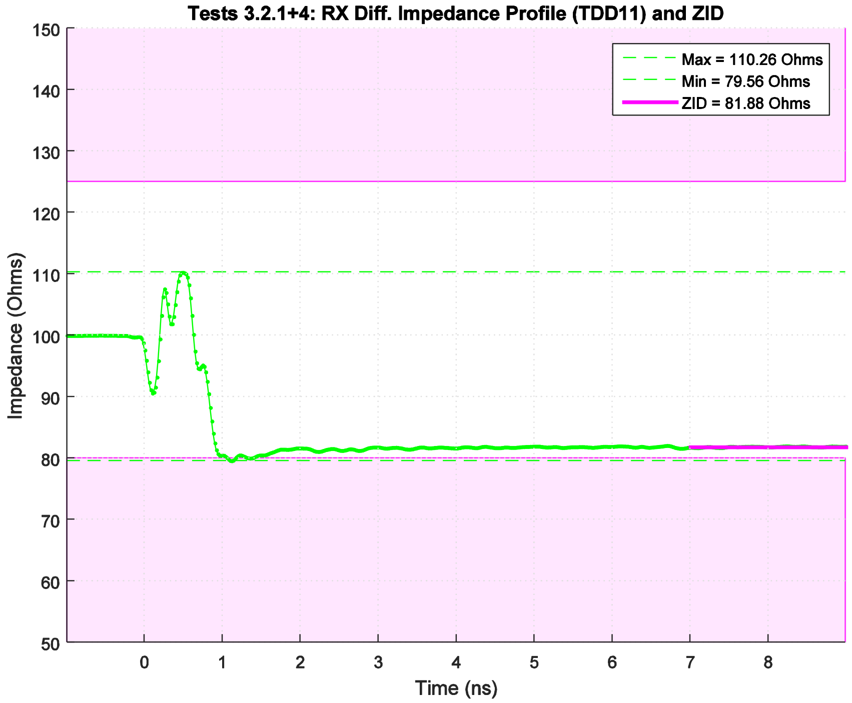


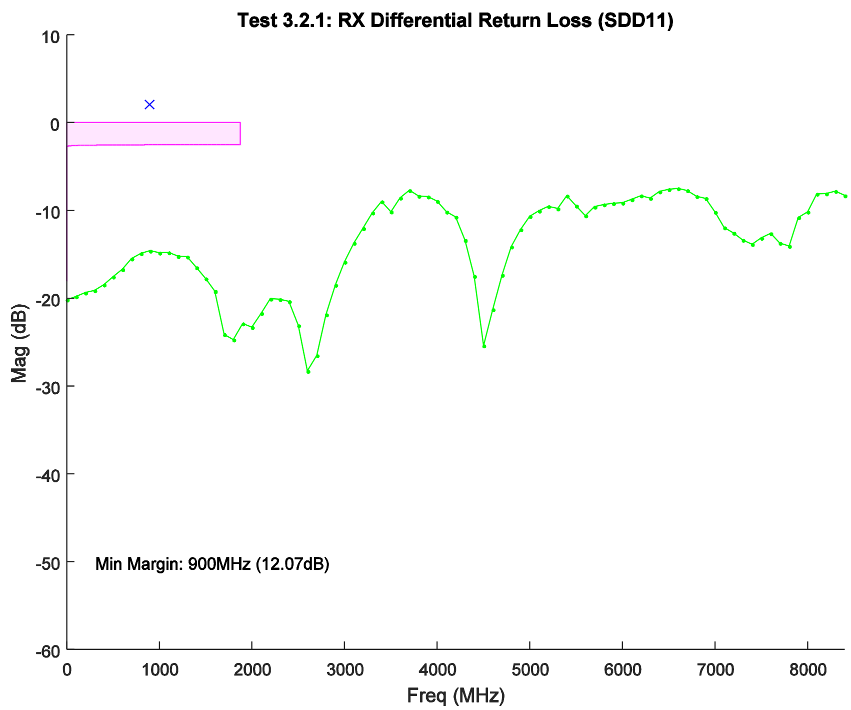


Data Lane 2: Differential Impedance Imbalance (2500 Mbps, 50ps t_R)

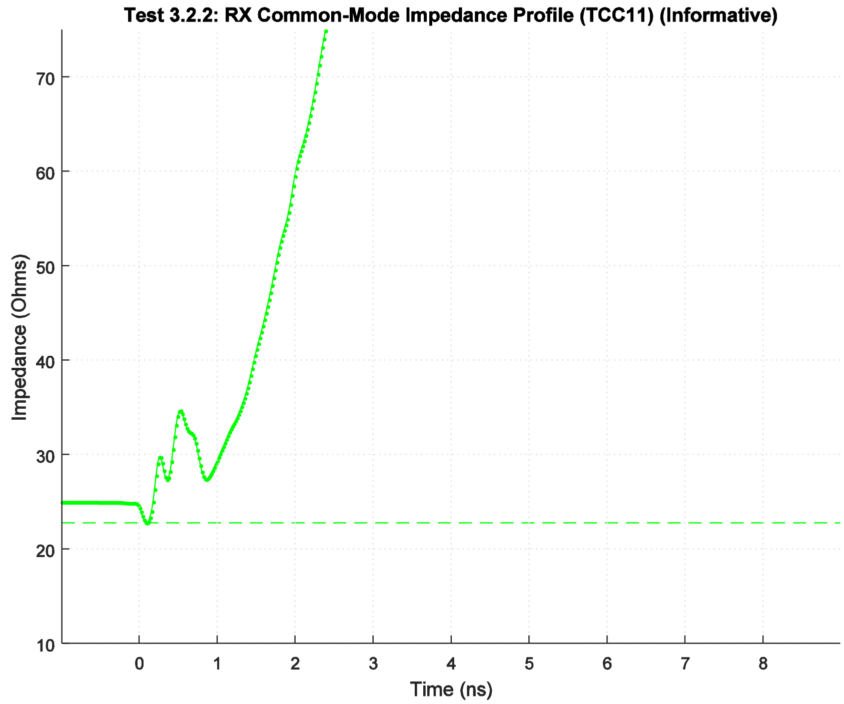


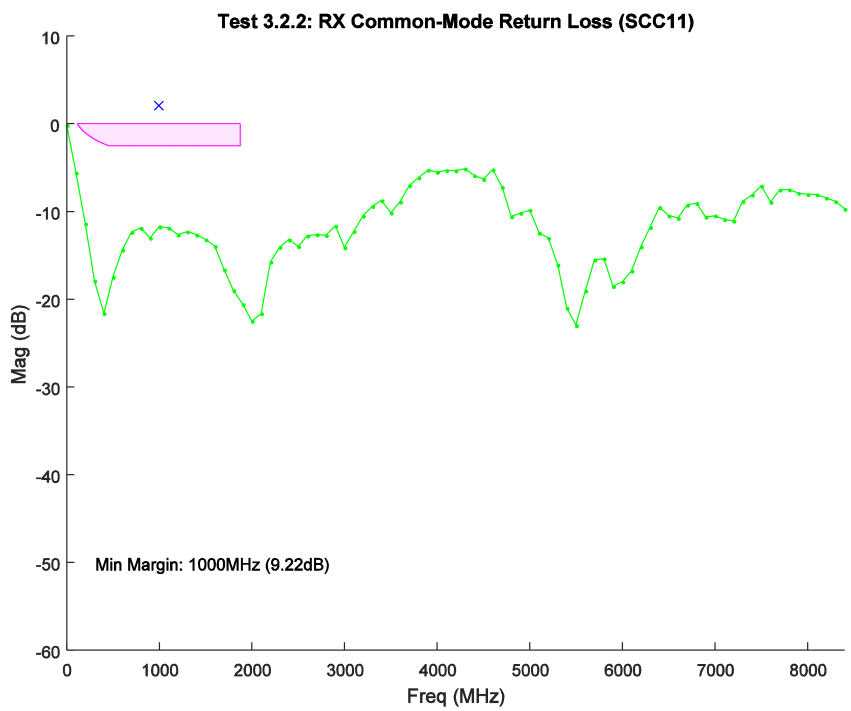
Data Lane 3: Differential Impedance Profile and Return Loss (ZID = 80 ohms) (2500 Mbps, 50ps t_R)





Data Lane 3: Common-Mode Impedance Profile and Return Loss (2500 Mbps, 50ps t_R)





Data Lane 3: Differential Impedance Imbalance (2500 Mbps, 50ps t_R)