



# UNH-IOL MIPI Alliance Test Program D-PHY RX S-Parameter Test Report

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September 27, 2010

Engineer Name  
Sample Company, Inc.  
1010 Mobile Way  
San Jose, CA 95101

Mr. Engineer:

Enclosed are the test results from the D-PHY RX S-Parameter Conformance testing performed on the:

Sample Company Model 4544 LCD Display 4-Lane DSI Receiver

The testing was performed according to v0.98 of the MIPI Alliance D-PHY Conformance Test Suite, which is available to MIPI Alliance Members at:

<https://members.mipi.org/mipi-testing/workspace/StartPage>

Any issues observed during testing are listed below:

- **Failure of Test 3.2.1: HS-RX Differential Return Loss (SDD11)**
- **Failure of Test 3.2.2: HS-RX Common-Mode Return Loss (SCC11)**

Please feel free to contact me via email at [aab@iol.unh.edu](mailto:aab@iol.unh.edu) with any questions you may have regarding this report.

Sincerely,

A handwritten signature in black ink that reads 'Andy Baldman'. The signature is written in a cursive, slightly slanted style.

Andy Baldman

### **Digital Signature Information**

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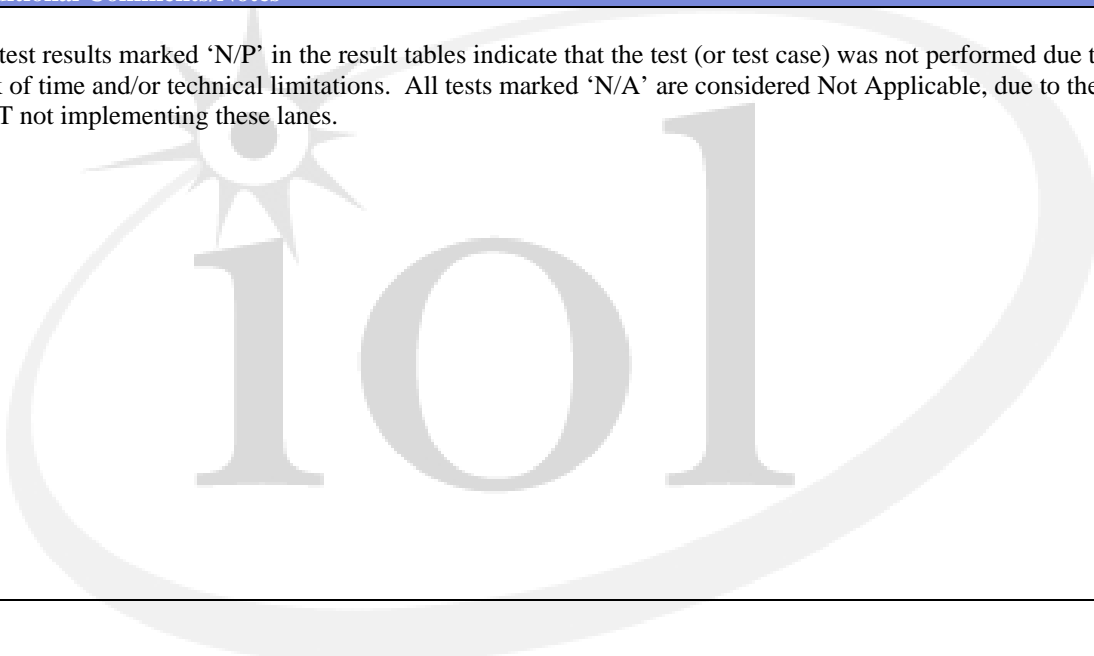
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SHA-1 Fingerprint (2010): ECFB 7FAF AB4A 0832 2408 E965 9F5C E3F2 D784 AAAB



**Table 1-0: Test Setup and DUT Configuration Information**

<b>DUT Details</b>	
Week testing was performed	20100927
Manufacturer	Sample Company
Model	Model 4544 LCD Display (4-Lane DSI Receiver)
Max. Supported HS Bit Rate	800 Mbps
Mfr. Serial Number	9876543210
Firmware Version	v1.0
Hardware Version	v0.10
Software Version	3.15
UNH-IOL ID Number	99999
<b>Test System Hardware</b>	
Time Domain Reflectometer	Agilent DCA-J 86100C, with S-parameter Option 201 and 54754A module
<b>Additional Comments/Notes</b>	
<p>All test results marked 'N/P' in the result tables indicate that the test (or test case) was not performed due to lack of time and/or technical limitations. All tests marked 'N/A' are considered Not Applicable, due to the DUT not implementing these lanes.</p> 	

**Table 3-2: (Section 3, Group 2): HS-RX S-Parameters**

Test/Parameter	Range	Measured	Units	Fig.
<b>Test 3.2.1: HS-RX Differential Return Loss (SDD11)</b>				
(Clock Lane): Minimum SDD11 margin	> 0	<b>-1.29</b>	dB	<a href="#">6</a>
(Data Lane 0): Minimum SDD11 margin	> 0	<b>-2.14</b>	dB	<a href="#">7</a>
(Data Lane 1): Minimum SDD11 margin	> 0	<b>-0.95</b>	dB	<a href="#">8</a>
(Data Lane 2): Minimum SDD11 margin	> 0	<b>-1.59</b>	dB	<a href="#">9</a>
(Data Lane 3): Minimum SDD11 margin	> 0	<b>-1.58</b>	dB	<a href="#">10</a>
<b>Test 3.2.2: HS-RX Common-Mode Return Loss (SCC11)</b>				
(Clock Lane): Minimum SCC11 margin	> 0	<b>-0.82</b>	dB	<a href="#">16</a>
(Data Lane 0): Minimum SCC11 margin	> 0	<b>1.08</b>	dB	<a href="#">17</a>
(Data Lane 1): Minimum SCC11 margin	> 0	<b>0.43</b>	dB	<a href="#">18</a>
(Data Lane 2): Minimum SCC11 margin	> 0	<b>-0.26</b>	dB	<a href="#">19</a>
(Data Lane 3): Minimum SCC11 margin	> 0	<b>-0.37</b>	dB	<a href="#">20</a>
<b>Test 3.2.3: HS-RX Mode Conversion Limits (SDC11)</b>				
(Clock Lane): Minimum SDC11 margin	> 0	<b>1.29</b>	dB	<a href="#">31</a>
(Data Lane 0): Minimum SDC11 margin	> 0	<b>2.89</b>	dB	<a href="#">32</a>
(Data Lane 1): Minimum SDC11 margin	> 0	<b>5.44</b>	dB	<a href="#">33</a>
(Data Lane 2): Minimum SDC11 margin	> 0	<b>3.27</b>	dB	<a href="#">34</a>
(Data Lane 3): Minimum SDC11 margin	> 0	<b>2.72</b>	dB	<a href="#">35</a>
<b>Test 3.2.4: HS-RX DC Differential Input Impedance (<math>Z_{ID}</math>)</b>				
(Clock Lane): $Z_{ID}$	80 / 125	<b>107.06</b>	Ohms	<a href="#">1</a>
(Data Lane 0): $Z_{ID}$	80 / 125	<b>106.29</b>	Ohms	<a href="#">2</a>
(Data Lane 1): $Z_{ID}$	80 / 125	<b>106.57</b>	Ohms	<a href="#">3</a>
(Data Lane 2): $Z_{ID}$	80 / 125	<b>105.65</b>	Ohms	<a href="#">4</a>
(Data Lane 3): $Z_{ID}$	80 / 125	<b>106.57</b>	Ohms	<a href="#">5</a>

Figure 1: HS-RX Differential Impedance Profile (TDD11) and ZID (Clock Lane)

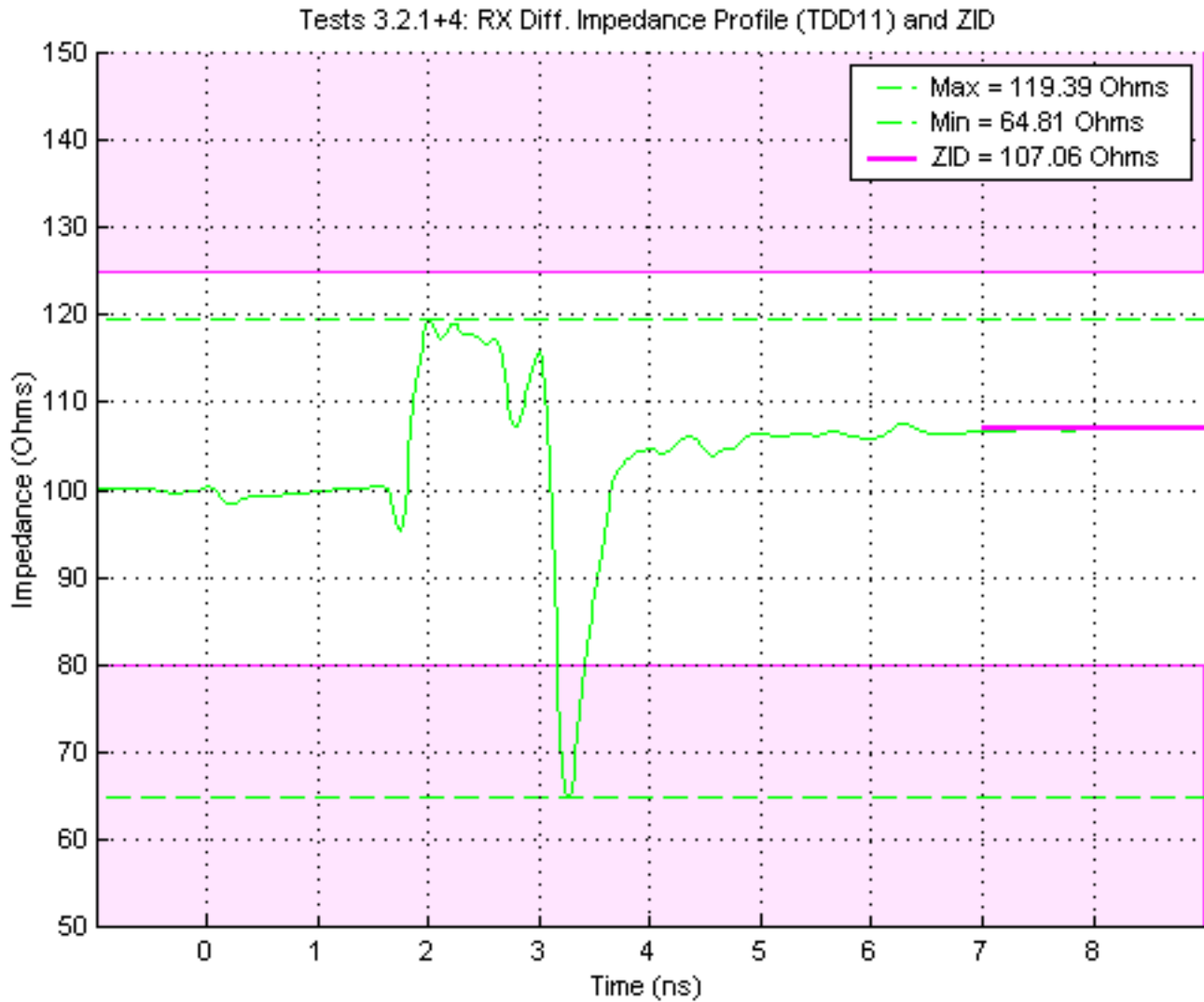


Figure 2: HS-RX Differential Impedance Profile (TDD11) and ZID (Data Lane 0)

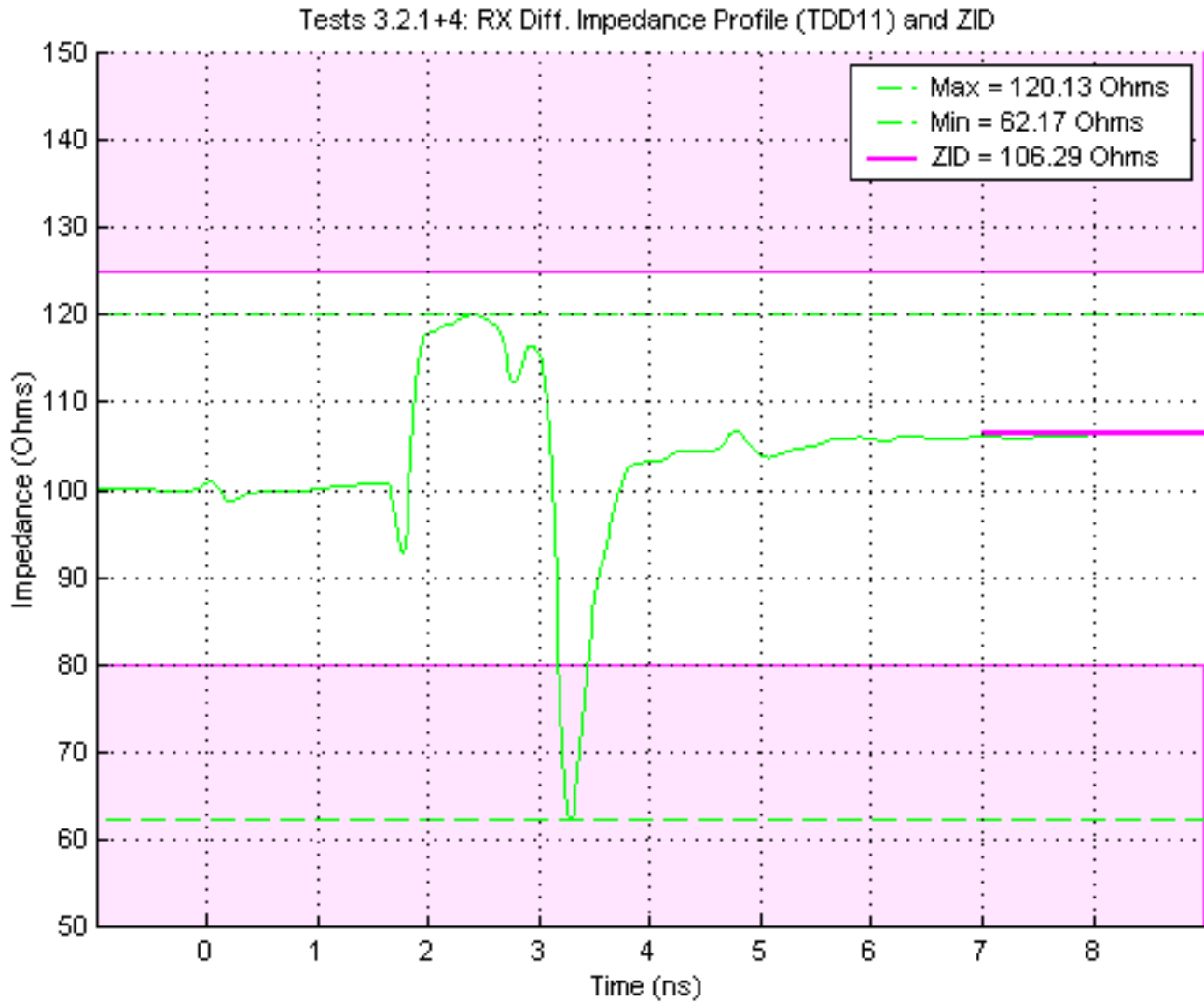


Figure 3: HS-RX Differential Impedance Profile (TDD11) and ZID (Data Lane 1)

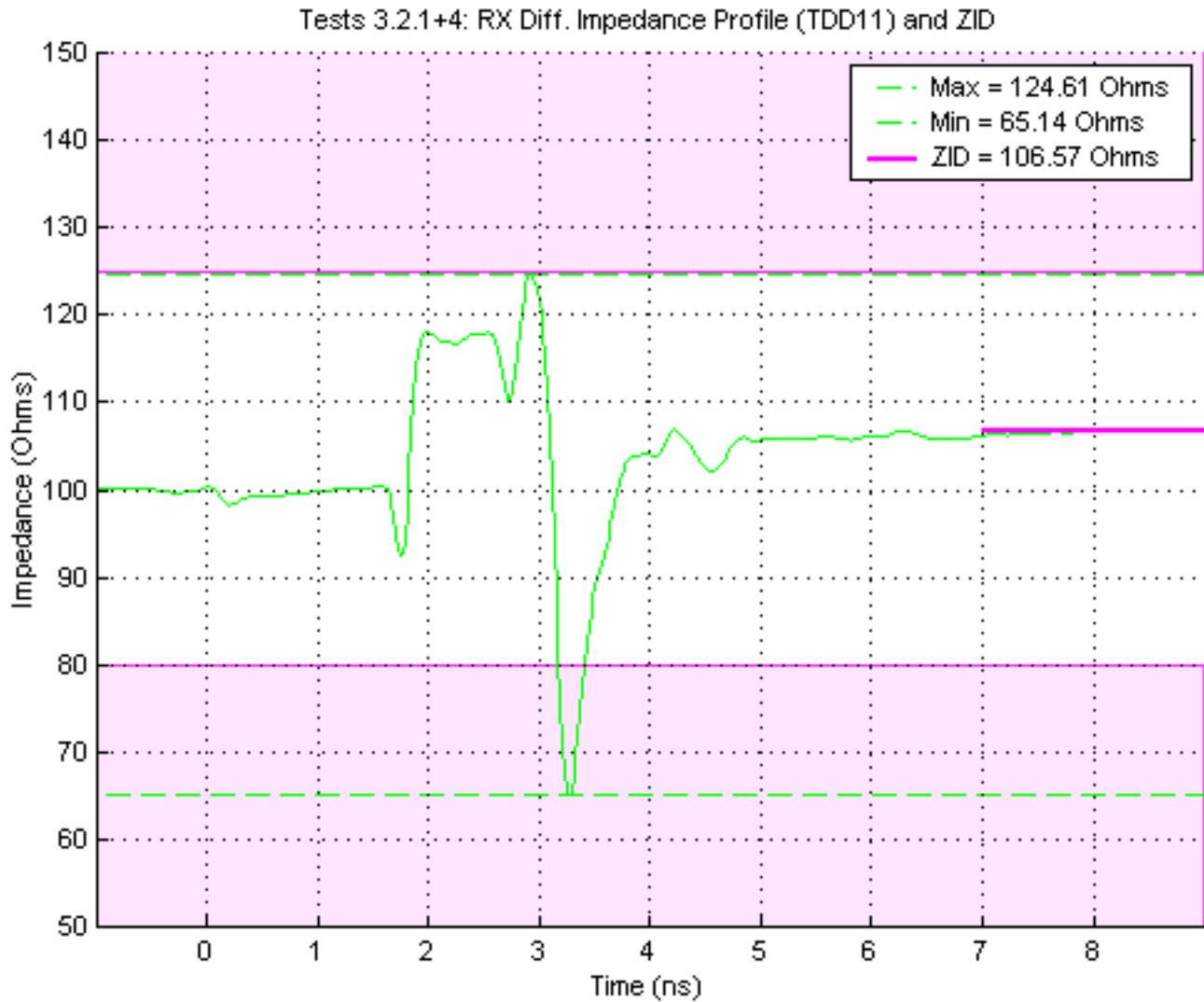


Figure 4: HS-RX Differential Impedance Profile (TDD11) and ZID (Data Lane 2)

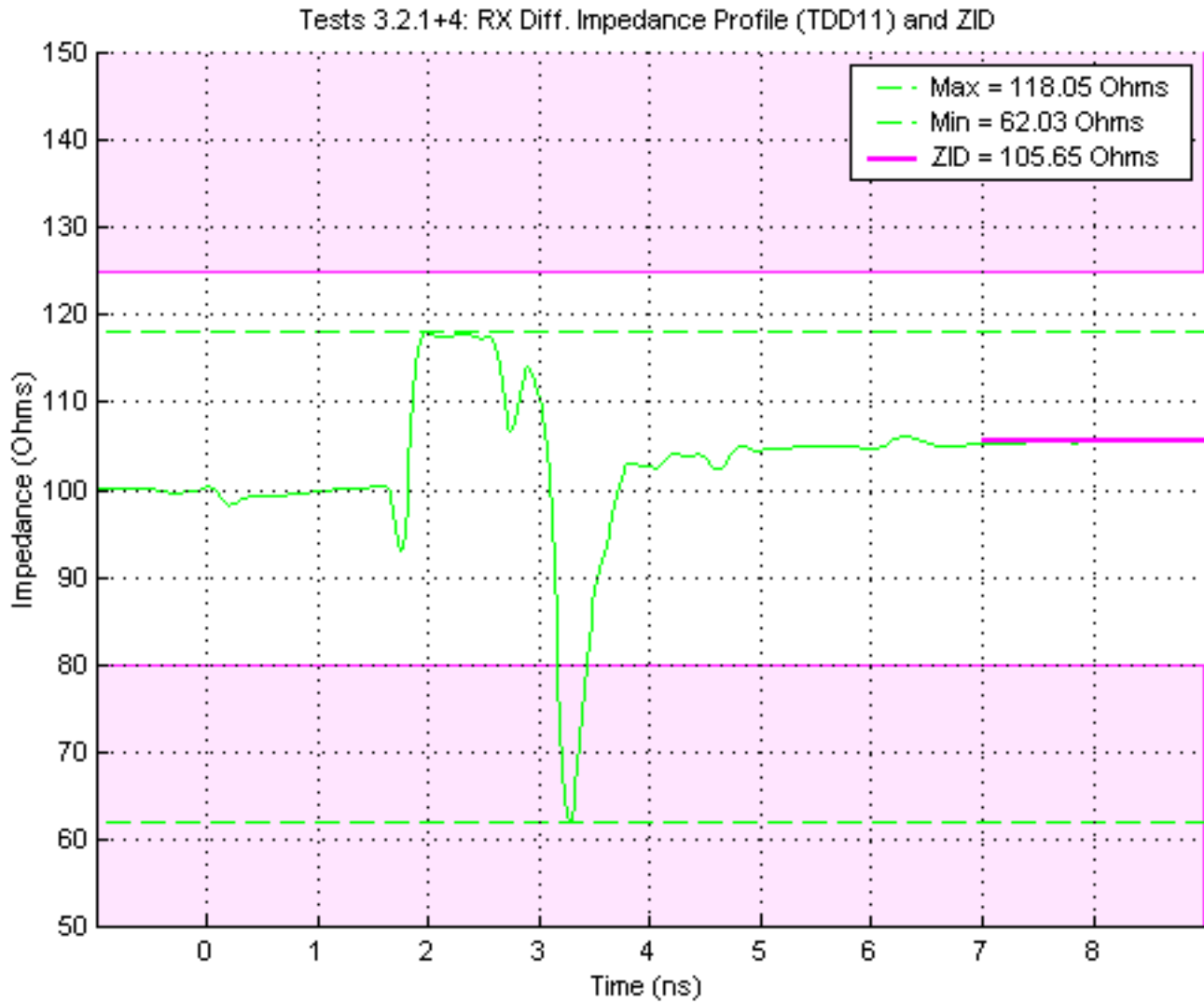




Figure 5: HS-RX Differential Impedance Profile (TDD11) and ZID (Data Lane 3)

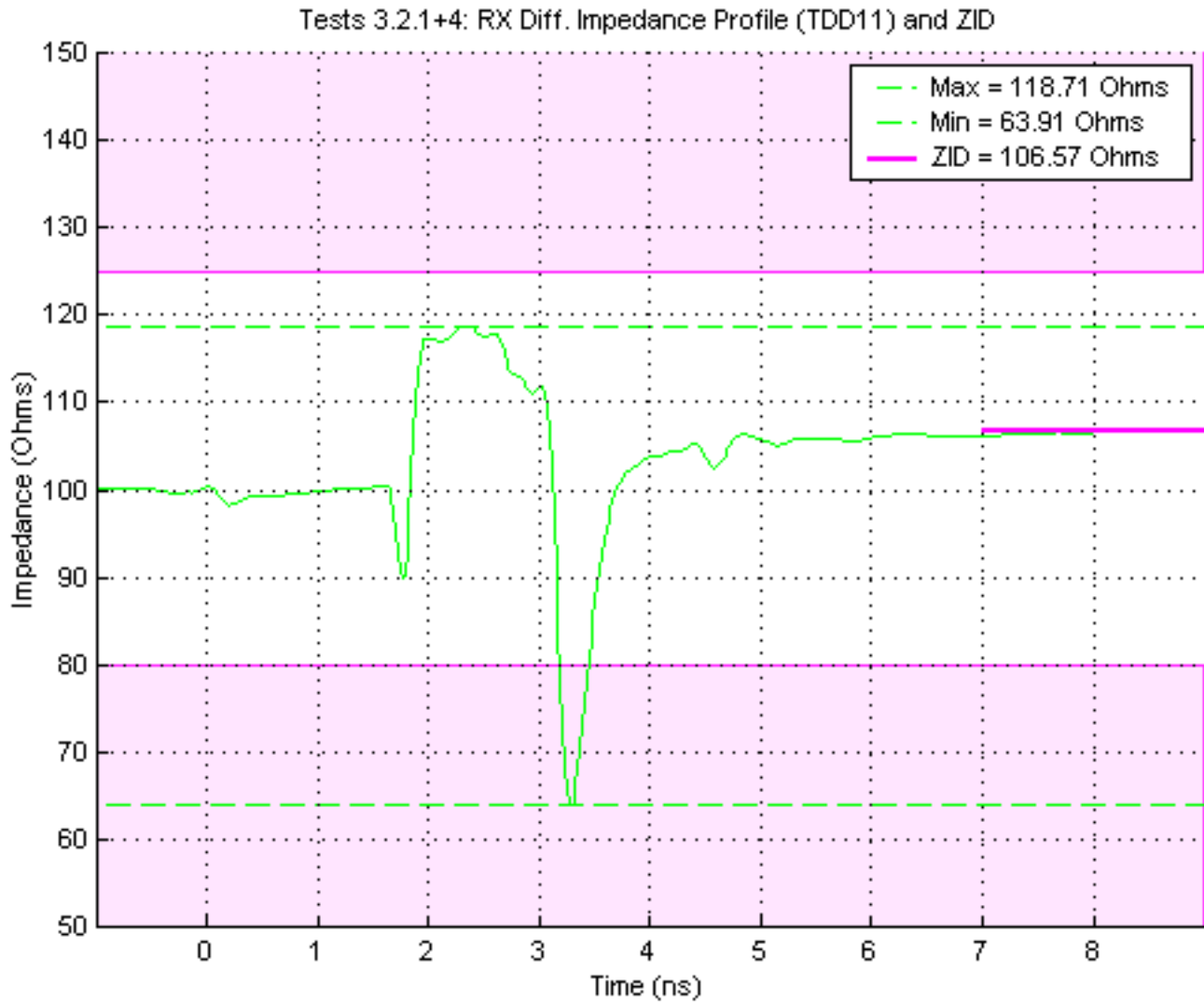


Figure 6: HS-RX Differential Return Loss (SDD11) (Clock Lane)

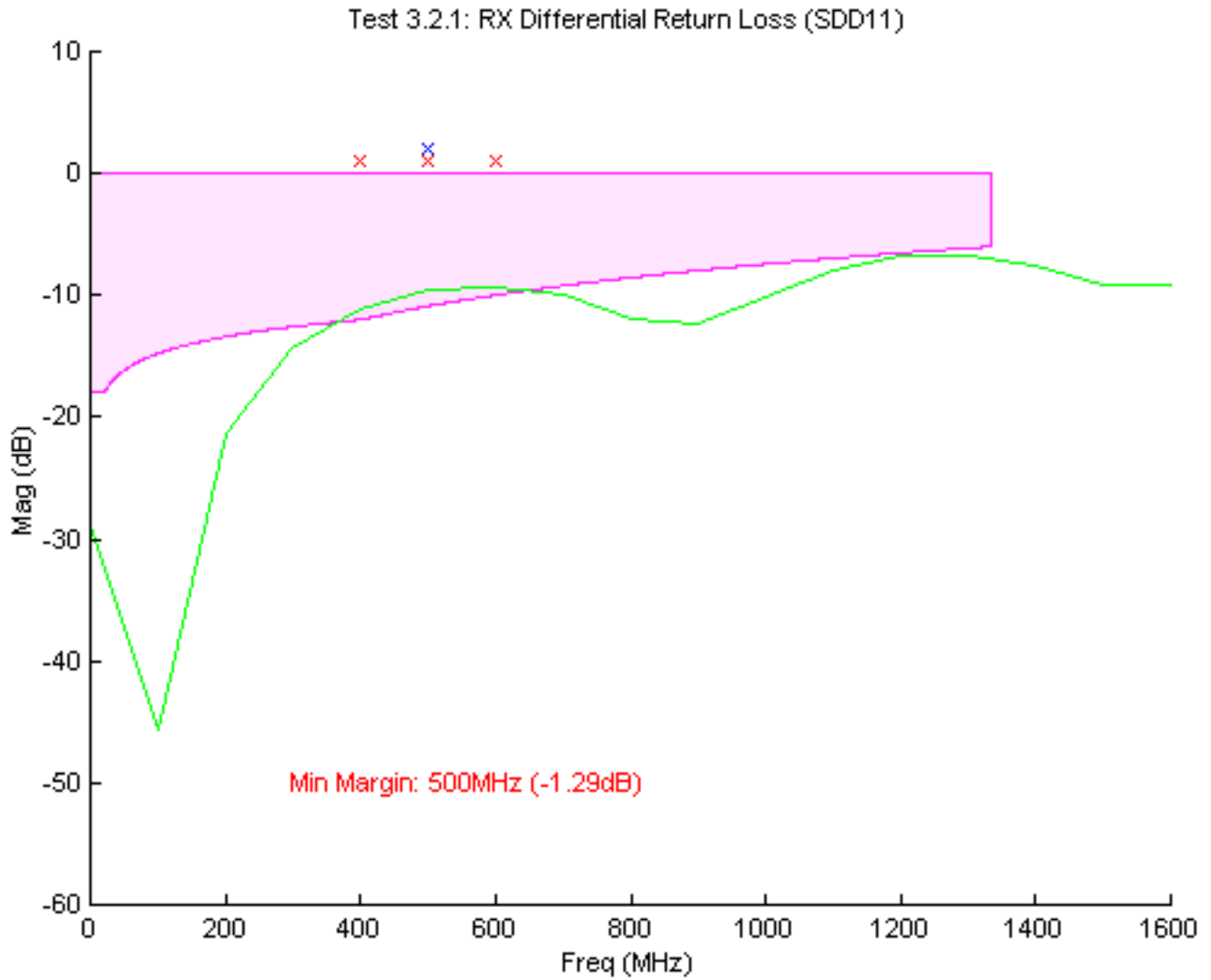


Figure 7: HS-RX Differential Return Loss (SDD11) (Data Lane 0)

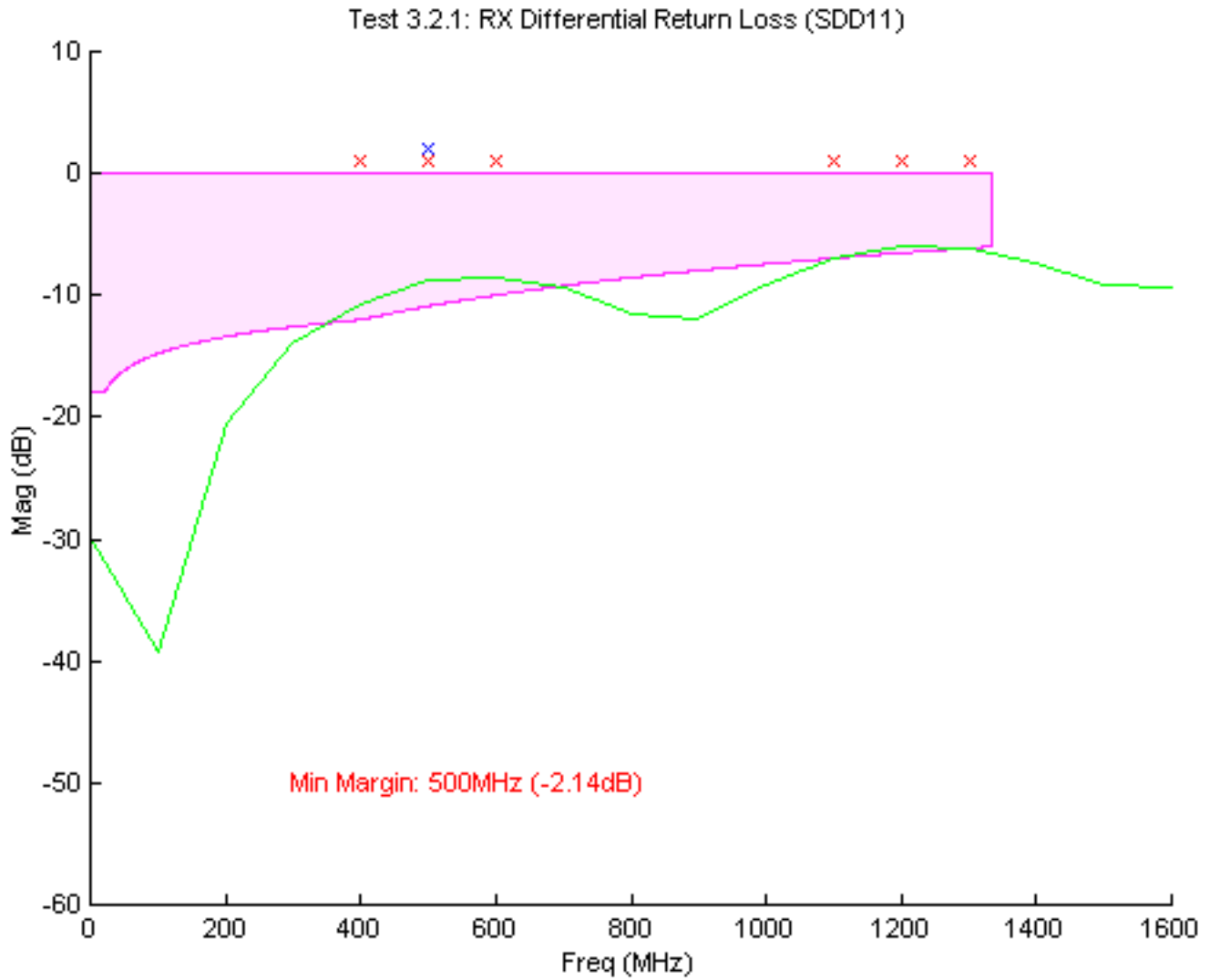


Figure 8: HS-RX Differential Return Loss (SDD11) (Data Lane 1)

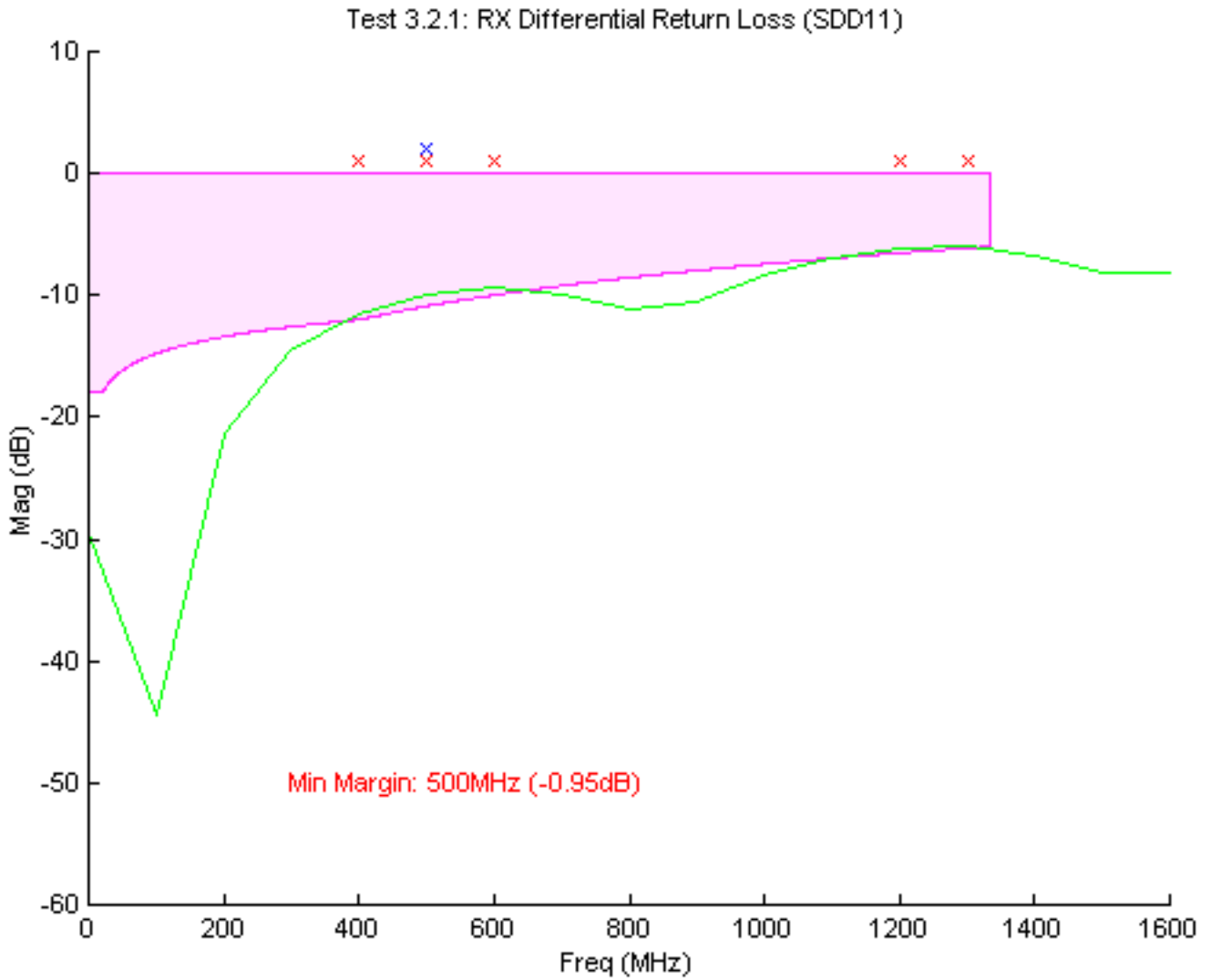


Figure 9: HS-RX Differential Return Loss (SDD11) (Data Lane 2)

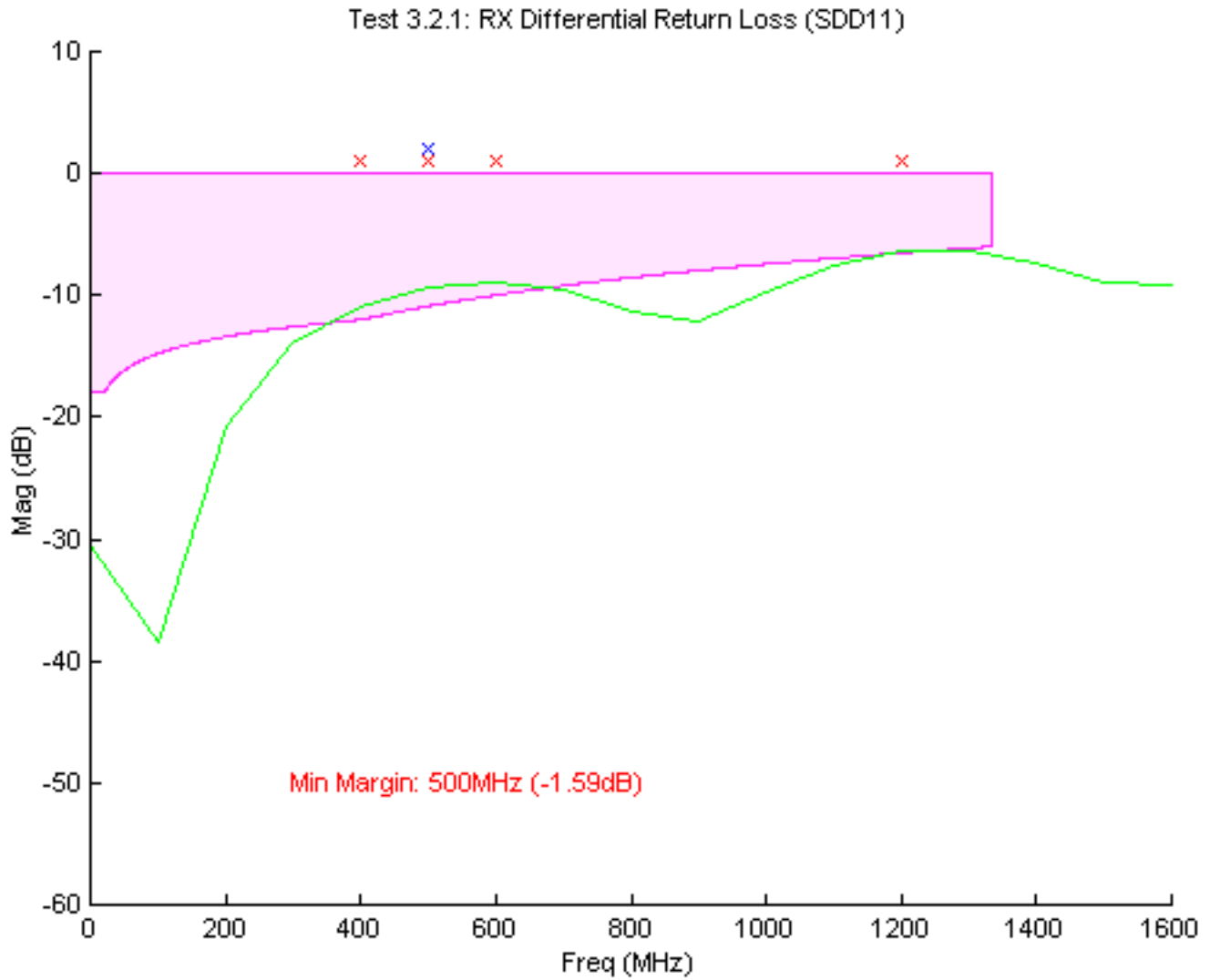


Figure 10: HS-RX Differential Return Loss (SDD11) (Data Lane 3)

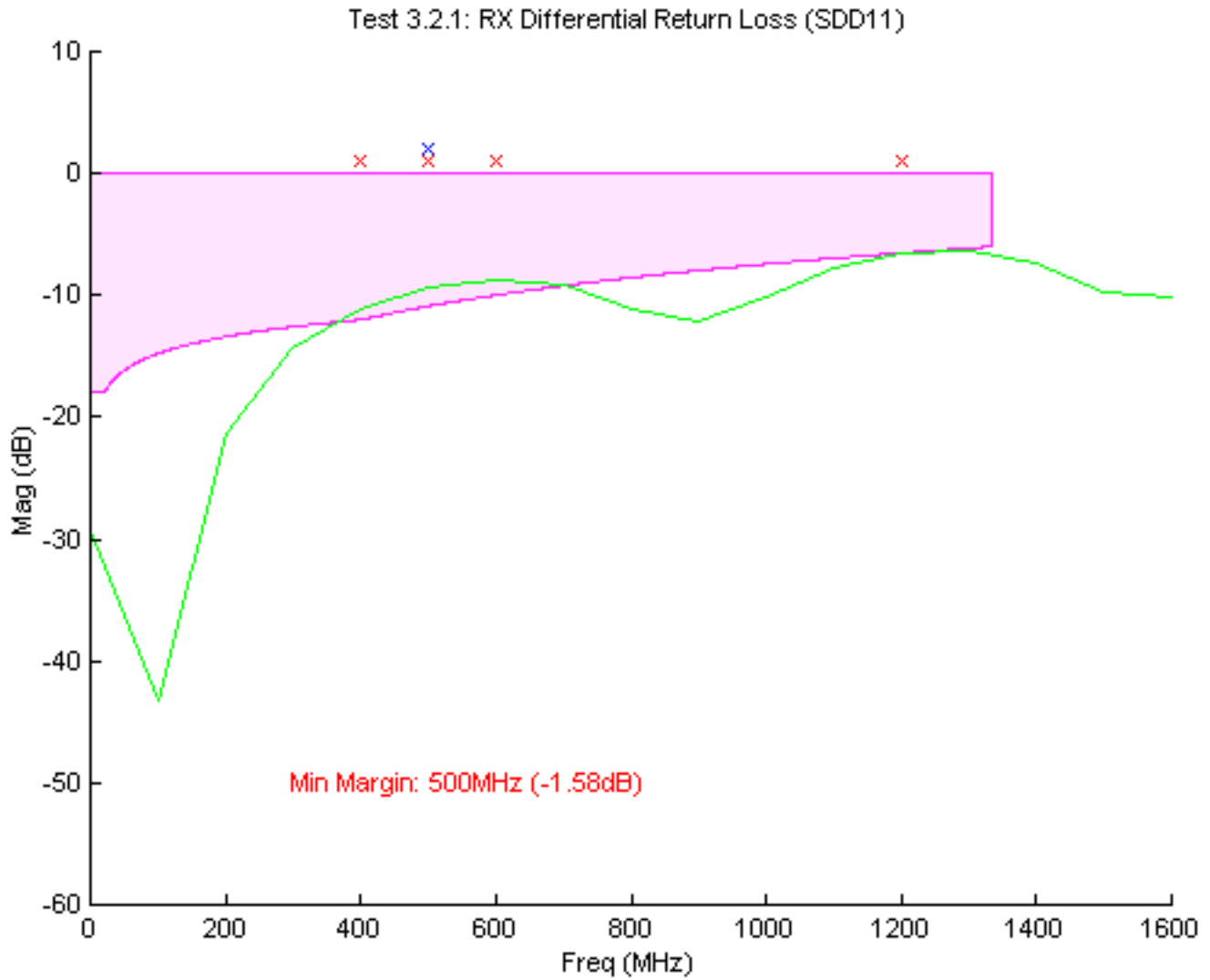


Figure 11: HS-RX Common-Mode Impedance Profile (TCC11) (Clock Lane) (Informative)

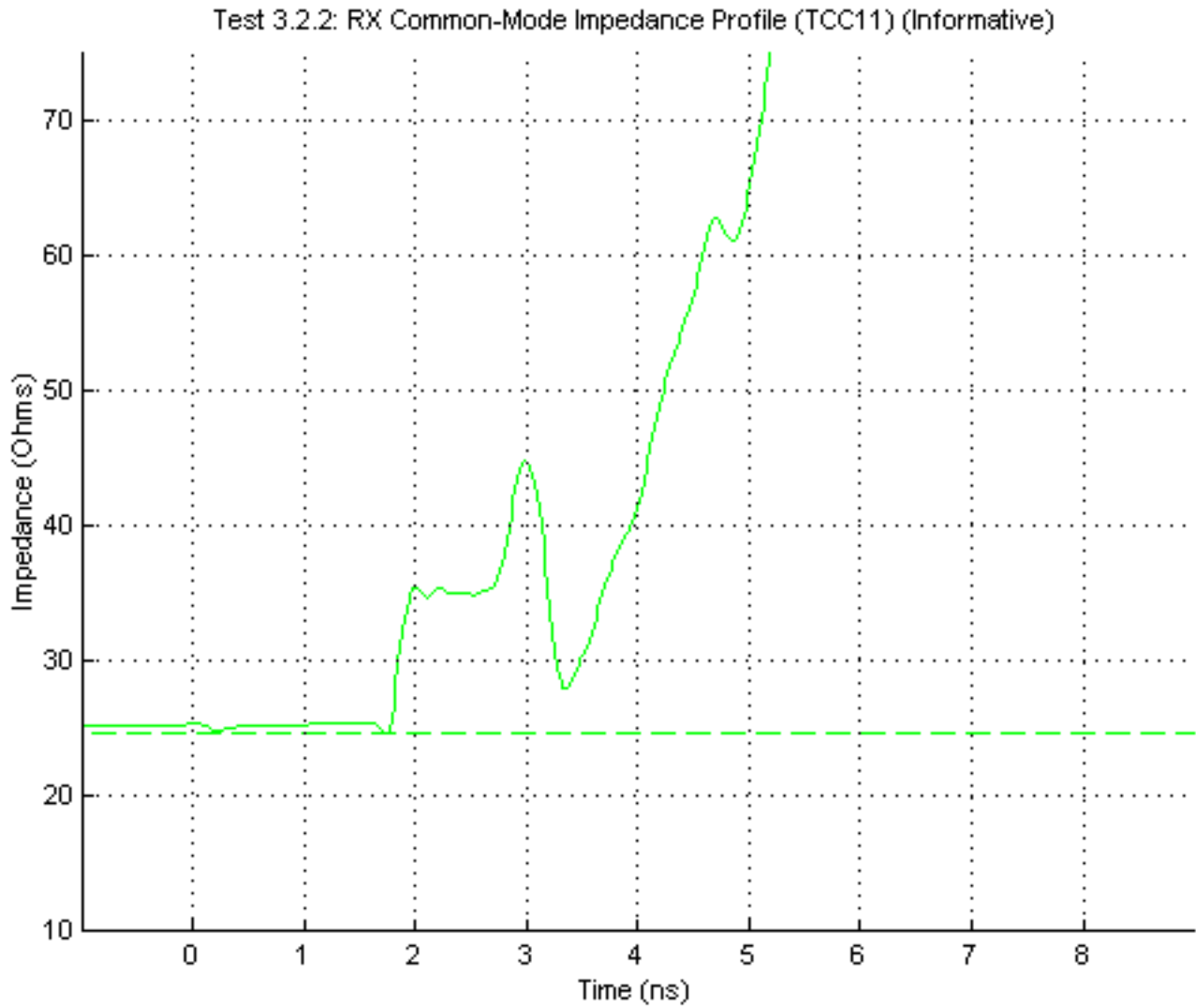


Figure 12: HS-RX Common-Mode Impedance Profile (TCC11) (Data Lane 0) (Informative)

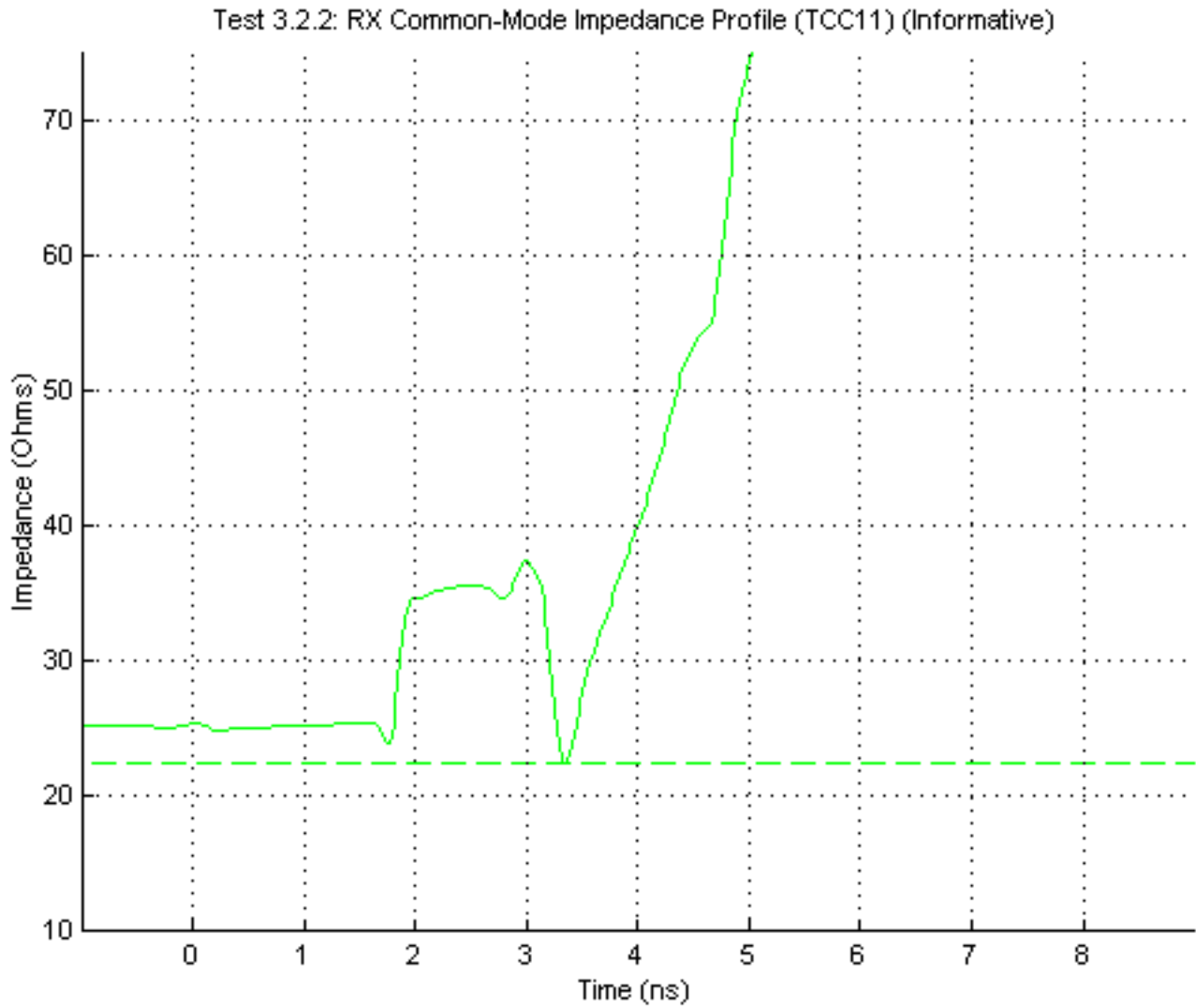




Figure 13: HS-RX Common-Mode Impedance Profile (TCC11) (Data Lane 1) (Informative)

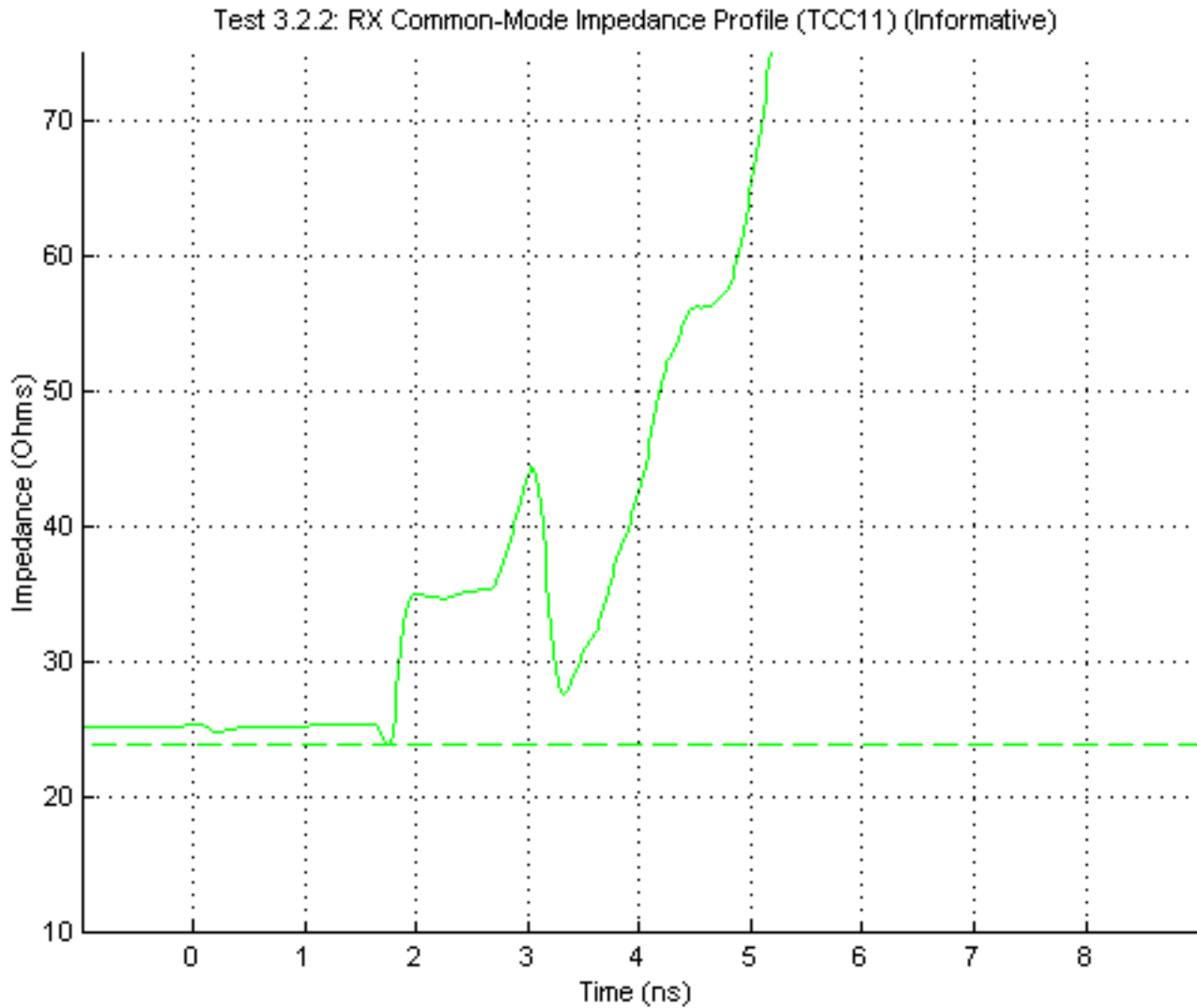


Figure 14: HS-RX Common-Mode Impedance Profile (TCC11) (Data Lane 2) (Informative)

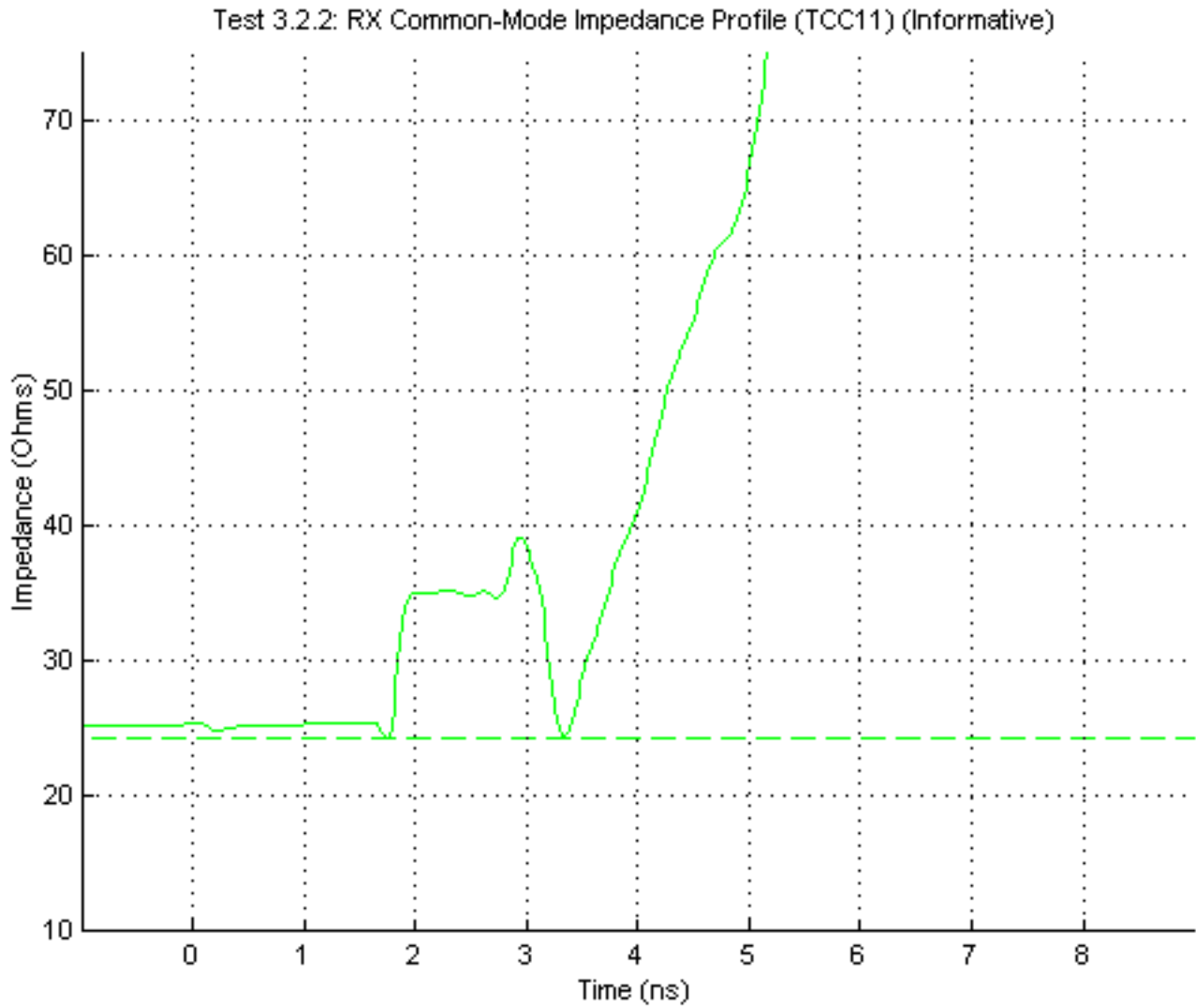


Figure 15: HS-RX Common-Mode Impedance Profile (TCC11) (Data Lane 3) (Informative)

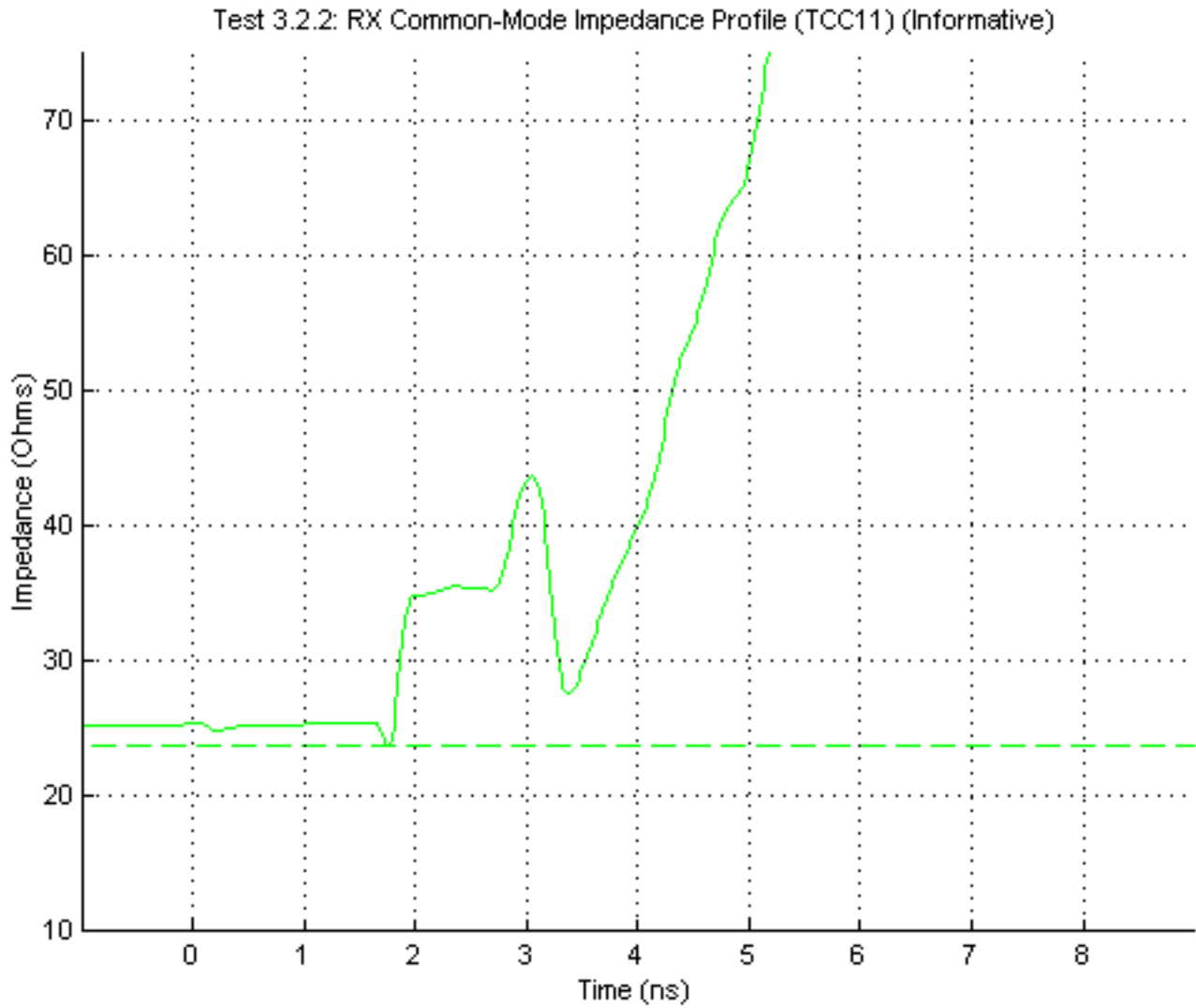


Figure 16: HS-RX Common-Mode Return Loss (SCC11) (Clock Lane)

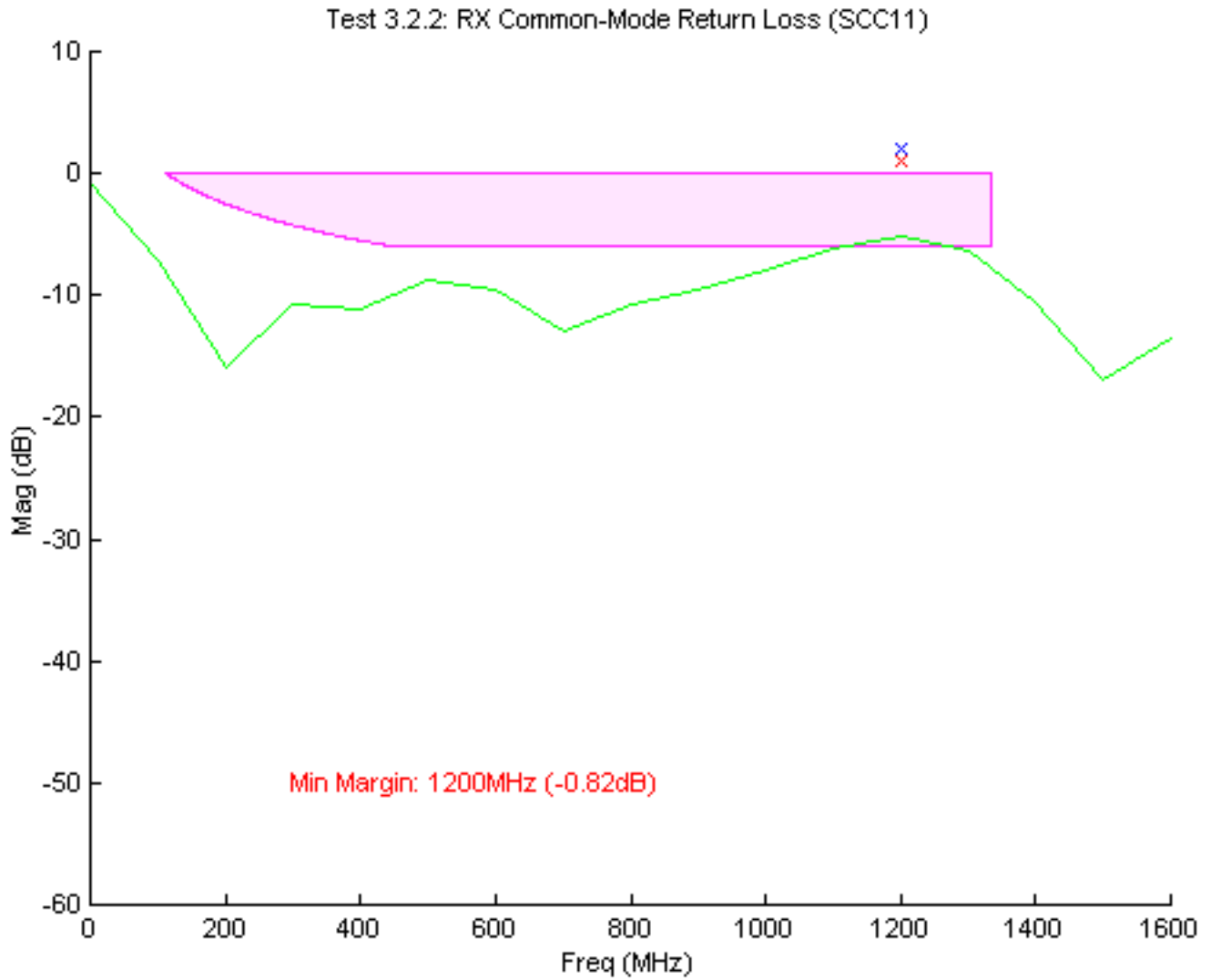


Figure 17: HS-RX Common-Mode Return Loss (SCC11) (Data Lane 0)

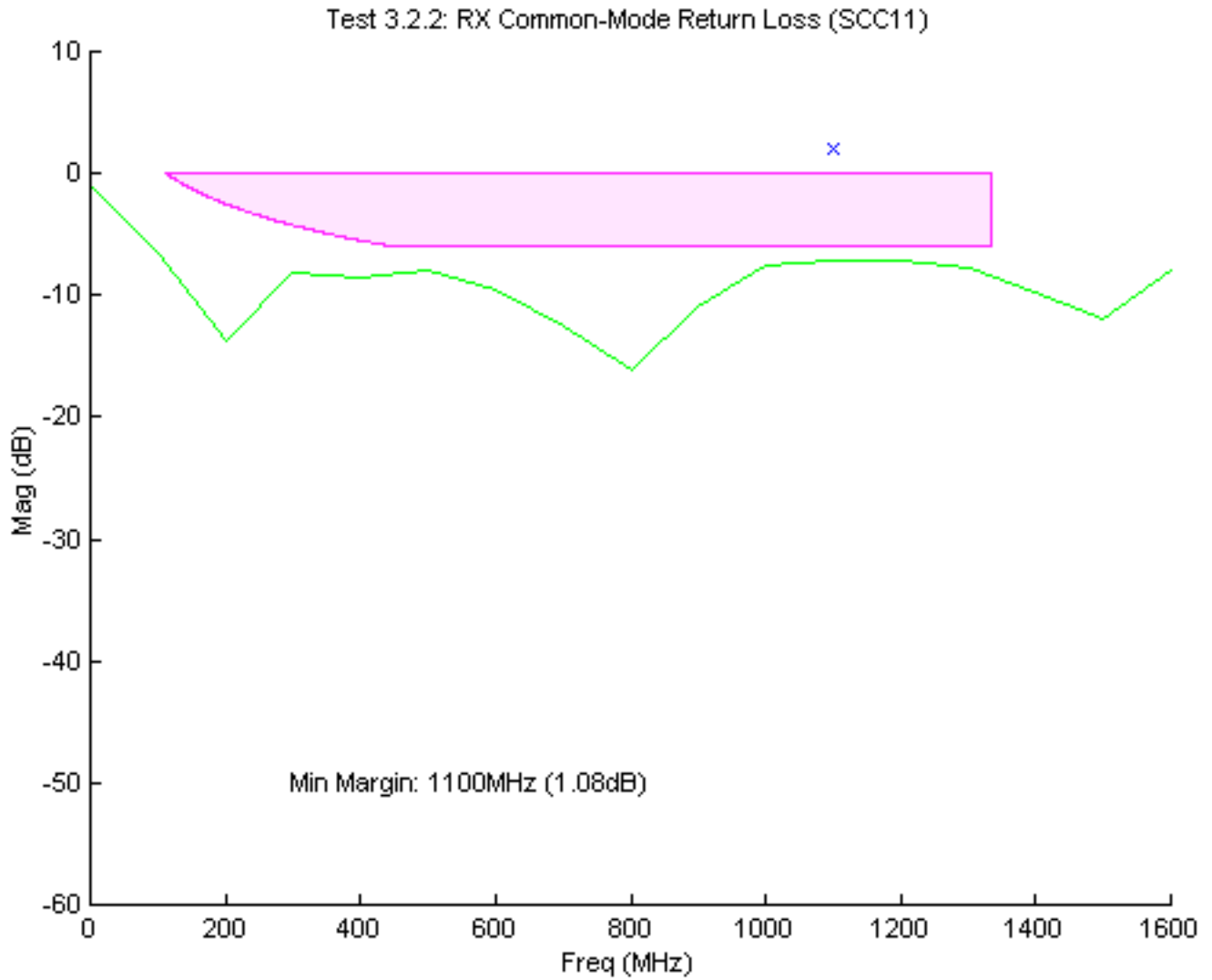


Figure 18: HS-RX Common-Mode Return Loss (SCC11) (Data Lane 1)

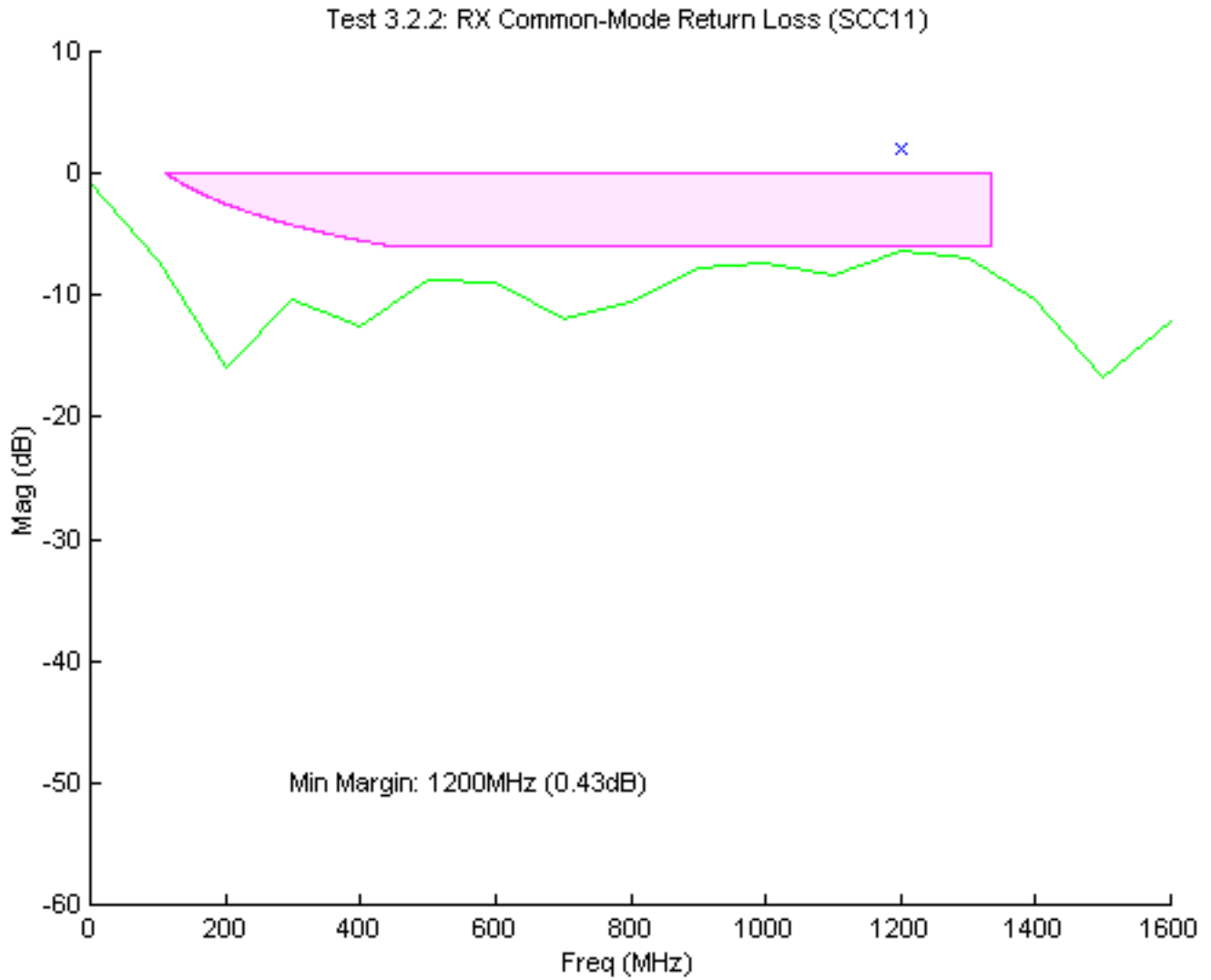


Figure 19: HS-RX Common-Mode Return Loss (SCC11) (Data Lane 2)

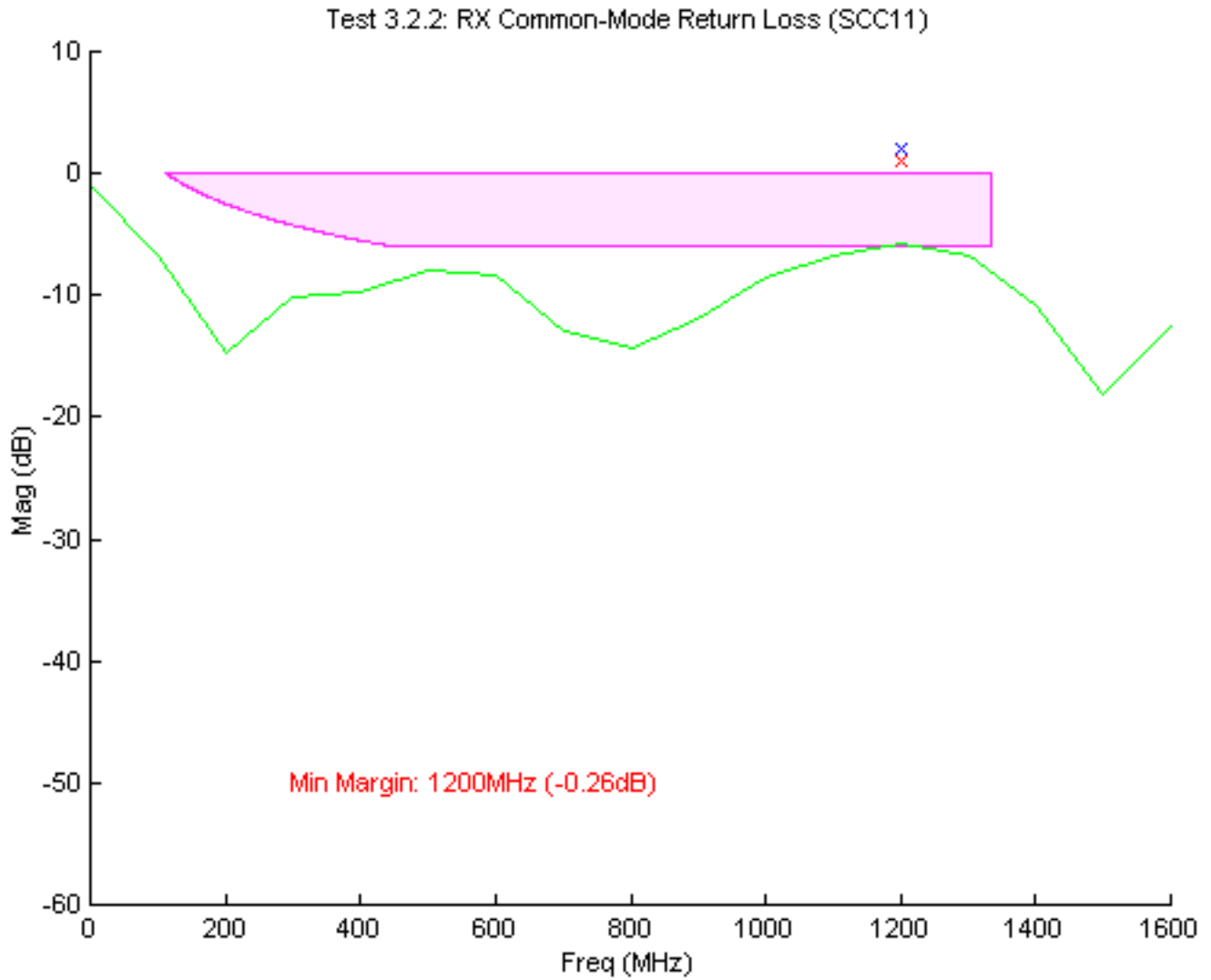


Figure 20: HS-RX Common-Mode Return Loss (SCC11) (Data Lane 3)

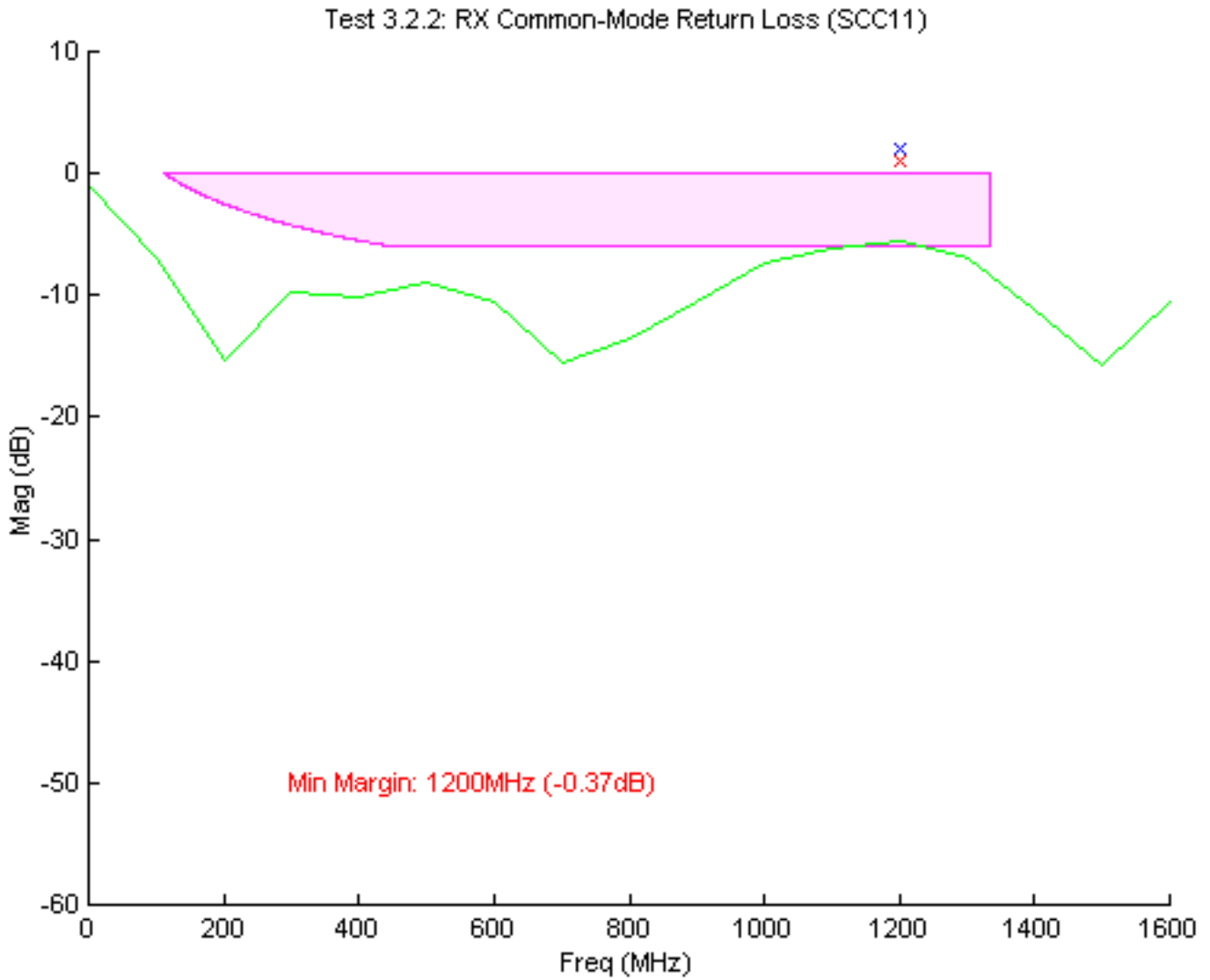




Figure 21: HS-RX Single-Ended Impedance Profiles (Clock Lane) (Informative)

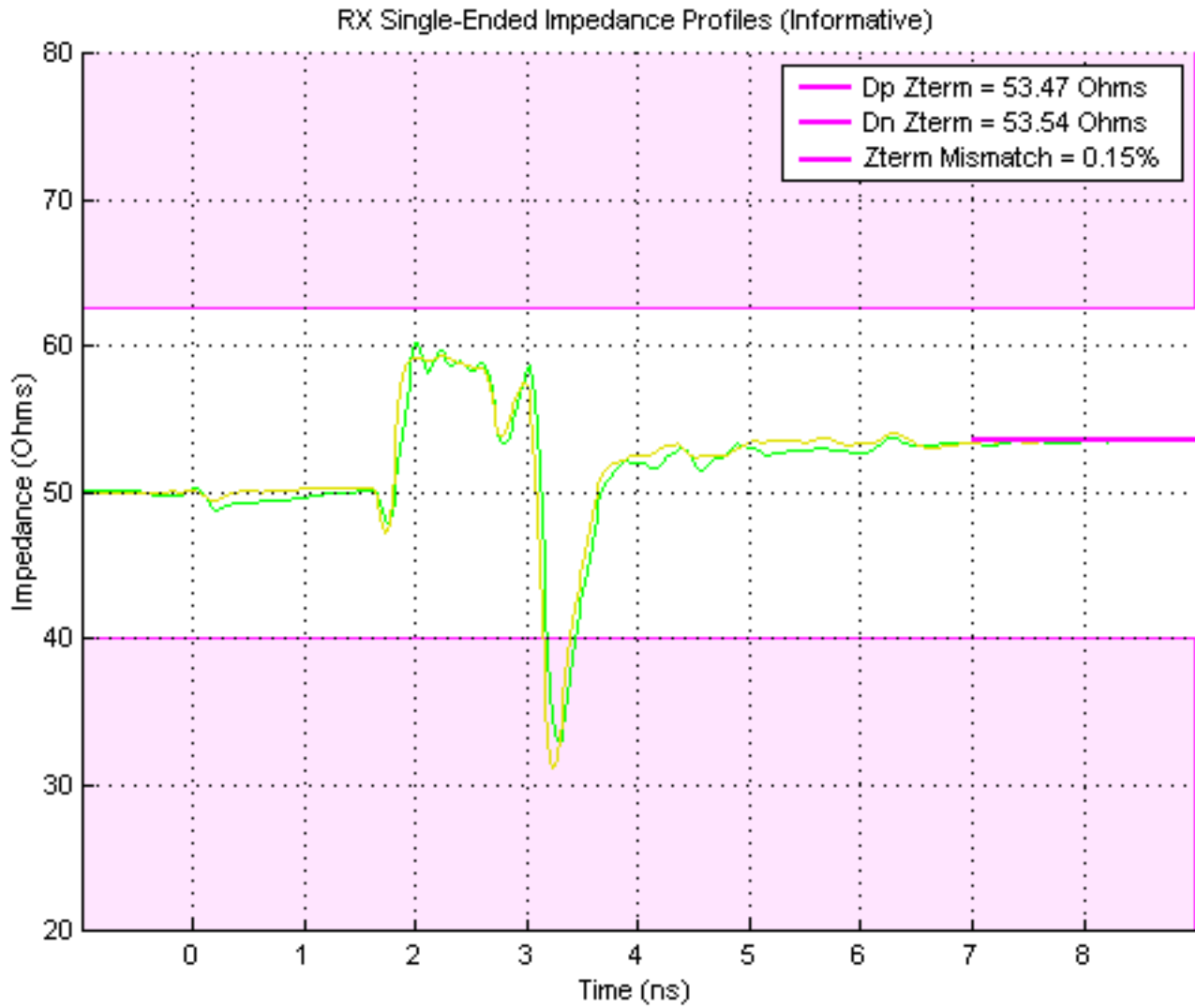


Figure 22: HS-RX Single-Ended Impedance Profiles (Data Lane 0) (Informative)

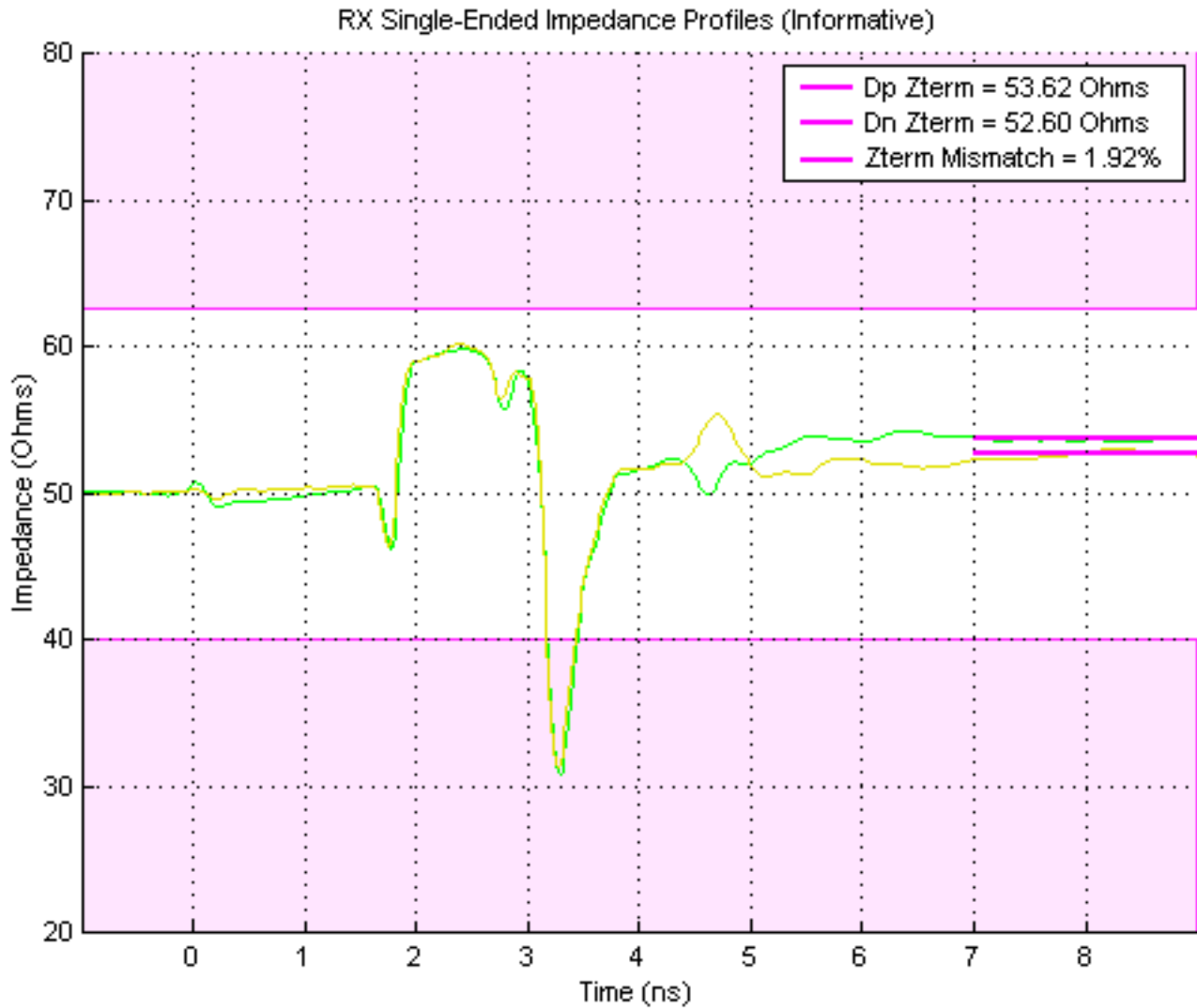


Figure 23: HS-RX Single-Ended Impedance Profiles (Data Lane 1) (Informative)

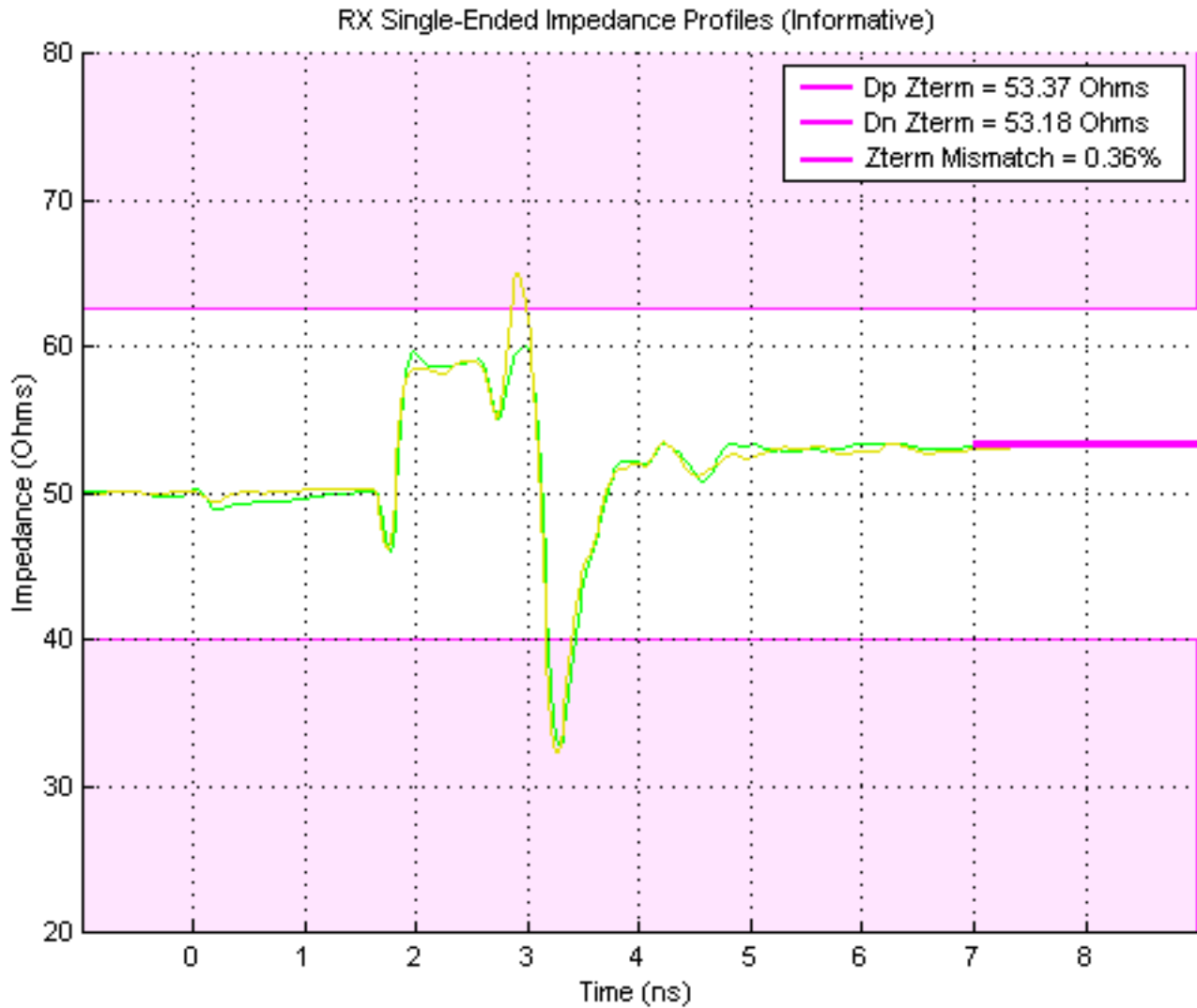


Figure 24: HS-RX Single-Ended Impedance Profiles (Data Lane 2) (Informative)

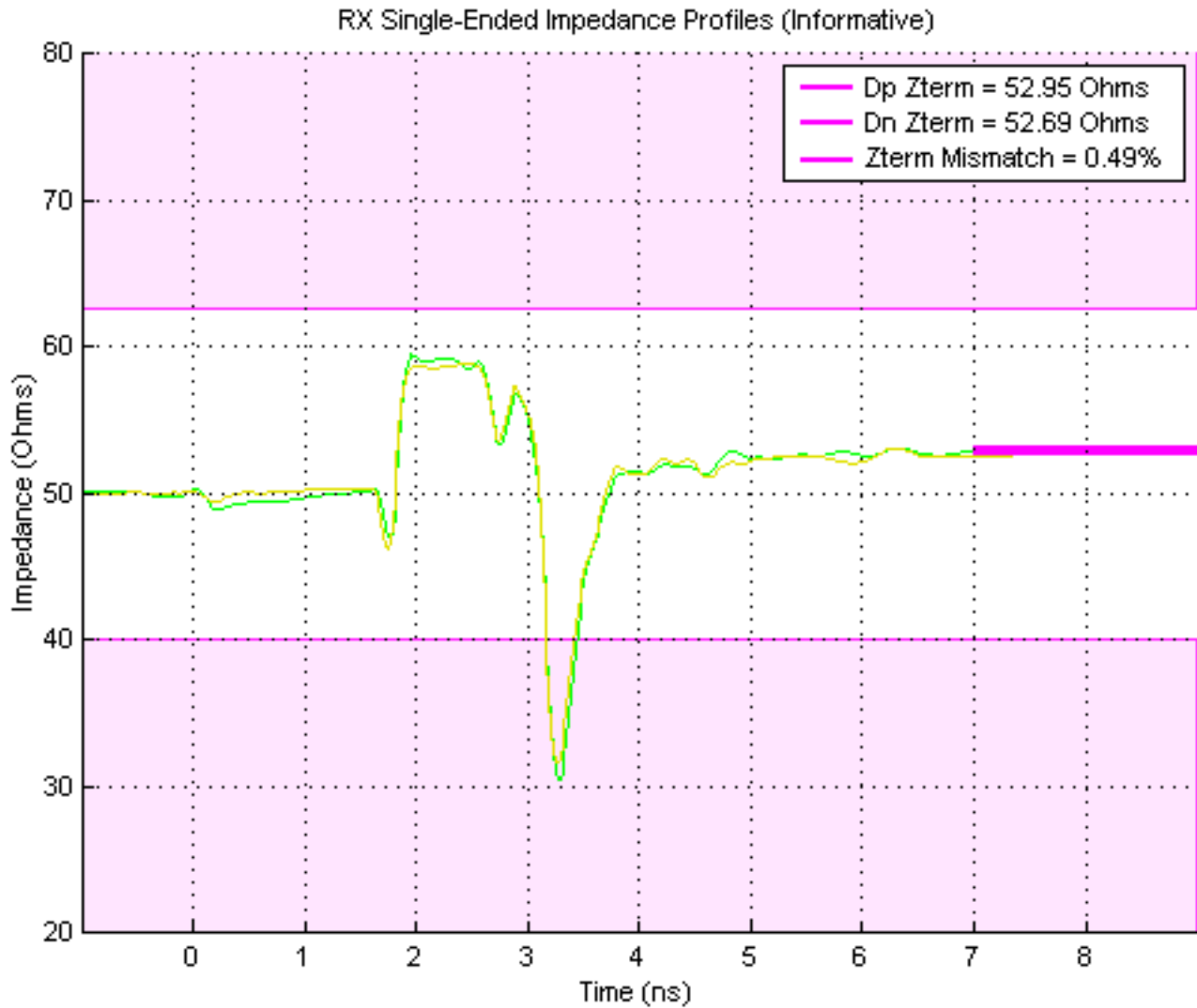


Figure 25: HS-RX Single-Ended Impedance Profiles (Data Lane 3) (Informative)

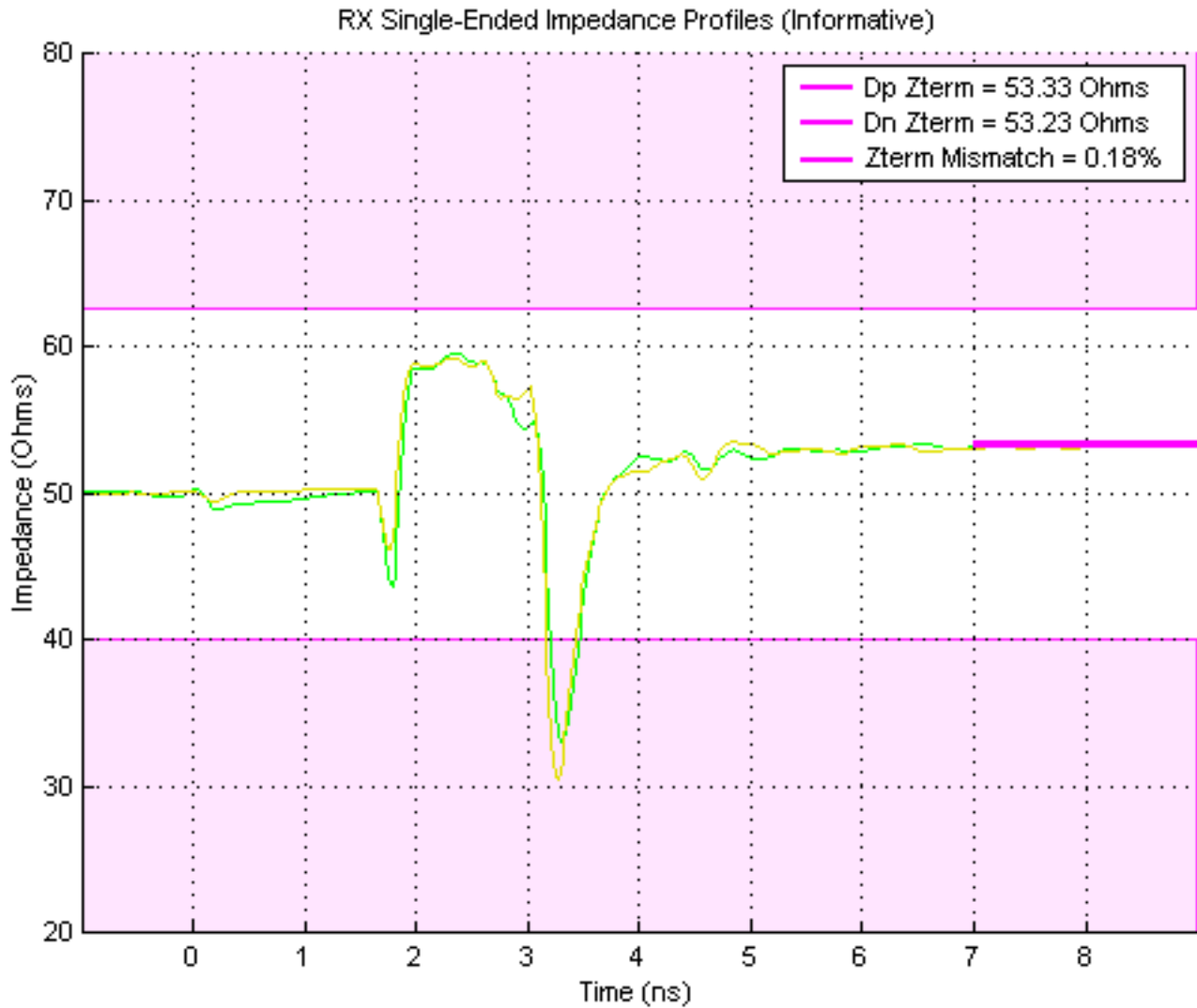


Figure 26: HS-RX Impedance Balance Profile (TDC11) (Clock Lane) (Informative)

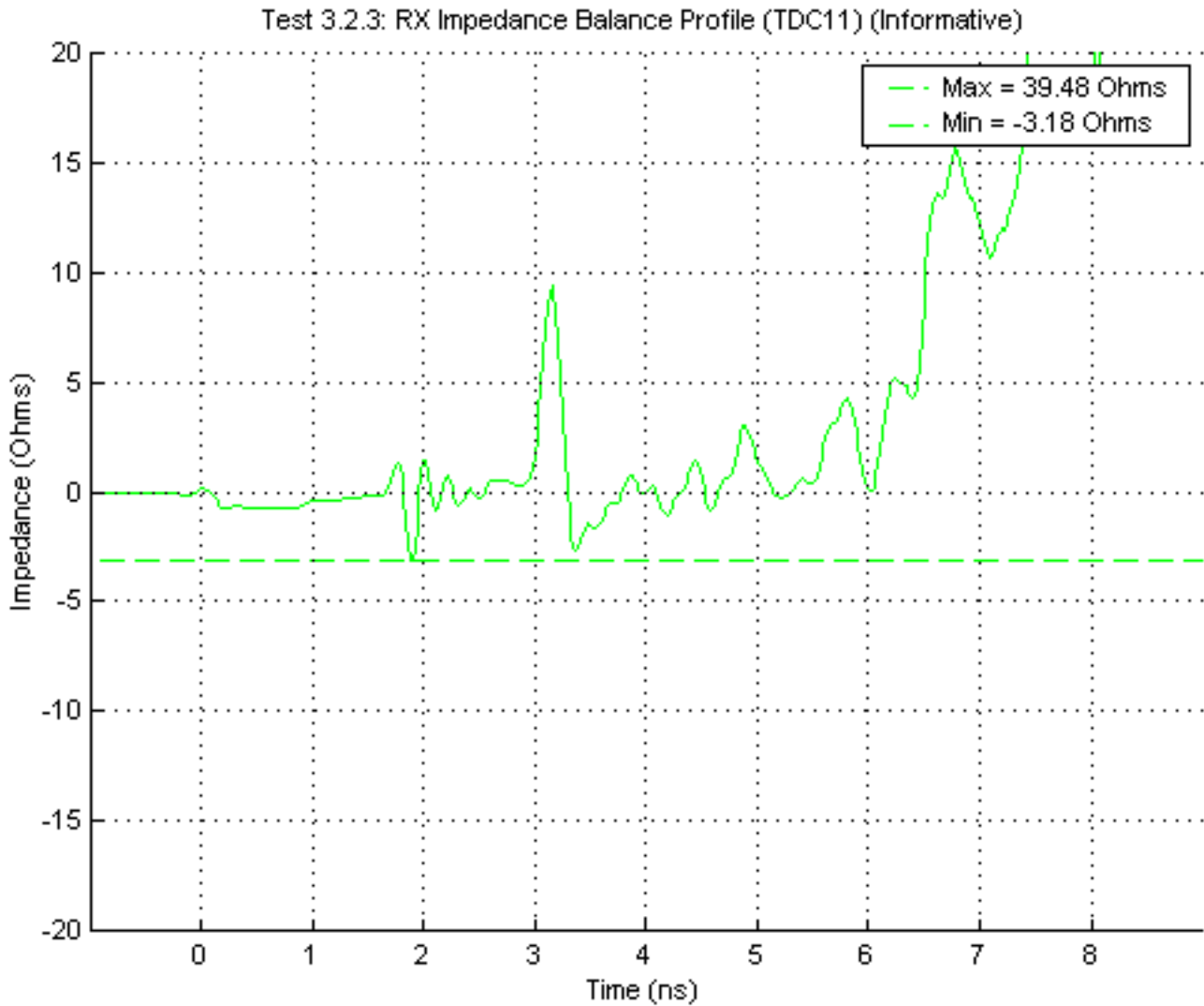


Figure 27: HS-RX Impedance Balance Profile (TDC11) (Data Lane 0) (Informative)

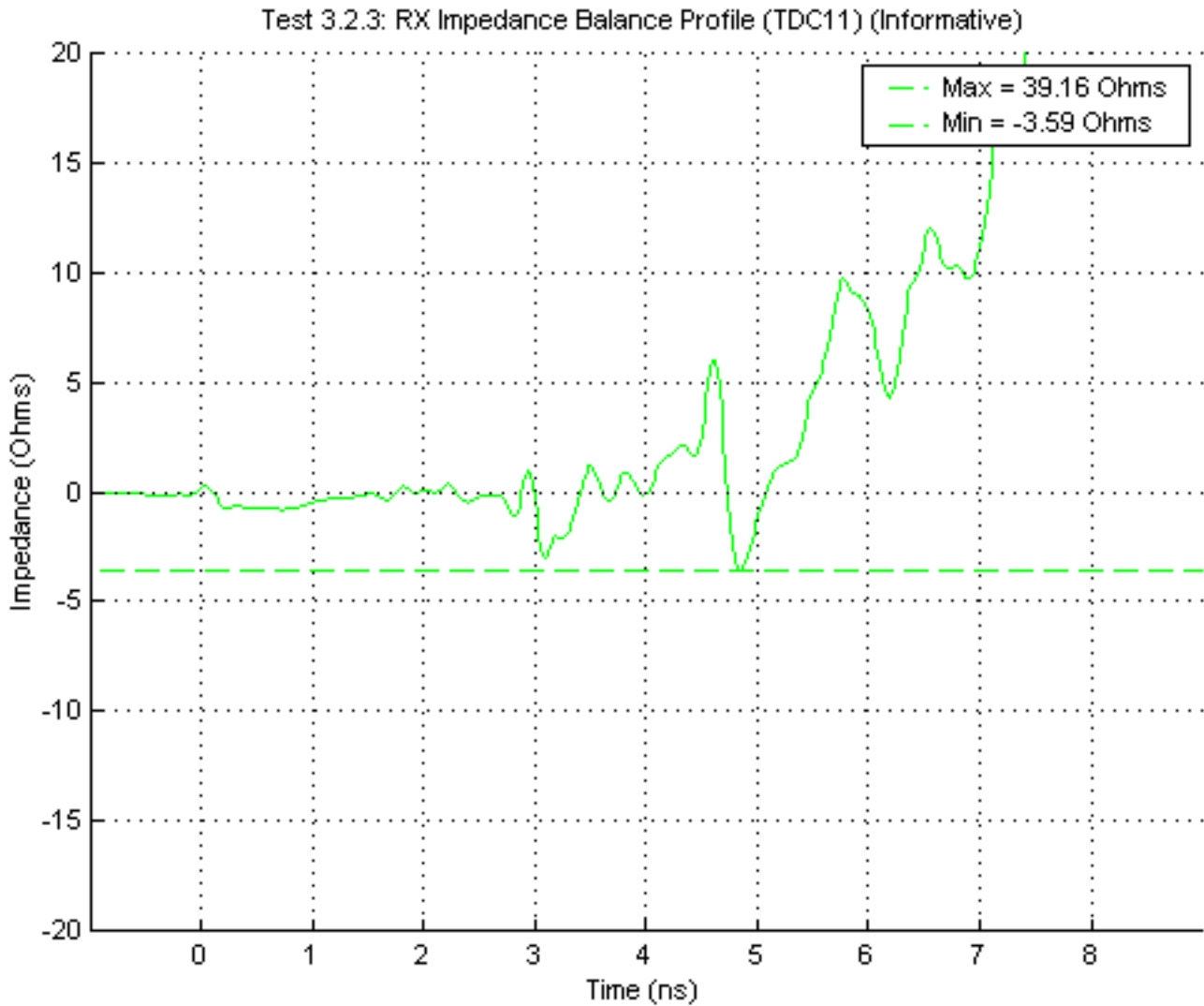


Figure 28: HS-RX Impedance Balance Profile (TDC11) (Data Lane 1) (Informative)

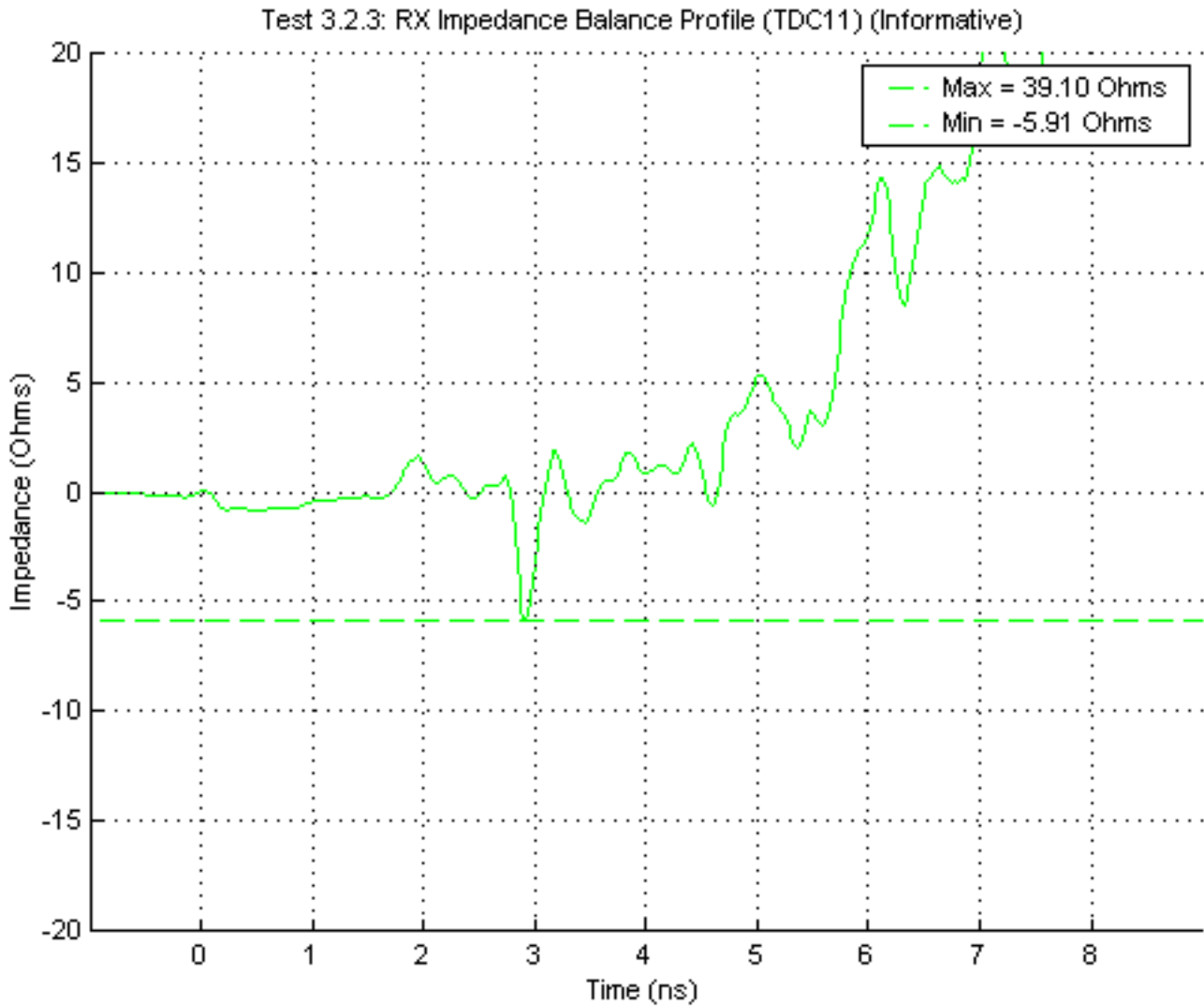




Figure 29: HS-RX Impedance Balance Profile (TDC11) (Data Lane 2) (Informative)

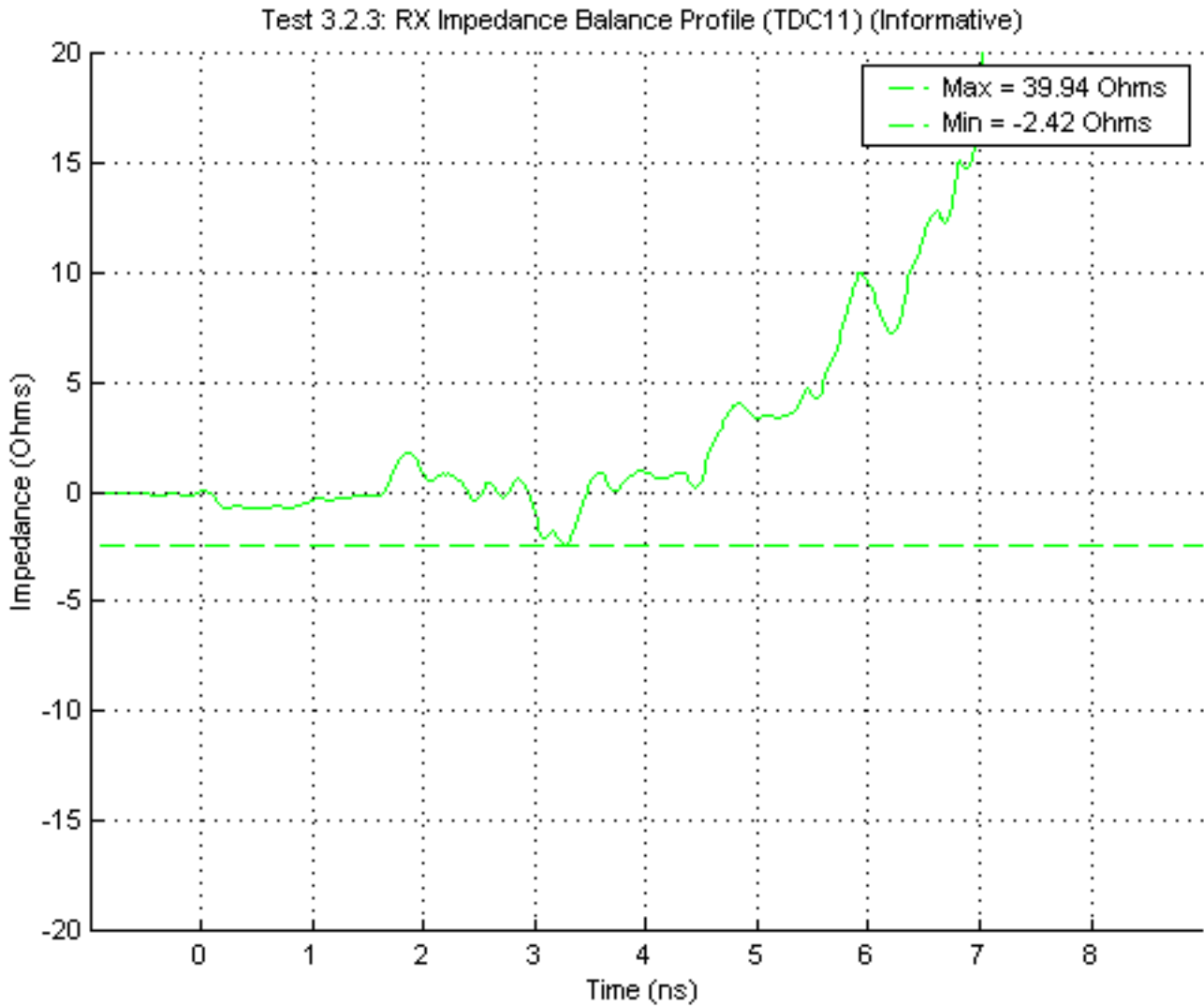


Figure 30: HS-RX Impedance Balance Profile (TDC11) (Data Lane 3) (Informative)



Figure 31: HS-RX Mode Conversion Loss (SDC11) (Clock Lane)

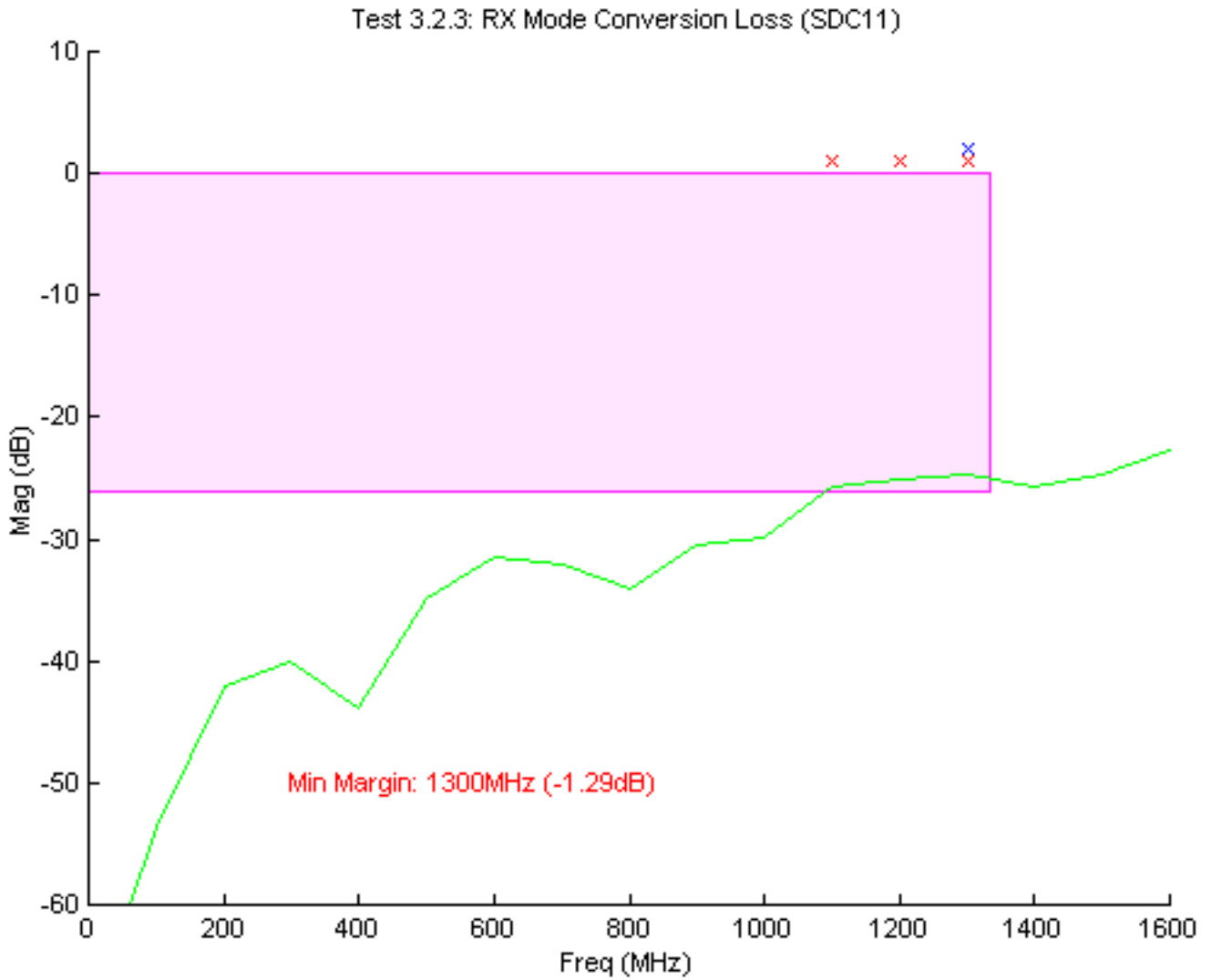


Figure 32: HS-RX Mode Conversion Loss (SDC11) (Data Lane 0)

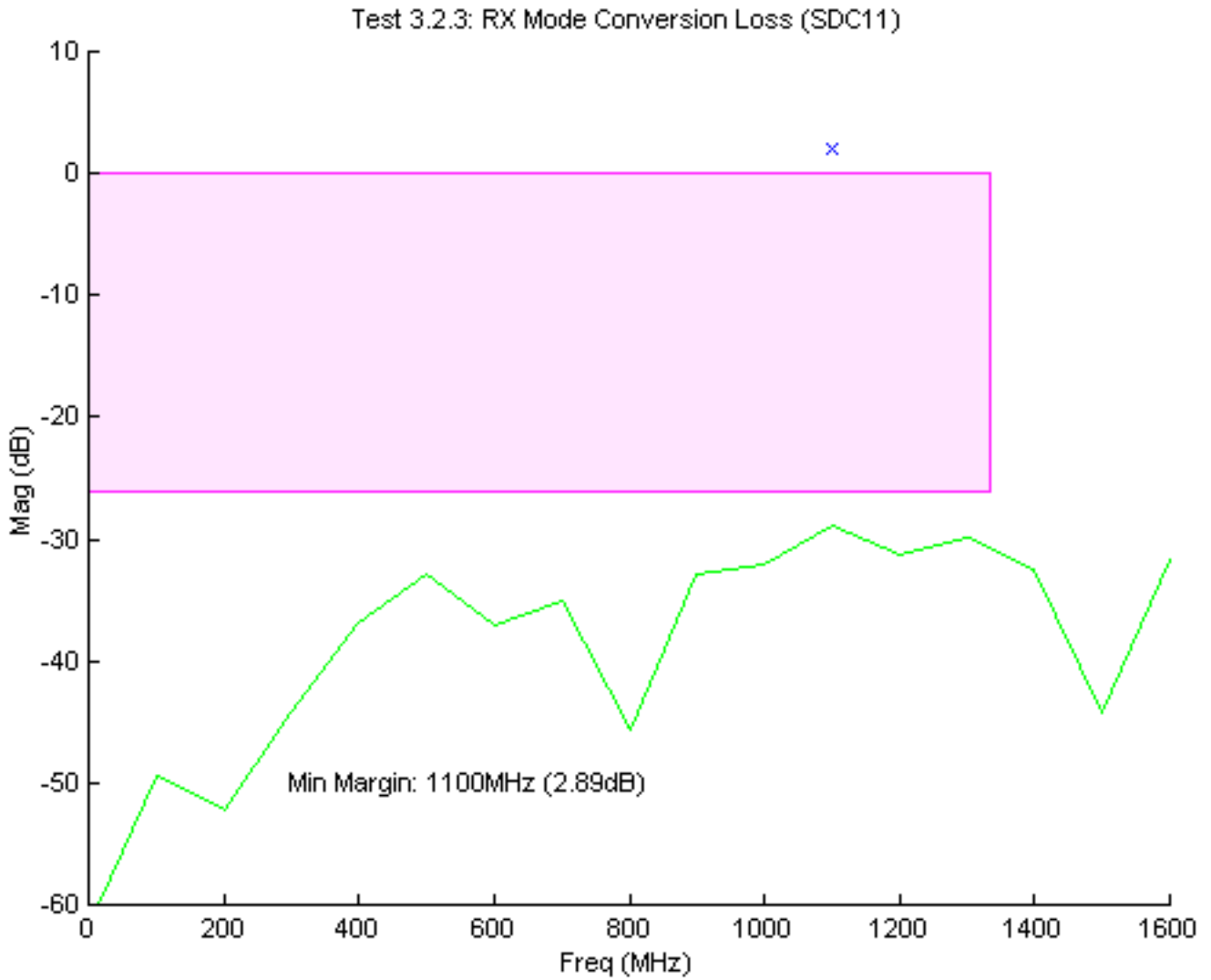


Figure 33: HS-RX Mode Conversion Loss (SDC11) (Data Lane 1)

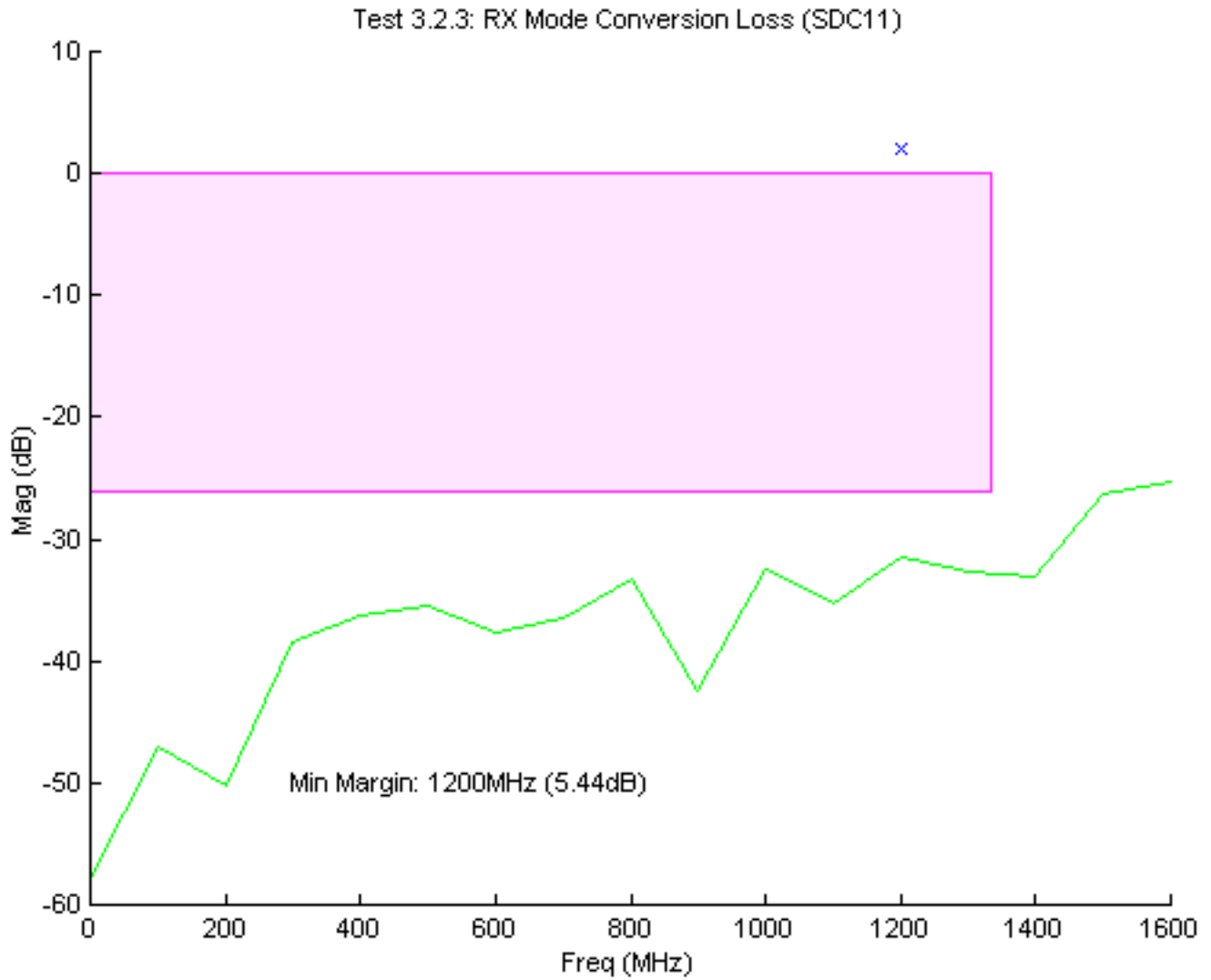


Figure 34: HS-RX Mode Conversion Loss (SDC11) (Data Lane 2)

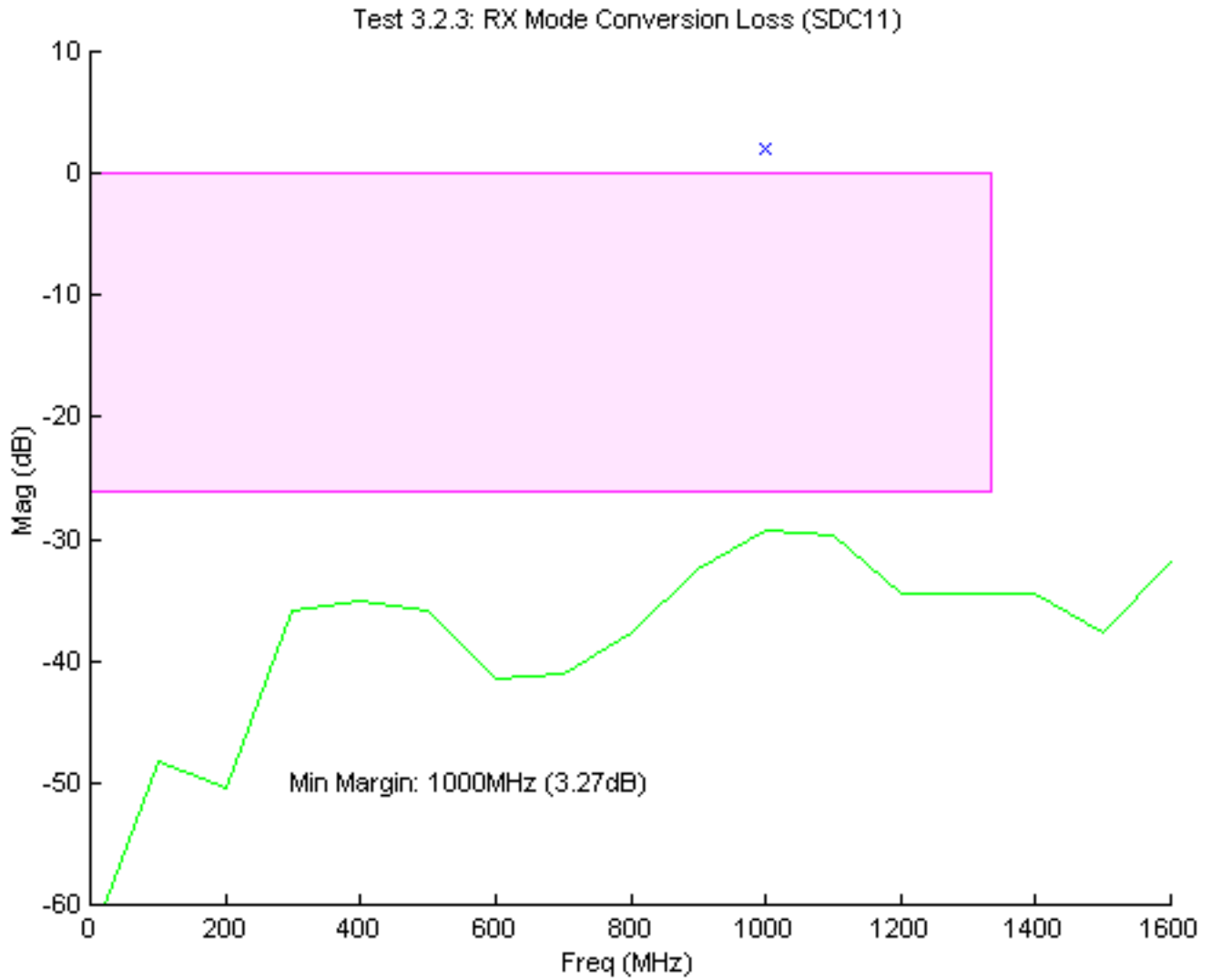


Figure 35: HS-RX Mode Conversion Loss (SDC11) (Data Lane 3)

