Gigabit Ethernet Consortium
Clause 40 PMA Conformance Test Suite v2.5 Report

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Report Rev. 1.0

Enclosed are the results from the Clause 40 Conformance testing performed on:

Device Under Test (DUT):	Company Com DUT
Hardware Version:	HW v2.3A
Firmware Version:	Not Available
Software Version:	SW v1.4.46
Miscellaneous:	Port 0
IOL ID:	GE-CCOM-0000000001

The test suite referenced in this report is available at the UNH-IOL website:

ftp://ftp.iol.unh.edu/pub/ethernet/test_suites/CL40_PMA/PMA_Test_Suite_v2.5.pdf

Issues Observed While Testing
Access to the TX_TCLK was not available during the testing; therefore not all tests could be completed.
40.1.1 – Peak Differential Output Voltage and Level Accuracy – The DUT was observed to have point A/B amplitude less than 670 mV on pair B.
40.1.8 – Common-mode Output Voltage – The DUT was observed to have a common mode voltage greater than 50 mV on pair D.
40.2.1 – Bit Error Ratio Verification – The DUT was observed to receive more than 7 packets in error at 100% attenuation for both risetimes.

Testing Completed: 07/08/2008

Review Completed: 07/08/2008

Digitally signed by UNH-IOL
Date: 2008.07.08 15:22:39 -04'00'

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SHA-1 Fingerprint: 8BBA 64F2 AFC5 54E9 A875 AF4E C623 DCE9 EC9C EB74

Table 1 – Hardware Information

1000BASE-T PHY	
Manufacturer	PhyMaker
Model	Phy2000
Version	Not Available
Magnetics	
Manufacturer	MagMaker
Model	MAG2000
Version	Not Available
Test System Hardware	
Real-time DSO	TEKTRONIX,CSA7404,Q13,CF:91.1CT FV:2.5.3
Vector Network Analyzer	"HEWLETT-PACKARD,8712B,US34400165,B.03.02"
Arbitrary Waveform Genearator	SONY/TEK,AWG2041,0,CF:91.1CT FV:1.27
Test System Software	UNH-IOL PMA Test System v3.3

Test Setup

All tests in this report were performed using the test setup specified in the 1000BASE-T PMA Test Suite in the Test Setup section of each test.

GROUP 1 – PMA Electrical Specifications

Table 2 – Test Requirements

Test	Title	Min	Max	Units
40.1.1 – Peak Differential Output Voltage and Level Accuracy				
A	Magnitude of point A	670	820	mV
B	Magnitude of point B	670	820	mV
C	Difference between the magnitudes of points A and B	0	1	%
D	Difference between the magnitude of point C and 0.5 times the average of the magnitudes of points A and B	0	2	%
E	Difference between the magnitude of point D and 0.5 times the average of the magnitudes of points A and B	0	2	%
40.1.2 – Maximum Output Droop				
A	Ratio of the voltage at point G to the voltage at point F	73.1	100	%
B	Ratio of the voltage at point J to the voltage at point H	73.1	100	%
40.1.3 – Differential Output Templates				
A-D	The waveforms around points A, B, C, and D, after normalization, shall lie within time domain template 1.			
E-F	The waveforms around points F and H, after normalization, shall lie within time domain template 2.			
40.1.4 – MDI Return Loss				
A	The return loss of the MDI shall be at least 16 dB from 1 to 40 MHz and at least 10–20 $\log_{10}$(f /80 MHz) dB from 40 to 100 MHz for all differential signals incident upon the MDI from an 85 or 115 Ω source.			
40.1.5 – Transmitter Timing Jitter				
A	The Test Mode 2 Jtxout value is informative			
B	The Test Mode 3 Jtxout value is informative			
C	The peak-to-peak jitter on the MASTER TX_TCLK relative to an unjittered reference	0	1.4	ns
D	The peak-to-peak jitter on the MASTER TX_TCLK when passed through a 5kHz high-pass filter	0	0.3 – (Max Test Mode 2 J_{txout})	ns
E	The peak-to-peak jitter on the SLAVE TX_TCLK relative to a Link Partner's MASTER TX_TCLK	0	1.4	ns
F	The peak-to-peak jitter on the SLAVE TX_TCLK relative to a Link Partner's MASTER TX_TCLK, when passed through a 32kHz high-pass-filter plus Max Test Mode 3 Jtxout	0	0.4 + (Link Partner 5k HPF jitter) – (Max Test Mode 3 J_{txout})	ns
G	The peak-to-peak jitter on the Link Partner's MASTER TX_TCLK, when passed through a 5kHz high-pass-filter	0	0.3	ns
40.1.6 – Transmitter Distortion				
A	The maximum peak transmitter distortion within 60% UI	0	10	mV
B	The percent of UI under 10mV distortion limit	60	100	%
40.1.7 – Transmit Clock Frequency				
A	Frequency minus 125 MHz	-12.5	+12.5	kHz
40.1.8 – Common-mode Output Voltage				
A	Peak-to-peak Common-mode Output Voltage	0	50	mV

Table 3 – Summary of results

Test	Parameter	Min	Max	BI_DA	BI_DB	BI_DC	BI_DD	Units	Figure
40.1.1 – Peak Differential Output Voltage and Level Accuracy									
A	Point A amplitude	670	820	710	662	707	706	mV	
B	Point B amplitude	670	820	709	662	710	705	mV	
C	Point A/B symmetry	0	1	0.141	0.000	0.424	0.142	%	
D	Point C symmetry	0	2	1.127	0.578	0.565	0.567	%	
E	Point D symmetry	0	2	0.845	0.578	1.130	0.567	%	
40.1.2 – Maximum Output Droop									
A	Droop from F to G	73.1	100	95.50	95.19	95.14	95.18	%	
B	Droop from H to J	73.1	100	96.04	95.58	95.77	95.66	%	
40.1.3 – Differential Output Templates									
A	Point A waveform			Pass	Pass	Pass	Pass		1
B	Point B waveform			Pass	Pass	Pass	Pass		2
C	Point C waveform			Pass	Pass	Pass	Pass		3
D	Point D waveform			Pass	Pass	Pass	Pass		4
E	Point F waveform			Pass	Pass	Pass	Pass		5
F	Point H waveform			Pass	Pass	Pass	Pass		6
40.1.4 – MDI Return Loss									
A	Return Loss margin	0	Inf	2.727	2.553	1.066	3.160	dB	7
40.1.5 – Transmitter Timing Jitter									
A	Jtxout, Test Mode 2	Informative		0.163	0.145	0.160	0.174	ns	8
B	Jtxout, Test Mode 3	Informative		0.155	0.145	0.164	0.169	ns	9
C	Master unfilt. pk-pk	0	1.4				0.139	ns	10
D	Master filt. pk-pk	0	0.3 - J_{txout}				0.119	ns	
	Master filt. plus J_{txout}	0	0.3				0.293	ns	
E	Slave unfilt. pk-pk	0	1.4				0.409	ns	11, 12
F	Slave filt. pk-pk	0	0.4 + (part G) - J_{txout}				0.123	ns	
	Slave filt. plus J_{txout}	0	0.4 + (part G)				0.292	ns	
G	LP Master filt. pk-pk	0	0.3				0.294	ns	
40.1.6 – Transmitter Distortion									
A	Max Peak Distortion	0	10	6.7	9.0	8.5	7.4	mV	14, 15, 16
B	% of UI under 10mV	60	100	100.0	100.0	85.0	100.0	%	
40.1.7 – Transmit Clock Frequency									
A	Clock deviation	-12.5	+12.5				0.414	kHz	
40.1.8 – Common-mode Output Voltage									
A	Common-mode p-p	0	50	43.257	45.266	44.692	52.862	mV	

GROUP 2 – PMA Receive Tests

Table 4 – Test Requirements and Summary of Results

<table>
<tr><th>Test #</th><th>Parameter</th></tr>
<tr><td colspan="2">40.2.1 – Bit Error Ratio Verification</td></tr>
<tr><td>Requirements</td><td>The receiver shall maintain a bit error rate better than 10^{-10} over test channels representing 10% to 100% (10% increments) of the worst-case cable attenuation. This implies that no more than 7 out of 2,500,000 1518 byte packets may be received in error</td></tr>
<tr><td>Results</td><td>
<table>
<tr><th>Attenuation Level</th><th>Errors, Low Rise Time</th><th>Errors, High Rise Time</th></tr>
<tr><td>10%</td><td>0</td><td>0</td></tr>
<tr><td>20%</td><td>0</td><td>0</td></tr>
<tr><td>30%</td><td>0</td><td>0</td></tr>
<tr><td>40%</td><td>0</td><td>0</td></tr>
<tr><td>50%</td><td>0</td><td>0</td></tr>
<tr><td>60%</td><td>0</td><td>0</td></tr>
<tr><td>70%</td><td>0</td><td>0</td></tr>
<tr><td>80%</td><td>0</td><td>0</td></tr>
<tr><td>90%</td><td>0</td><td>0</td></tr>
<tr><td>100%</td><td>14</td><td>19</td></tr>
</table>
</td></tr>
</table>

Annex A – Supplemental figures

Figure 1: Waveform around point A

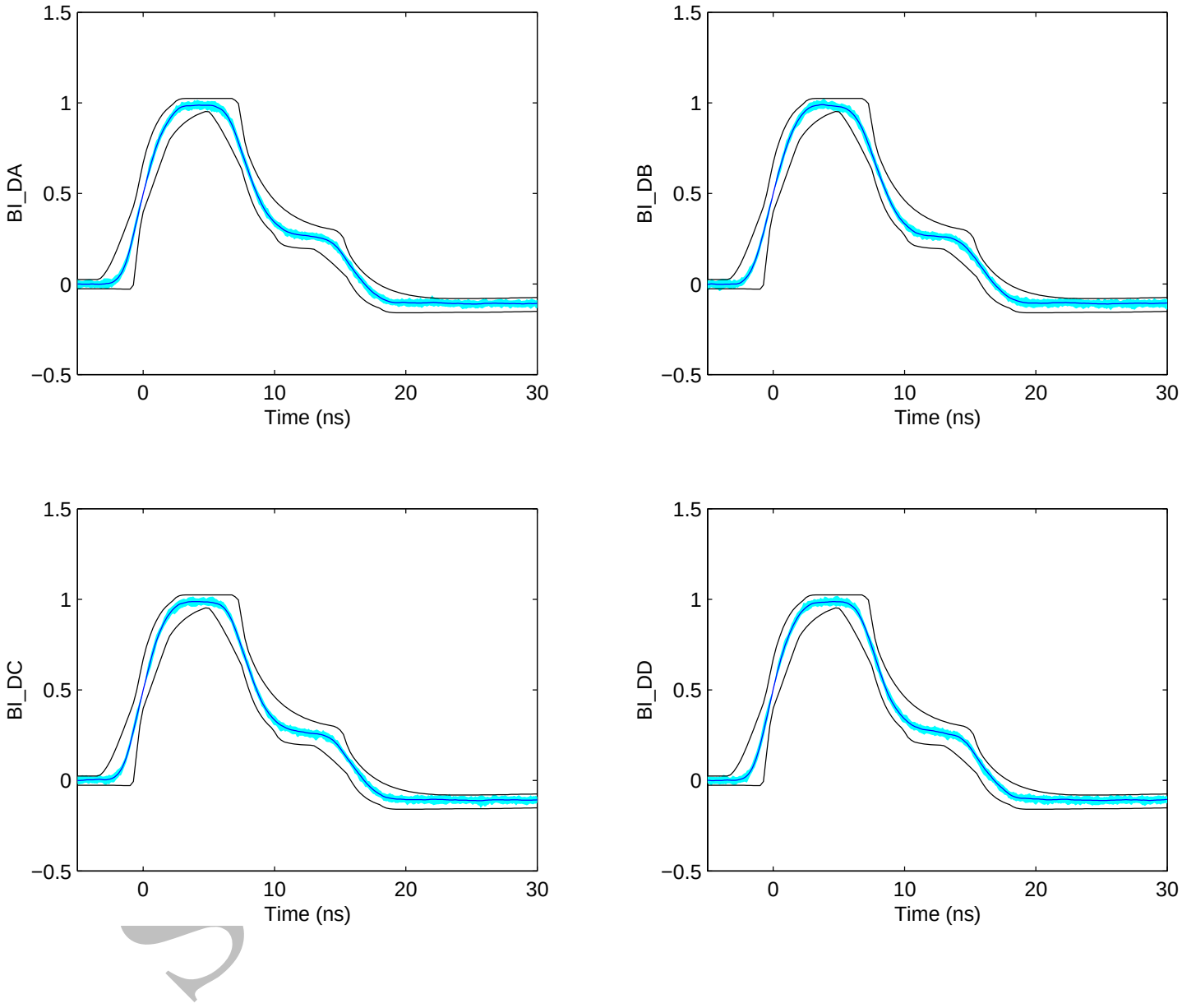


Figure 2: Waveform around point B

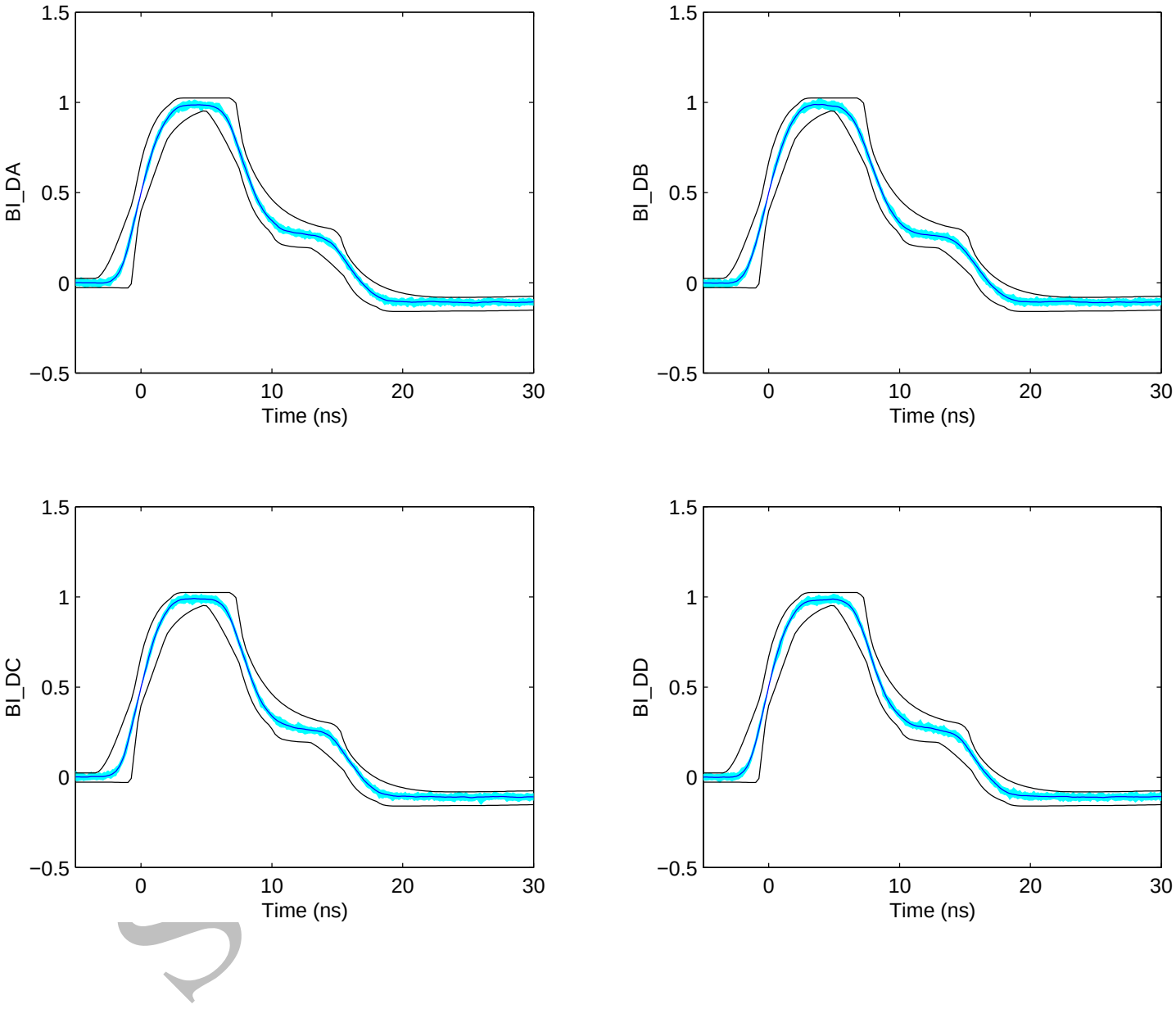


Figure 3: Waveform around point C

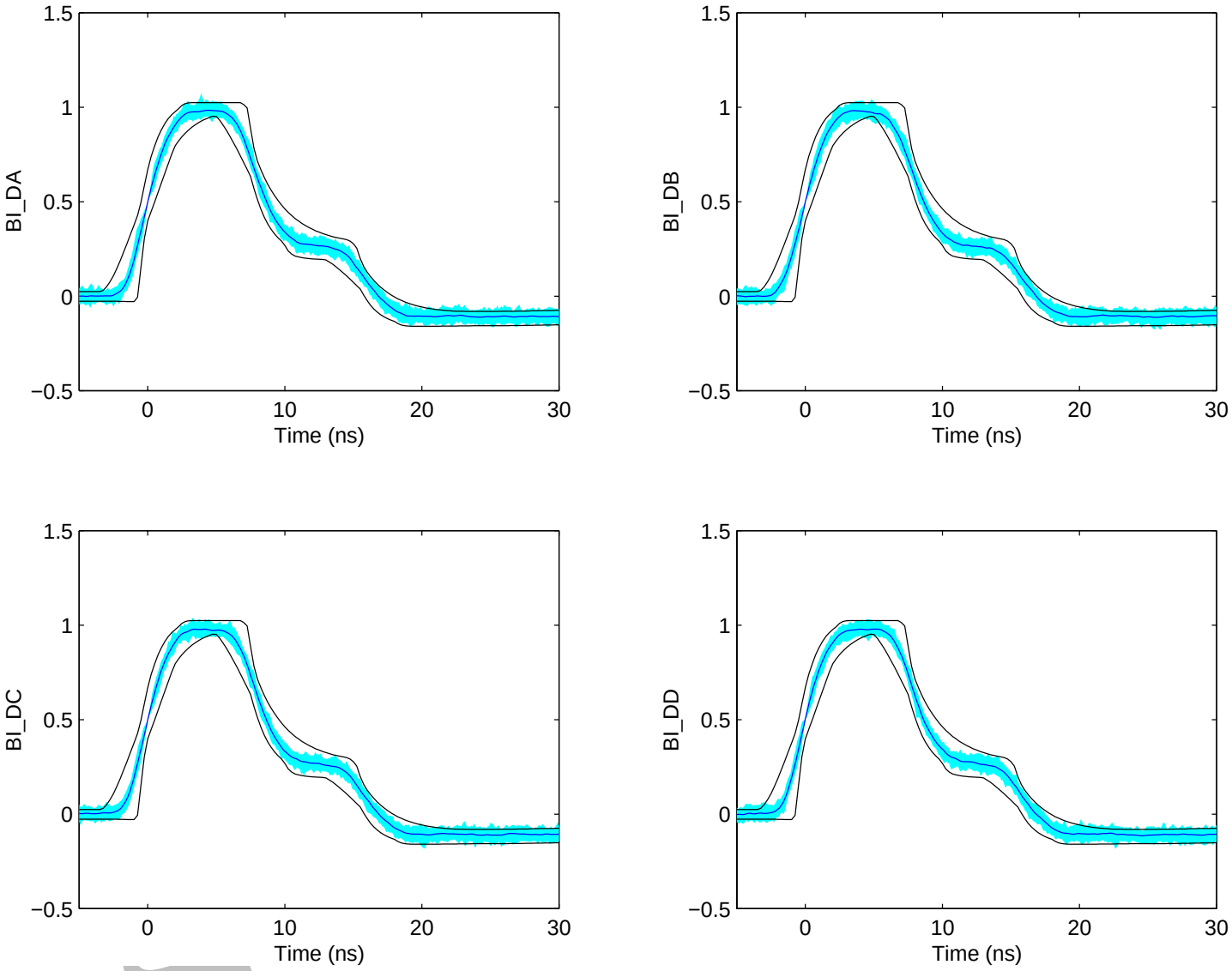


Figure 4: Waveform around point D

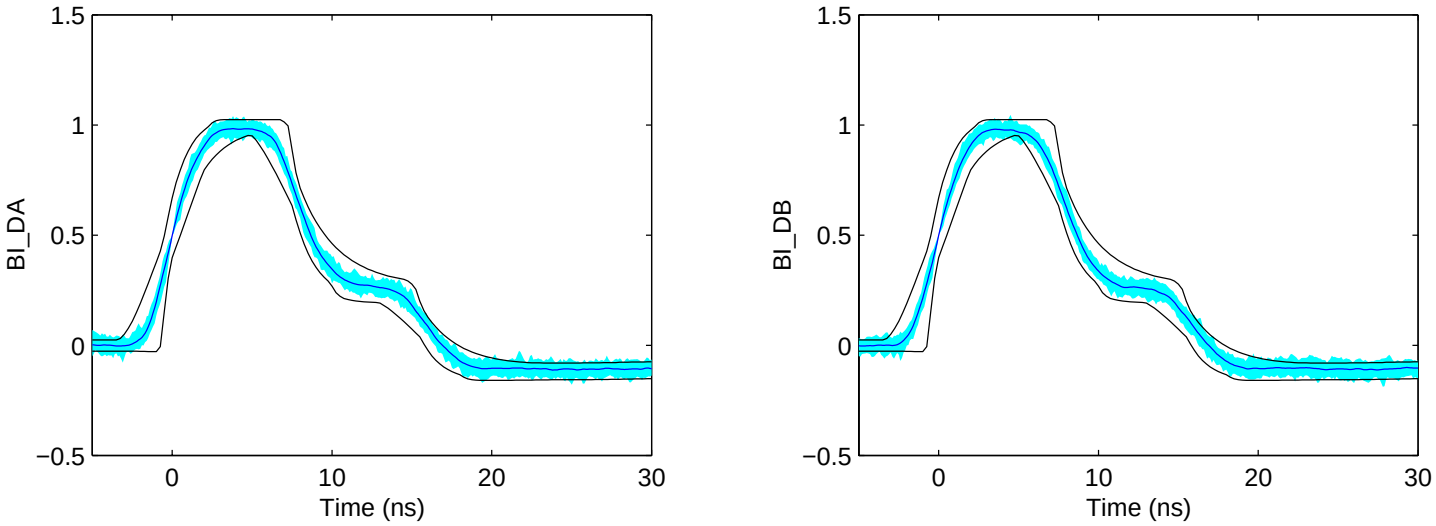


Figure 5: Waveform around point F

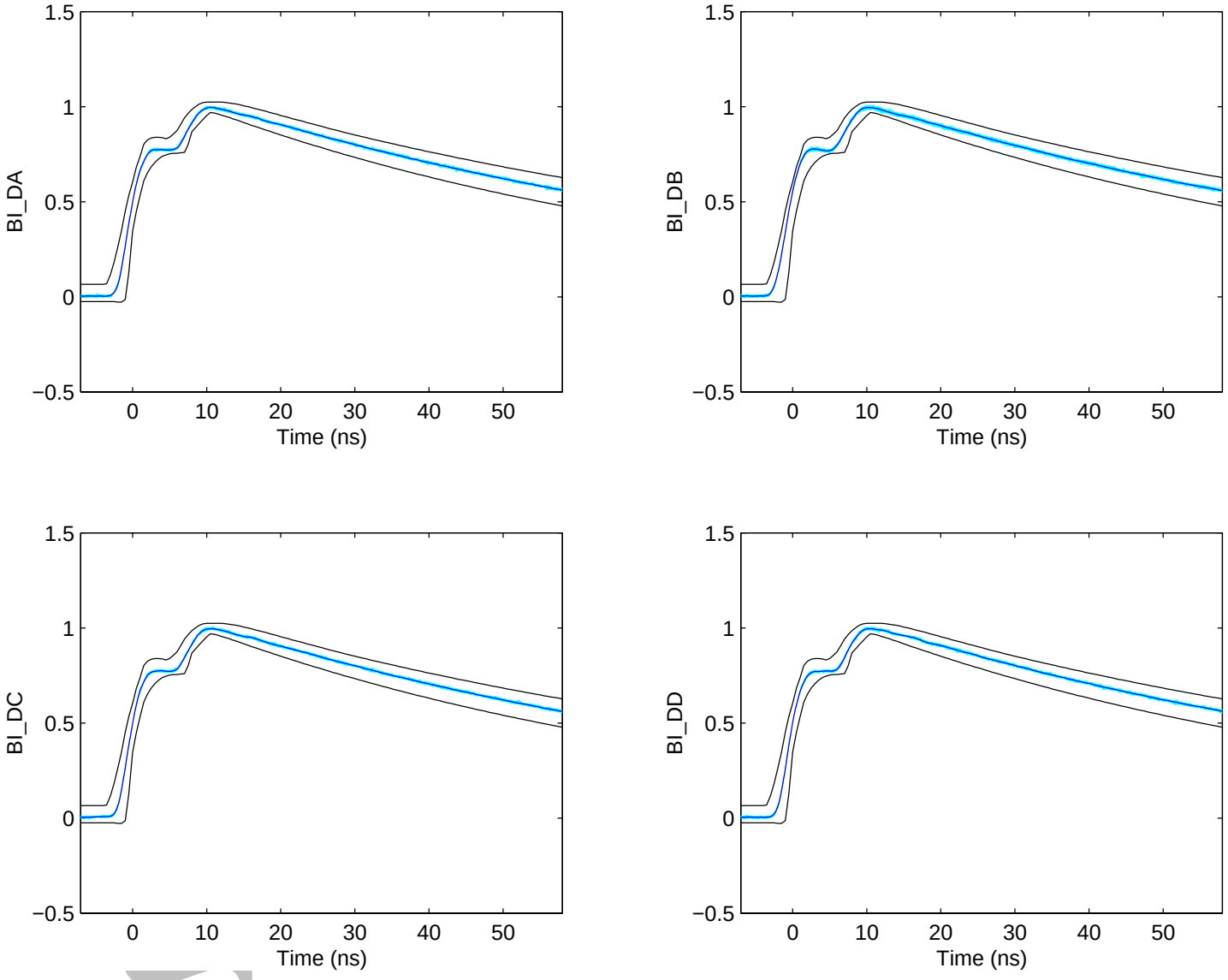


Figure 6: Waveform around point H

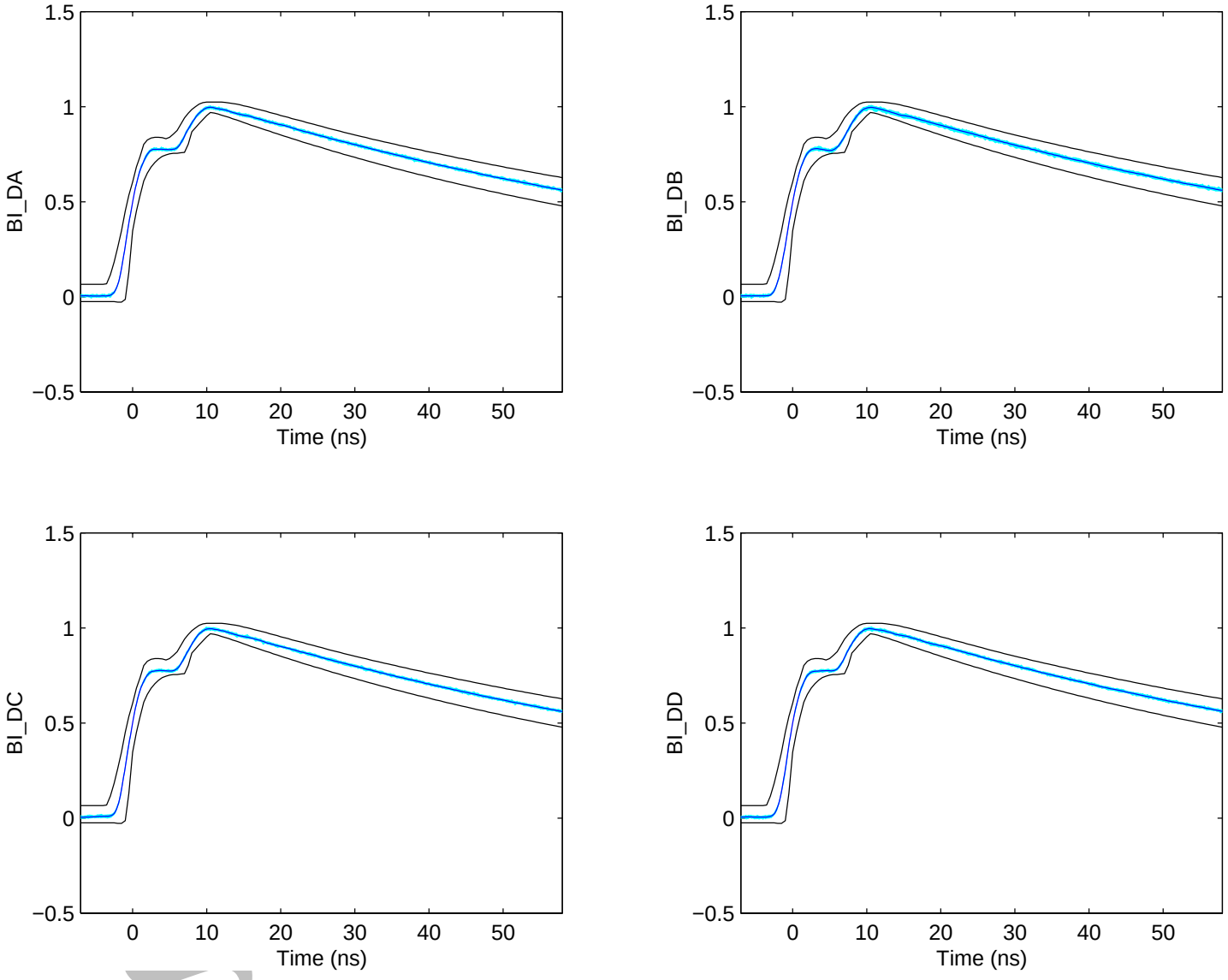


Figure 7: Return loss vs. frequency

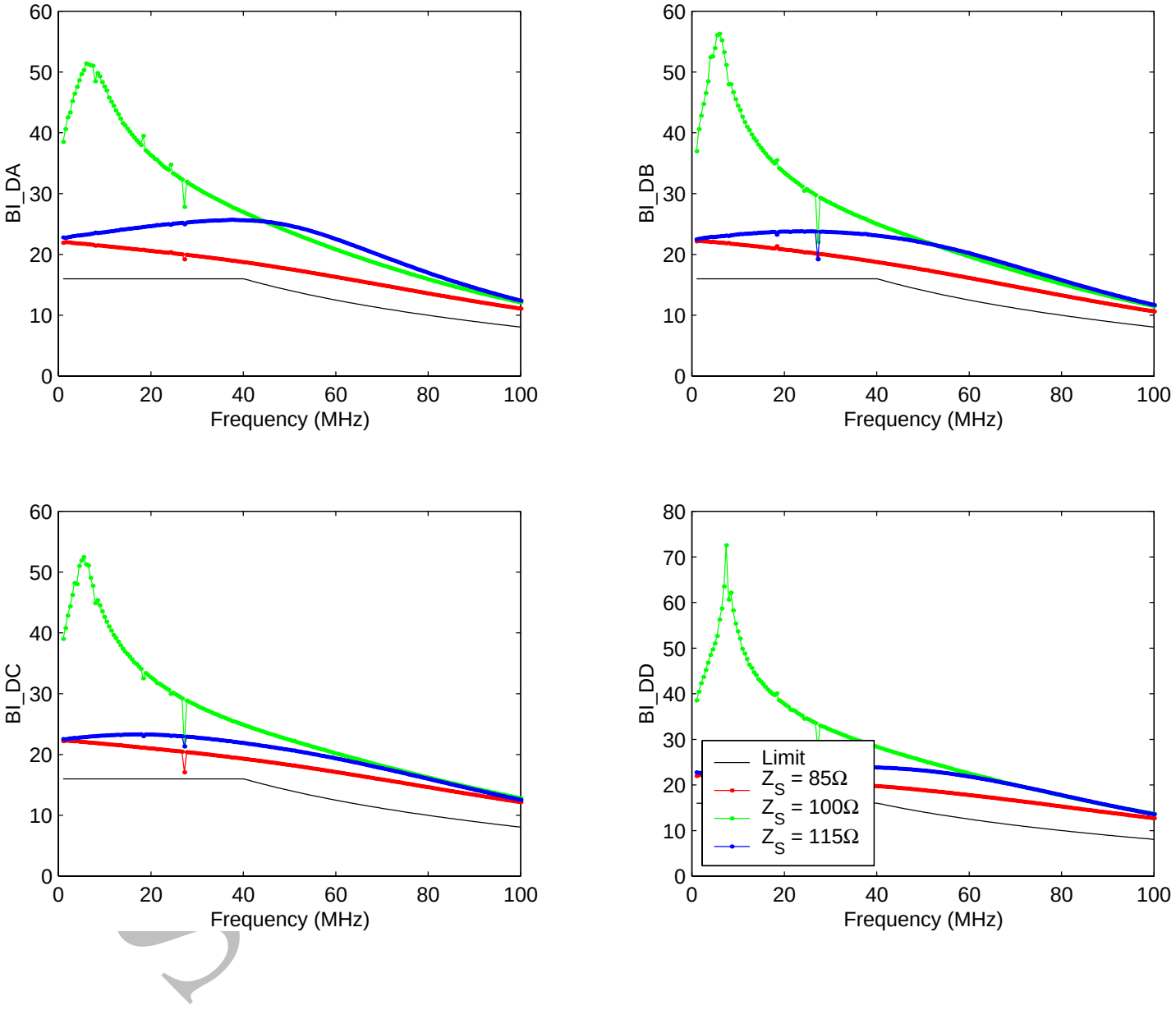


Figure 8: JTXM Histogram

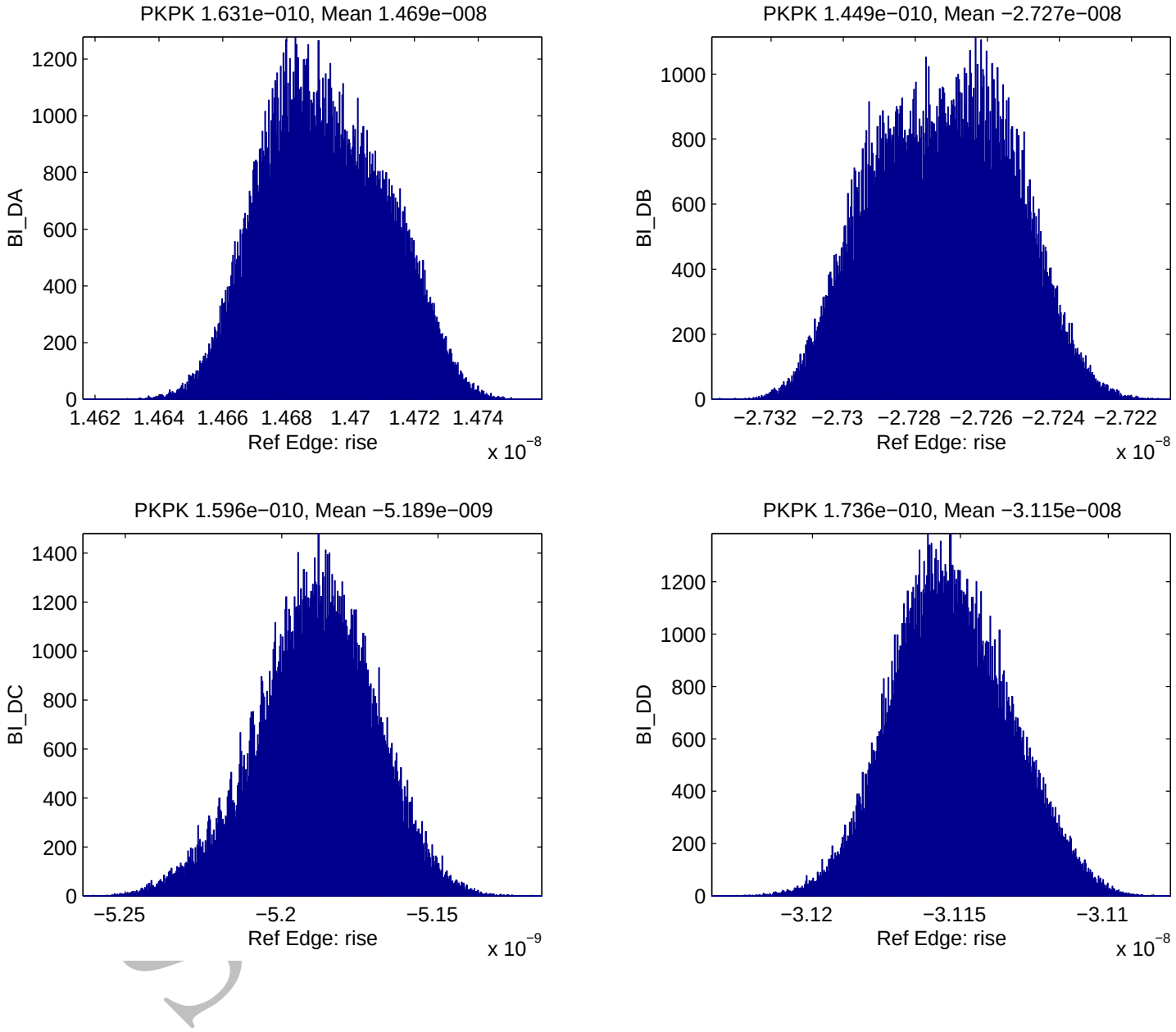


Figure 9: JTXS Histogram

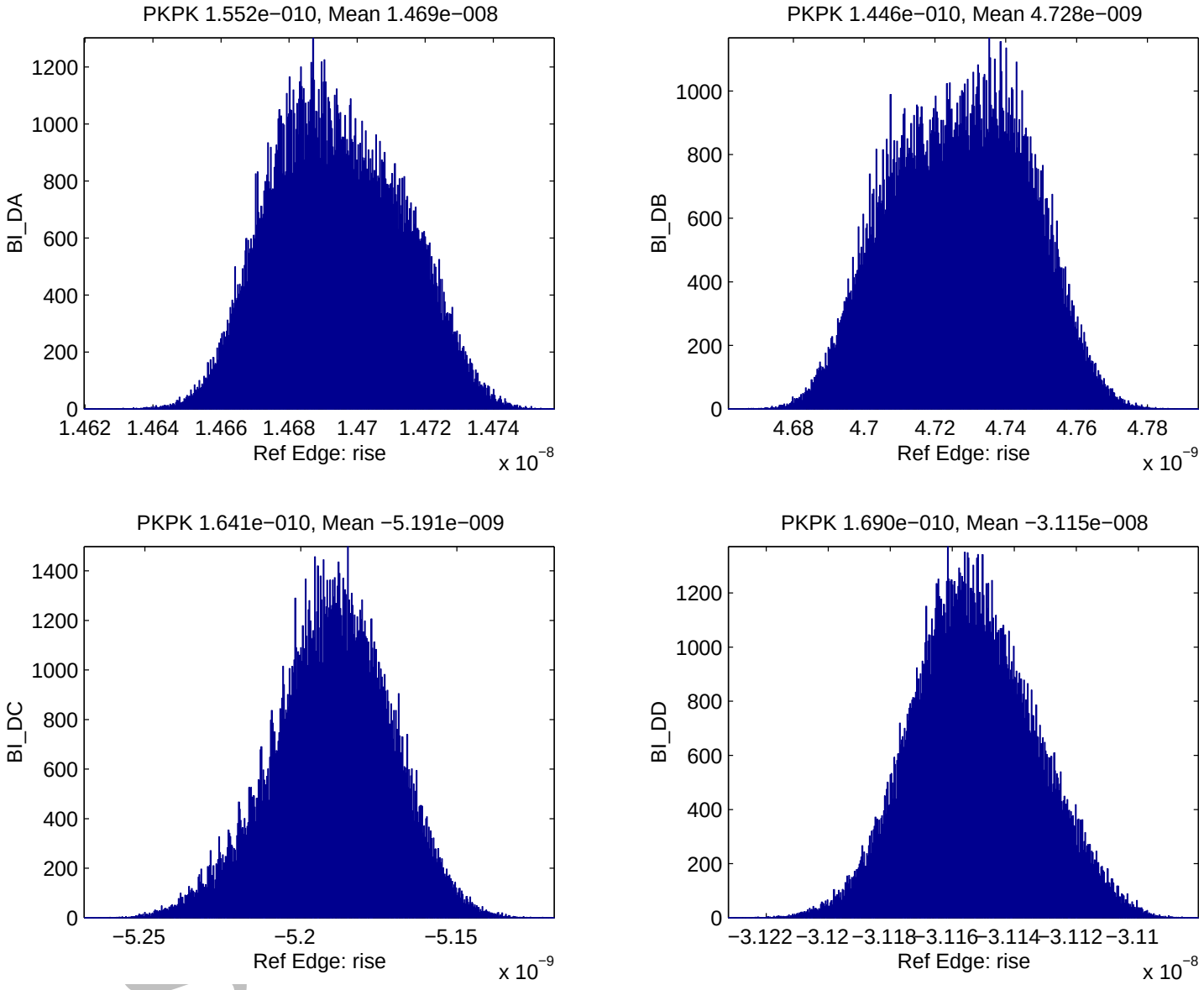
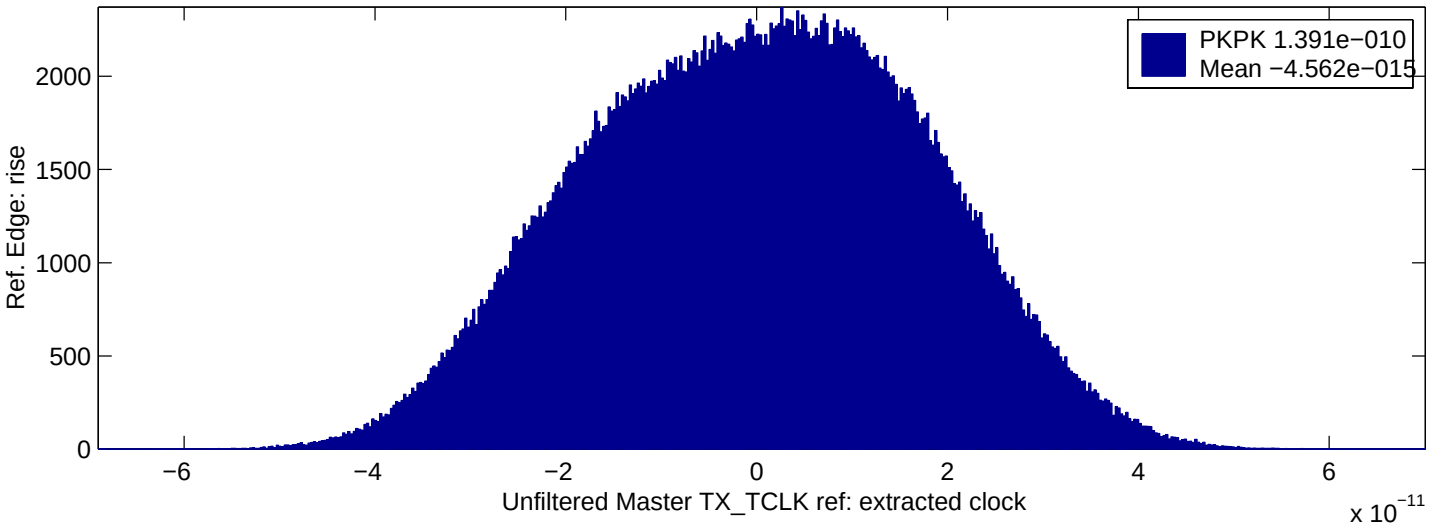


Figure 10: Jitter Histogram, Master Timing Mode



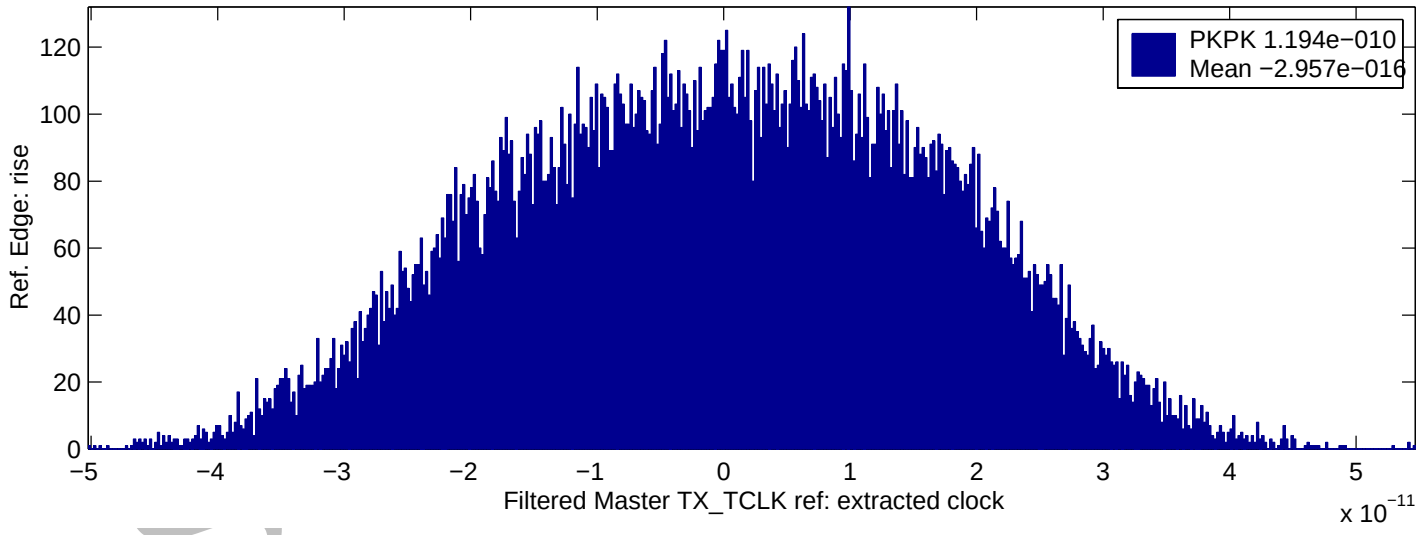


Figure 11: Jitter Histogram, Slave Timing Mode

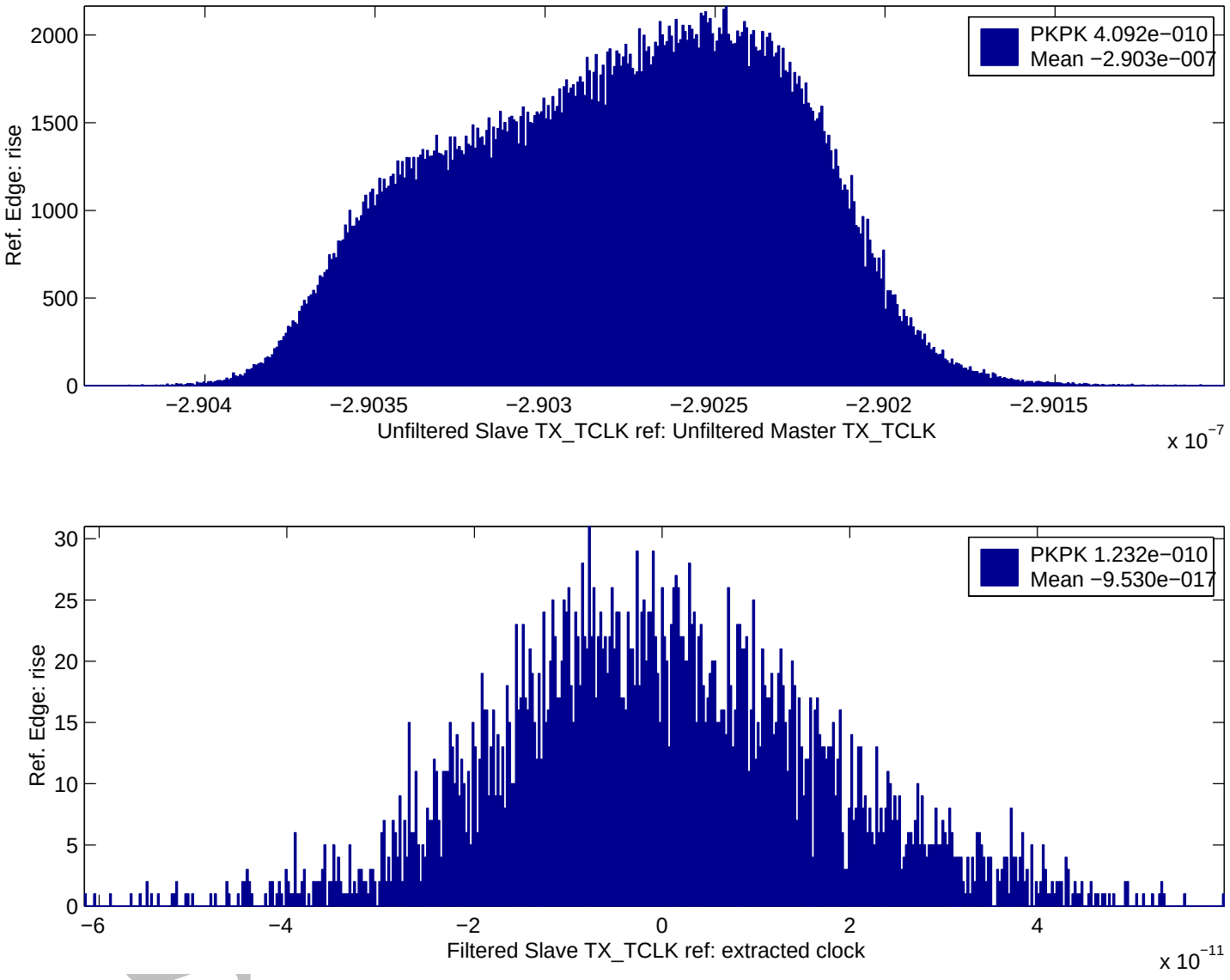
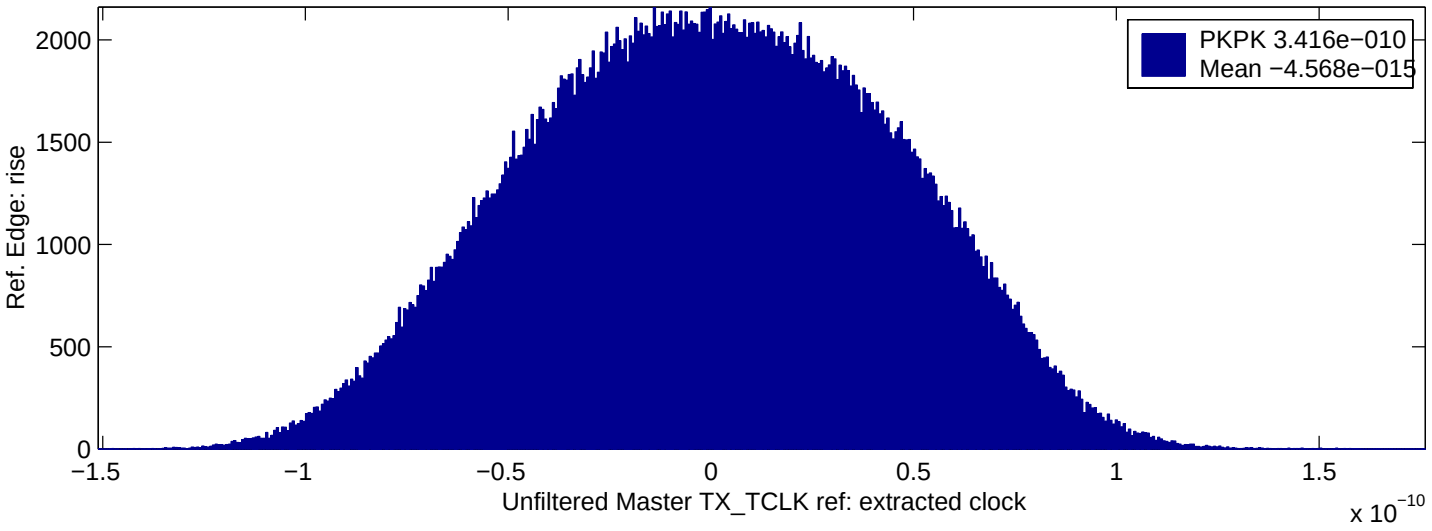


Figure 12: Jitter Histogram, Slave Timing Mode



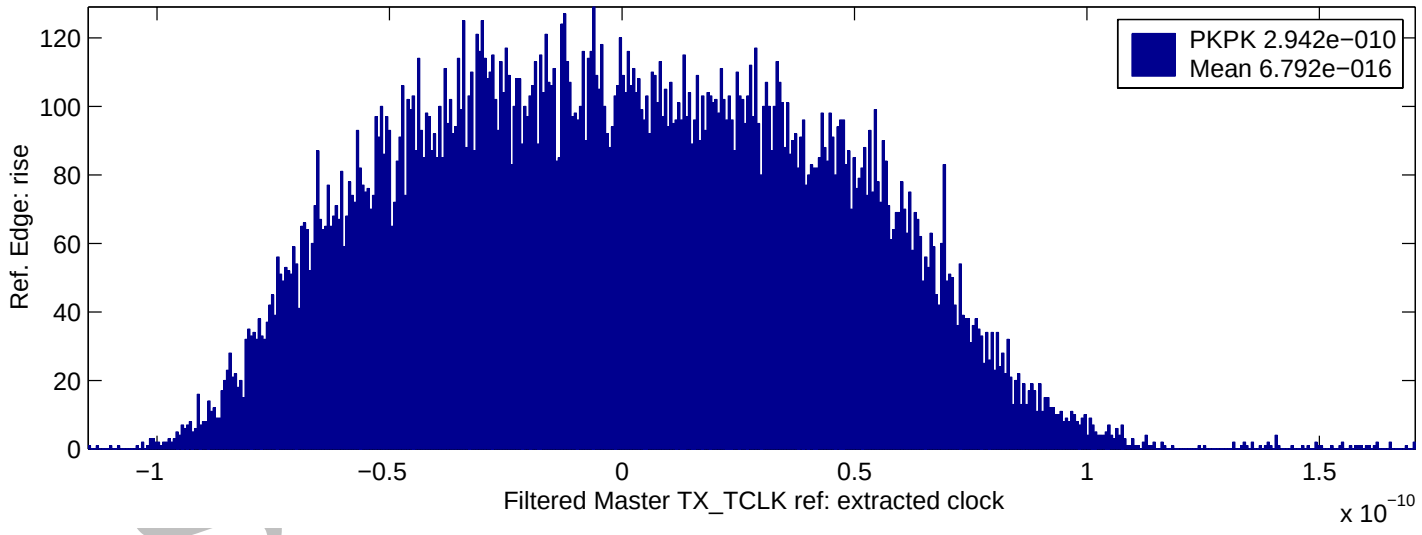


Figure 13: 1000−T Eye Diagram

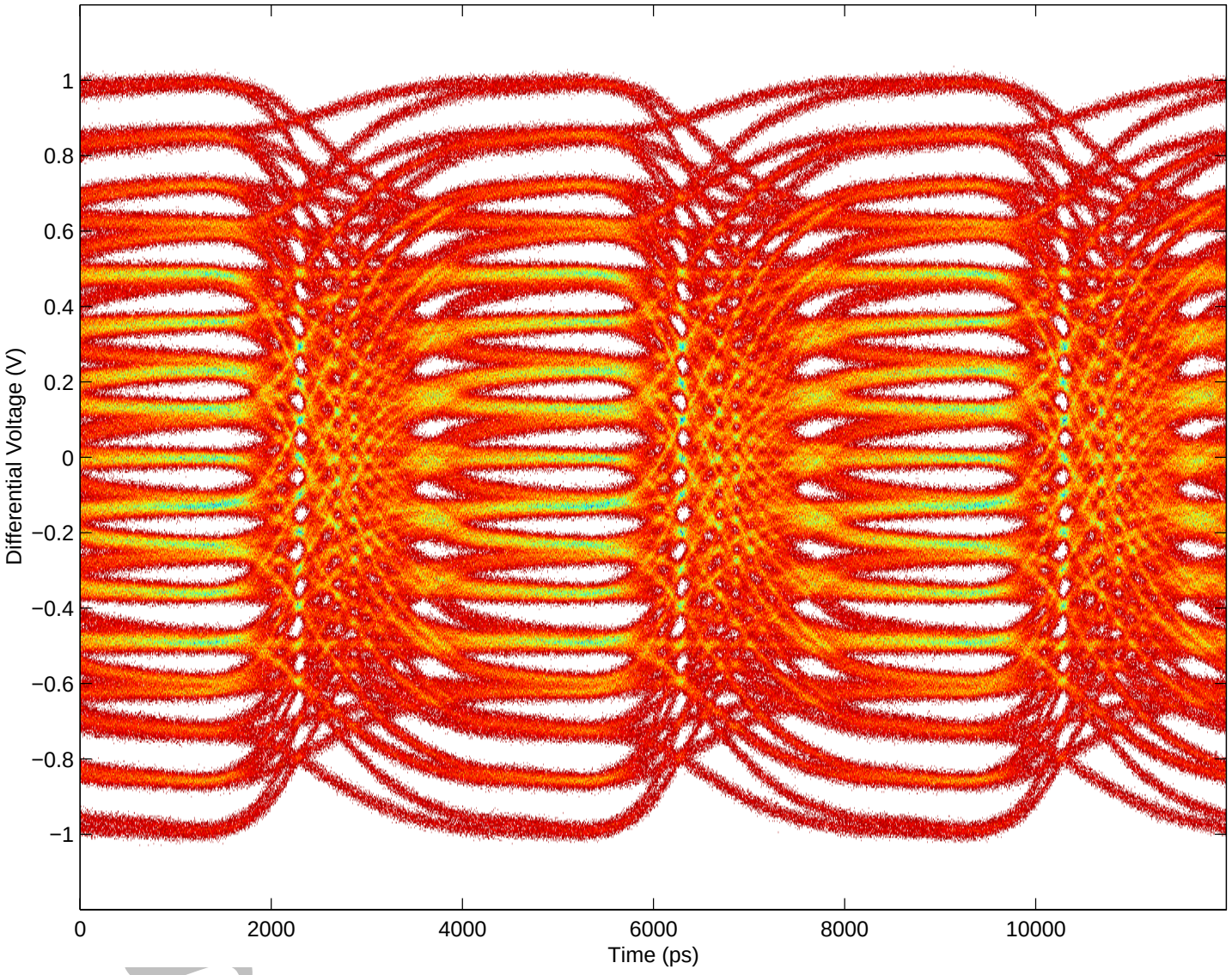


Figure 14: Peak Distortion vs. Phase Offset

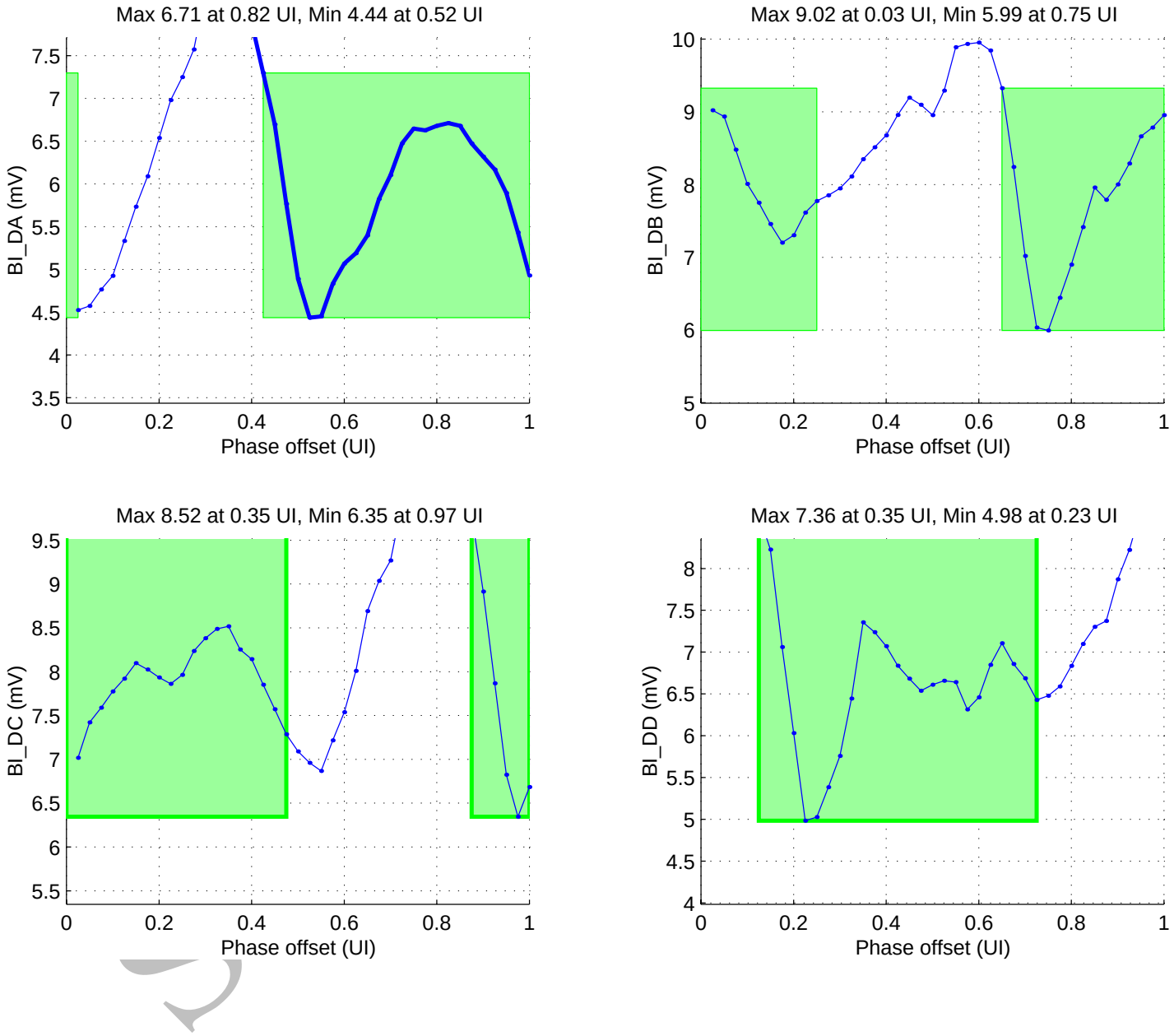


Figure 15: Distortion waveform

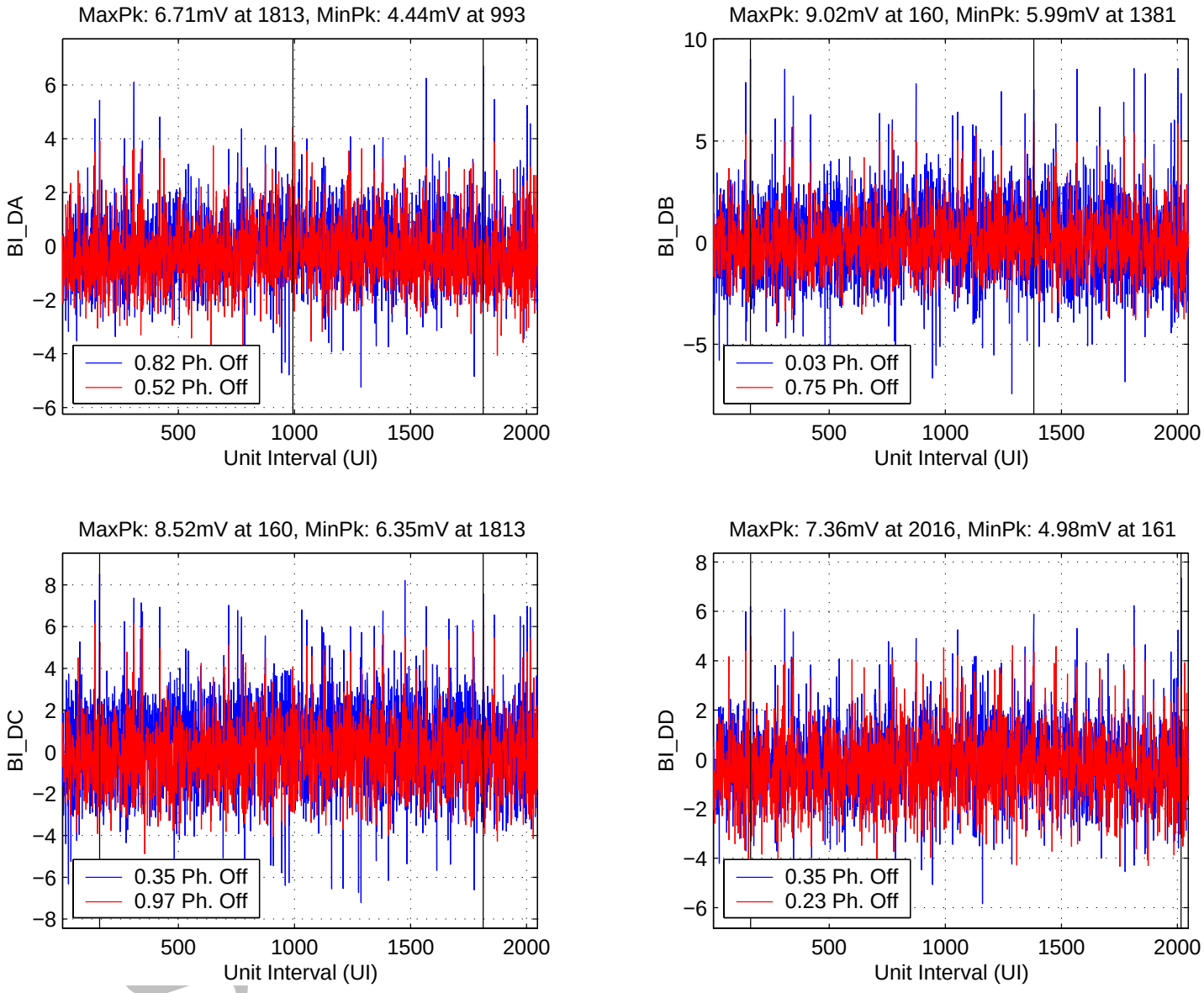


Figure 16: PSD of Distortion Waveform