Gigabit Ethernet Consortium
Clause 28 Auto-Negotiation State Machine Test Suite v5.7 Report

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Report Rev. 1.0

Enclosed are the results from the Clause 28 Auto-Negotiation State Machine testing performed on:

Device Under Test (DUT):	Computer HBL7845 NIC
Hardware Version:	Not Available
Firmware Version:	Not Available
Software Version:	1005
Miscellaneous:	PHY: Int LCX72A; Magnetics: BET 04M S558-5999-T7

The test suite referenced in this report is available at the UNH-IOL website:

ftp://ftp.iol.unh.edu/pub/ethernet/test_suites/State_Machine_Suite/State_Machine_Base_Page_Test_Suite_v5.7.pdf

Issues Observed While Testing
28.4.4 – Link Integrity and RD Active part a: It was observed that the DUT improperly implemented RD=active

For specific details regarding issues please see the corresponding test result.

Testing Completed 02/08/2006

Review Completed 02/08/2006

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Result Key

The following table contains possible results and their meanings:

Result	Interpretation
PASS	The Device Under Test (DUT) was observed to exhibit conformant behavior.
PASS with Comments	The DUT was observed to exhibit conformant behavior however an additional explanation of the situation is included, such as due to time limitations only a portion of the testing was performed.
FAIL	The DUT was observed to exhibit non-conformant behavior.
Warning	The DUT was observed to exhibit behavior that is not recommended.
Informative	Results are for informative purposes only and are not judged on a pass of fail basis.
Refer to Comments	From the observations, a valid pass or fail could not be determined. An additional explanation of the situation is included.
Not Applicable	The DUT does not support the technology required to perform these tests.
Not Available	Due to testing station or time limitations, the tests could not be performed.
Borderline	The observed values of the specified parameters are valid at one extreme, and invalid at the other.
Not Tested	Not tested due to the time constraints of the test period.

Test Setup

All tests were completed using the UNH-IOL created Python Board, with exception of test 28.1.4. This board allows us to view signaling transmitted and received before establishing a link, along with viewing the type of link signaling a device is transmitting. Some of our testing tools can be viewed at:
http://www.iol.unh.edu/consortiums/ethernet/tools/aneg/
Some tests required the use of specific Smart Bits cards to establish a link and send packets.

28.1.4 – NLP Compliance uses an oscilloscope to capture the form of the DUTs Link Test Pulse.

Test System Hardware	
Real-time DSO	LECROY,9354AM,935401934,08.0.1
Vector Network Analyzer	
Arbitrary Waveform Generator	

28.4.4 – Link Integrity and RD Active uses an Arbitrary Waveform Generator, which allows us to transmit 10BASE-T frames after establishing a 10BASE-T link.

GROUP 1: BASE PAGE TRANSMISSION

Test # and Label	Part(s)	Result(s)
28.1.1 – Transmit Link Burst Timer	**a**	**PASS**
Expected Results and Procedural Comments		
Purpose: To verify proper separation of consecutive fast link test pulse (FLP) bursts. a. The separation of FLP bursts should be 14 ± 8.3 ms		
Comments on Test Results		
a. The separation of FLPs from the rising edge of the last pulse in an FLP to the rising edge of the first pulse in an FLP has been observed:		

Transmit_link_burst_timer Of 954 FLP gaps observed	max: 14.3395 ms ± 0.5 µs	avg: 14.3380 ms ± 0.5 µs	min: 14.3370 ms ± 0.5 µs

Test # and Label	Part(s)	Result(s)
28.1.2 – Interval Timer	**a**	**PASS**
	b	**PASS**
Expected Results and Procedural Comments		
Purpose: To verify that the device under test (DUT) transmits FLPs with valid pulse separation. a. 2x interval_timer should be 125 ± 14 µs b. Interval_timer should be 62.5 ± 7 µs		
Comments on Test Results		
Timings below conform to proper values:		

2x Interval_timer Of 10,494 Clk-Clk gaps	max: 128.500 µs ± 0.5 µs	avg: 127.999 µs ± 0.5 µs	min: 127.000 µs ± 0.5 µs
Interval_timer Of 9,542 Clk-Data gaps	max: 64.500 µs ± 0.5 µs	avg: 63.793 µs ± 0.5 µs	min: 61.000 µs ± 0.5 µs

Test # and Label	Part(s)	Result(s)
28.1.3 – Transmitted Link Code Word (Base Page) Encoding	**a**	**PASS**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT transmits valid FLP data. This includes an acceptable Selector Field combination, advertises the correct abilities in the Technology Ability Field, and transmits proper initial values for the Remote Fault, Acknowledge, and Next Page bits.

a. The number of pulses in a burst should be 17-33 (inclusive).
The data in the default base code word should not change.
b. The Selector Field combination should correspond to S[4:0]=00001 as defined in Table 28A-1.
The Technology Ability Field should advertise the proper abilities as indicated in Table 28B-1.
The DUT should not advertise any abilities that it does not possess.
The value of the Remote Fault bit should be zero.
The value of the Acknowledge bit should be zero.
The value of the Next Page bit should be one if it supports Next Page and desires a Next Page exchange, otherwise it should be zero.

Comments on Test Results

a. Of 955 default Base Page FLPs observed, all contained 23 pulses and contained identical 16-bit Link Code Words which would correspond to a value of 81E1 in MII Register 4.
b. The DUT was observed to transmit by default:
- A Selector Field corresponding to 802.3.
- A Technology Ability Field corresponding to 10BASE-T half duplex, 10BASE-T full duplex, 100BASE-TX half duplex, and 100BASE-TX full duplex.
- PAUSE and ASM_DIR PAUSE bits set to zero.
- Remote Fault (RF) and Acknowledge (ACK) bits both set to zero.
- Next Page (NP) bit set to one.

Test # and Label	Part(s)	Result(s)
28.1.4 – NLP Compliance	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify the DUT's link pulse waveforms meet specification.

a. Under each test setup, the FLP's link pulses should fit within the NLP template defined in Figure 14-12, *Transmitter Waveform for link test pulse*. After the differential output voltage drops below -50 mV, it shall remain below +50 mV.

Comments on Test Results

a. The NLPs comprising an FLP were verified to conform to the LTP (NLP) template specified in Figure 14-12, *Transmitter waveform for link test pulse*. Conformance was verified for both terminations 'Test Load 1' and 'Test Load 2' specified in Figure 14-11, *Start-of-TP_IDL test load*. Also, for each test load, conformance was verified both with and without a Twisted pair cable model inserted into the channel, as illustrated in Figure 14-8, *Differential output voltage test*.

For the observed waveform envelopes for each case, refer to the Figures 1 through 4 at the end of this report.

Test # and Label	Part(s)	Result(s)
28.1.5 – Break Link Timer	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT ceases transmission within the acceptable range.

a. The DUT is sent a series of 20 identical, validly formed FLP bursts without the ACK bit set. Once reception of the FLP bursts cease, the DUT should enter the TRANSMIT DISABLE state. Of 10 gaps observed, the minimum and maximum gap between the last FLP sent from the DUT to the resumption of FLPs from the DUT, is observed. The DUT's break_link_timer should be in the range 1200 to 1500 ms.

Comments on Test Results

a. 1.243 s ≤ break_link_timer ≤ 1.341 s.

Test # and Label	Part(s)	Result(s)
28.1.6 – Link Fail Inhibit Timer	**a**	**PASS**
	b	**PASS**
	c	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT will defer for the proper amount of time before attempting to verify the status of the link determined by the Auto-Negotiation process.

a. The DUT is sent a sequence of FLPs designed to cause it to enter the FLP LINK GOOD CHECK state and resolve a 10BASE-T link. Upon entering this state, the DUT should cease FLP transmission and source a 10BASE-T link signal for the duration of link_fail_inhibit_timer. At this point, since it has not received a valid link from the Link Partner, it should determine that link_status=fail, and should cease sending a 10BASE-T link signal as it proceeds to the TRANSMIT DISABLE state. The DUT's link_fail_inhibit_timer + transmit_link_burst_timer should lie in the range 750 to 1000 ms.
b. Repeat previous sequence ('a') with the addition of 100BASE-TX advertisement. The DUT should cease FLP transmission and source a 100BASE-TX link signal for the duration of link_fail_inhibit_timer. At this point, since it has not received a valid link from the Link Partner, it should determine that link_status=fail, and should cease sending a 100BASE-TX link signal as it proceeds to the TRANSMIT DISABLE state. The DUT's link_fail_inhibit_timer should lie in the range 750 to 1000 ms.
c. Repeat sequence ('a') with the addition of 1000BASE-T advertisement, via a Next Page exchange. The DUT should cease FLP transmission and source a 1000BASE-T link signal for the duration of link_fail_inhibit_timer. At this point, since it has not received a valid link from the Link Partner, it should determine that link_status=fail, and should cease sending a 1000BASE-T link signal as it proceeds to the TRANSMIT DISABLE state. The DUT's link_fail_inhibit_timer should lie in the range 750 to 1000 ms.

Comments on Test Results

a. Of 10 observed intervals between FLP cessation and 10BASE-T link signaling cessation + transmit_link_burst_timer, the minimum was 783 ms.
b. Of 10 observed intervals between FLP cessation and 100BASE-TX link signaling cessation, the minimum was 900 ms.
c. Of 10 observed intervals between FLP cessation and 1000BASE-T link signaling cessation, the minimum was 875 ms.

Test # and Label	Part(s)	Result(s)
28.1.7 – Remote Fault Bit	**a**	**Not Applicable**

Expected Results and Procedural Comments

Purpose: To verify that if the DUT implements the Remote Fault function, the DUT properly sets the Remote Fault bit in its Link Code Word and keeps the Remote Fault bit set until exiting the COMPLETE ACKNOWLEDGE state and restarting Auto-Negotiation.

a. If the DUT supports the Remote Fault function, the Remote Fault bit should be set in all FLPs that are transmitted. The device is sent enough FLPs with the Remote Fault bit set to cause the DUT to set ability_match=true. The DUT should have the Remote Fault bit set when it sends FLPs with the ACK bit set, and when the DUT restarts Auto-Negotiation, the Remote Fault bit should still be set. The device is then sent enough FLPs to cause the DUT to obtain both an ability_match and an acknowledge_match. When the DUT restarts Auto-Negotiation, the Remote Fault bit should not be set.

Comments on Test Results

a. The DUT was observed to not support the Remote Fault function.

Test # and Label	Part(s)	Result(s)
28.1.8 – Failed Link for HCD	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT starts a re-negotiation upon the reception of a link_status=FAIL from the resolved highest common denominator (HCD) technology.

a. The DUT should restart Auto-Negotiation upon reception of the link_status=FAIL message. The DUT is connected to another 100BASE-TX device. Once the device's LEDs indicated a link, the connection was broken. Thus, referring to Figure 28-16, *Arbitration state diagram*, the DUT should leave the FLP LINK GOOD state and progress through the TRANSMIT DISABLE state to the ABILITY DETECT state.

Comments on Test Results

a. The delay observed from the end of transmission by the DUT to the first FLP transmitted by the DUT was measured to be approximately break_link_timer value, which would indicate proper state-machine behavior.

GROUP 2: BASE PAGE RECEPTION

Test # and Label	Part(s)	Result(s)
28.2.1 – Ability Match	**a**	**PASS**
	b	**PASS**
	c	**PASS**
	d	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT enters the ACKNOWLEDGE DETECT state upon reception of complete, consecutive, and consistent FLP bursts, ignoring the value of the Acknowledge bit.

a. The DUT should not enter the ACKNOWLEDGE DETECT state after the reception of 3 identical FLPs. The DUT should enter the ACKNOWLEDGE DETECT state after the reception of at least 4 complete and matching FLPs, regardless of the value of the Acknowledge bit. For use in later tests, the number of FLPs required by the DUT to enter into the ACKNOWLEDGE DETECT state (n) is recorded.
b. The device is sent (n) FLPs separated by 16 ms, where (n) is the minimum number of FLPs required to put the DUT into the ACKNOWLEDGE DETECT state (determined in part a, above). The 1st and 3rd FLPs are identical, and the 2nd and 4th FLPs are identical (assuming n=4), but one bit different than the 1st and 3rd. All FLPs are identical except for the Technology Ability Fields. The DUT should not enter the ACKNOWLEDGE DETECT state. All one-bit differences are tested.
c. The DUT is sent a sequence of (n) NLPs and FLPs. The FLPs in the sequence are all identical. The pattern is then varied such that the number of FLPs and NLPs changes; however, the total amount sent never exceeds (n).
d. The DUT should reset to its default Base Page and be sending FLPs with the Acknowledge Bit not set, after restarting Auto-Negotiation.

Comments on Test Results

a. The device was observed to not set its ACK bit upon receipt of 3 identical FLPs. The device was observed to set its ACK bit upon receipt of the fourth FLP regardless of the ACK bit, indicating that the DUT entered the ACKNOWLEDGE DETECT state.
b. In all cases, the DUT was observed to properly not set its ACK bit upon receipt of the alternating FLPs.
c. In all cases, the DUT was observed to properly not set its ACK bit upon receipt of alternating FLPs and NLPs.
d. The DUT was observed to properly reset to its default Base Page.

Test # and Label	Part(s)	Result(s)
28.2.2 – Acknowledge Match	**a**	**PASS**
	b	**PASS**
	c	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT enters the COMPLETE ACKNOWLEDGE state only after receiving 3 consecutive and consistent FLPs with the Acknowledge bit set.

a. The DUT is sent (n) FLPs without the ACK bit set, and a certain amount of FLPs with the ACK bit set, but otherwise identical. Where (n) is the value found in test #28.2.1 to cause the DUT to enter the ACKNOWLEDGE DETECT state. The DUT should obtain an acknowledge match and enter the COMPLETE ACKNOWLEDGE state after the reception of 3 such FLPs with the ACK bit set.
b. The DUT is sent (n) identical FLPs without the ACK bit set, then another identical FLP, but with the ACK bit set, then an FLP that is one bit different, and finally an FLP identical to the first FLP with the ACK bit set. In this way, the DUT does not see three consecutive FLPs with the ACK bit set and thus should not determine acknowledge_match=TRUE. The DUT should never enter the COMPLETE ACKNOWLEDGE state, and should send out FLPs with the Acknowledge bit set until nlp_test_max_timer expires. Following the FLPs should be a gap of 'break_link_timer' until FLP transmission resumes. All one-bit differences are tested.
c. The DUT is sent two groups of FLPs. The first group is comprised of (n) valid FLPs. The second group is comprised of one FLP with ACK, followed by one NLP, followed by FLPs with ACK until (m) is reached, where (m) is the minimum number of FLPs with ACK required to put the DUT into the COMPLETE ACKNOWLEDGE state (determined in part a, above). All the FLPs are the same except for the Acknowledge bit. The patterns are re-transmitted increasing the amount of NLPs sent in the second group, but never exceeding (m).

Comments on Test Results

a. The DUT was observed to enter the COMPLETE ACKNOWLEDGE state after the reception of 3 FLPs with the ACK bit set.
b. The DUT continued transmission of FLPs with ACK set after it received the last FLP from the traffic generator until the nlp_test_max_timer expired. Additionally, following the last FLP from the DUT was a gap of approximately break_link_timer before FLP transmission resumed.
c. In all cases, the DUT was observed to properly not enter the COMPLETE ACKNOWLEDGE state.

Test # and Label	Part(s)	Result(s)
28.2.3 – Consistency Match	**a**	**PASS**
	b	**PASS**
	c	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT performs a consistency match test on received FLPs.

a. The DUT is sent (n) FLPs without the ACK bit set and then (m) FLPs with the ACK bit set. The transmitted abilities in the first set of (n) FLPs differ from those in the second set of (m) FLPs. Where (n) is the value found in test #28.2.1 and where (m) is the value found in test #28.2.2. All FLPs are sent with 16 ms spacing. The DUT should cease transmitting FLPs immediately once the inconsistent FLPs are received. All one bit different combinations are tested.
b. The DUT should require 1 FLP to determine that the link partner is Auto-Negotiation able. The DUT should then require 3 identical FLPs (ignoring the ACK bit) in order to set ability_match=true. If the 3 FLPs received all had the ACK bit set, then acknowledge_match=true as well; however, upon transition to the ACKNOWLEDGE DETECT state, acknowledge_match should be reset to false. At this point, the DUT may re-evaluate acknowledge_match, prior to receiving additional FLPs, and determine that the last three FLPs were identical with the ACK bit set, and reset acknowledge_match to true. In this case, the DUT should enter COMPLETE ACKNOWLEDGE after receiving 4 FLPs, where at least the last three FLPs are identical with the ACK bit set. Alternatively, the DUT's acknowledge_match function may only update following the receipt of a new FLP. In this case acknowledge_match cannot be set true until another identical FLP with ACK bit set is received. Thus, a total of 5 identical FLPs would be required for the DUT to enter the COMPLETE ACKNOWLEDGE state, where the last three FLPs received must have the ACK bit set.
c. The DUT is sent (n) valid FLPs and then (m) additional pulses varying between NLPs and FLPs with the Acknowledge bit set. All the FLPs are identical except for the Acknowledge bit. The patterns are re-transmitted increasing the amount of NLPs sent in the second group, but never exceeding (m).

Comments on Test Results

a. In all cases, the DUT properly detected consistency_match=false and terminated transmission of FLPs, even if an FLP was being transmitted.
b. The DUT was observed to enter the COMPLETE ACKNOWLEDGE state after receiving 4 identical FLPs with the ACK bit set.
c. In all cases, the DUT properly ceased transmission of FLPs.

Test # and Label	Part(s)	Result(s)
28.2.4 – Complete Acknowledge	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT sends out a valid number of Link Code Words after the COMPLETE ACKNOWLEDGE state has been entered.

a. The DUT is sent (n) FLPs without the ACK bit set and then (m) FLPs with the ACK bit set (enough to put the DUT into COMPLETE ACKNOWLEDGE), but otherwise identical. After the COMPLETE ACKNOWLEDGE state has been entered, the DUT should send out remaining_ack_cnt FLPs containing its Link Code Word. The remaining_ack_cnt is defined as 6 to 8 inclusive, additional FLPs.

Comments on Test Results

a. The DUT transmitted 7 additional FLPs with ACK bit set before it attempted to establish a link.

Test # and Label	Part(s)	Result(s)
28.2.5 – Behavior with Incomplete FLPs	**a**	**PASS**
	b	**Informative**
	c	**PASS**

Expected Results and Procedural Comments

Purpose: To observe the DUT's behavior upon receipt of incomplete FLP bursts.

a. The DUT should not enter the ACKNOWLEDGE DETECT state upon reception (n) FLPs, when the "FLPs" contain only 9 or fewer data bits. The FLPs must be spaced so that the time required to transmit the entire sequence is greater than nlp_test_max_timer.
b. INFORMATIVE: The DUT may enter the ACKNOWLEDGE DETECT state upon reception of the minimum number of "FLPs" (as in part a) when the "FLPs" contain 10 to 16 data bits. This value should correspond to the implemented rx_bit_cnt_check value.
c. The DUT should not enter the ACKNOWLEDGE DETECT state upon reception of FLPs split into two halves, each half being separated by 16 ms.

Comments on Test Results

a. The DUT was observed to not set its ACK bit upon receipt of "FLPs" with only 1 through 9 data bits.
b. The DUT was observed to set its ACK bit upon receipt of FLPs with 17 clock pulses (16 data bits). This suggests that the implemented rx_bit_cnt_check value is 17. This test is not judged on a pass/fail basis as a DUT may "receive" an "FLP" with fewer than 17 clock pulses without timing out (refer to Figure 28-15, *Receive state diagram*); however, there is no requirement that received short FLPs be evaluated by the ability match function.
c. The DUT was observed to not set its ACK bit upon receipt of a 'normal' FLP pulled apart in time, as described in the test procedure.

Test # and Label	Part(s)	Result(s)
28.2.6 – Acceptance of Long FLPs	**a**	**PASS**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT properly accepts FLPs containing more than 16 data positions by ignoring all but the first 16 data bits.

a. The DUT is sent 4 long FLPs, each with an extra data one (requiring 1 extra data and 1 extra clock pulse). It should enter the ACKNOWLEDGE DETECT state
b. The DUT is sent 4 long FLPs, each with 5 extra data pulses, (requiring 2 extra data, and 5 extra clock pulses). It should enter the ACKNOWLEDGE DETECT state upon receipt of these FLPs.

Comments on Test Results

a. The DUT properly entered the ACKNOWLEDGE DETECT state as observed by the setting of its ACK bit.
b. The DUT properly entered the ACKNOWLEDGE DETECT state as observed by the setting of its ACK bit.

Test # and Label	Part(s)	Result(s)
28.2.7 – Next Page and Remote Fault Bits	**a**	**PASS**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT can handle the reception of an FLP from a Next Page capable device as well as the reception of a flagged Remote Fault bit.

a. The DUT is sent (n) FLPs with the Next Page bit set to one, and (m) FLPs with the NP and ACK bits set to one. It should enter the COMPLETE ACKNOWLEDGE state.
b. The DUT is sent (n) FLPs with the Remote Fault bit set to one, and (m) FLPs with the RF and ACK bits set to one. It should set the Remote Fault bit in its MII Status Register, and any other behavior is unpredictable.

Comments on Test Results

a. The DUT properly entered the COMPLETE ACKNOWLEDGE state.
b. The DUT properly entered the COMPLETE ACKNOWLEDGE state.

Test # and Label	Part(s)	Result(s)
28.2.8 – Selector Field Combinations	**a**	**PASS**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT accepts FLPs with the Selector Field set to a reserved combination or to the defined Isochronous Ethernet combination.

a. The DUT is sent (n) identical FLPs with Selector Fields of 00000, 11000, 11111, and 01000 (Isochronous Ethernet). The DUT should enter the ACKNOWLEDGE DETECT state in all cases.
b. The DUT is sent (n) identical FLPs with Selector Fields of 00000, 11000, 11111, and 01000 (Isochronous Ethernet) along with (m) additional, identical FLPs; enough to put the DUT through the COMPLETE ACKNOWLEDGE state. The DUT should enter the COMPLETE ACKNOWLEDGE state on all Selector Field combinations.

Comments on Test Results

a. In all cases, the DUT properly entered the ACKNOWLEDGE DETECT state as observed by the setting of its ACK bit.
b. In all cases, the DUT properly entered the COMPLETE ACKNOWLEDGE state.

Test # and Label	Part(s)	Result(s)
28.2.9 – Technology Ability Field Bits	**a**	**PASS**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT accepts FLPs with different combinations of the Technology Ability Field bits set to logic one.

a. The DUT is sent (n) identical FLPs with varying Technology Ability Field bits set to one. It should enter the ACKNOWLEDGE DETECT state on all combinations of Technology Ability Field bits set to one.
b. The DUT is sent (n) identical FLPs with varying Technology Ability Field bits set to one along with (m) additional identical FLPs, enough to put the DUT through the COMPLETE ACKNOWLEDGE. The DUT should enter the COMPLETE ACKNOWLEDGE state on all combinations of Technology Ability Field bits set to one.

Comments on Test Results

a. In all cases, the DUT properly entered the ACKNOWLEDGE DETECT state as observed by the setting of its ACK bit.
b. In all cases, the DUT properly entered the COMPLETE ACKNOWLEDGE state.

Test # and Label	Part(s)	Result(s)
28.2.10 – Identification of Link Partner as Auto-Negotiation Able	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT is able to recognize its link partner as capable of Auto-Negotiation within specification.

a. The DUT should recognize the Link Partner as Auto-Negotiation able when flp_cnt=done. Note: According to Figure 28-15, *Receive state diagram*, flp_cnt gets incremented to '1' after the *second* received pulse. This first pulse does not increment flp_cnt. Thus, the conformant range for flp_cnt (6 to 17) corresponds to a range of 7 to 18 received pulses.

Comments on Test Results

a. flp_cnt was observed to be 9 (thus flp_cnt=done after 10 pulses).

Test # and Label	Part(s)	Result(s)
28.2.11 – Range of NLP Timer	**a**	**PASS**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT accepts FLP bursts with proper spacing, and refuses those with spacing outside of the acceptable range.

a. The DUT is sent (n) FLPs at a valid spacing, which cause it to enter the ACKNOWLEDGE DETECT state and set its Acknowledge bit. This process is repeated, but the FLP-to-FLP spacing is *decreased* until the DUT no longer sets its Acknowledge bit. The values from when the DUT sets its ACK bit to when the DUT no longer sets its ACK bit are taken as the range of the nlp_test_min_timer. This range should lie between 5 ms and 7 ms.
b. The above procedure is repeated, but instead the FLP spacing is *increased*, and a range for the nlp_test_max_timer is determined. This range should lie between 50 ms and 150 ms.

Comments on Test Results

a. 5.6 ms ≤ nlp_test_min_timer ≤ 6.2 ms.
b. 73 ms ≤ nlp_test_max_timer ≤ 129 ms.

Test # and Label	Part(s)	Result(s)
28.2.12 – Range of FLP Test Timer	**a**	**PASS**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT determines that its link partner is Auto-Negotiation able upon receiving pulses spaced within flp_test_min_timer and flp_test_max_timer, and does not recognize a device as Auto-Negotiation able upon receiving pulses spaced outside the acceptable range.

a. The flp_test_min_timer should lie between 5 µs and 25 µs.
b. The flp_test_max_timer should lie between 165 µs and 185 µs.

Comments on Test Results

a. 15 µs ≤ flp_test_min_timer ≤ 16 µs.
b. 168 µs ≤ flp_test_max_timer ≤ 169 µs.

Test # and Label	Part(s)	Result(s)
28.2.13 – Range of Data Detect Timer	**a**	**PASS**
	b	**PASS**
	c	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT accepts data pulses with proper spacing and refuses data pulses with spacing outside the acceptable range.

a. The data_detect_min_timer should lie between 15 µs and 47 µs.
b. The data_detect_max_timer should lie between 78 µs and 100 µs.
c. The DUT should ignore the first data pulse and decode the second data pulse as logic one causing the DUT to enter the ACKNOWLEDGE DETECT state.

Comments on Test Results

a. 16 µs ≤ data_detect_min_timer ≤ 30 µs.
b. 84 µs ≤ data_detect_max_timer ≤ 96 µs.
c. The DUT properly entered the ACKNOWLEDGE DETECT state

Test # and Label	Part(s)	Result(s)
28.2.14 – Transmit Disable State	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT enters the ABILITY DETECT state upon completion of break_link_timer from the TRANSMIT DISABLE state.

a. The DUT should resume FLP transmission after break_link_timer is finished, regardless of the received FLPs during the time where the DUT was in the TRANSMIT DISABLE state.

Comments on Test Results

a. The DUT was observed to resume FLP transmission after the break_link_timer was finished.

Test # and Label	Part(s)	Result(s)
28.2.15 – Priority Resolution Function	**a**	**PASS**
	b	**Informative**

Expected Results and Procedural Comments

Purpose: To verify that the device under test properly configures the highest common denominator (HCD) technology for the transmitted technologies in a link code word.

a. In every case, the DUT should resolve a link at the highest priority possible based on the priority resolution function for the technologies advertised
b. INFORMATIVE: The DUT should enter the FLP LINK GOOD CHECK state and may disable all Ethernet PMAs.

Comments on Test Results

a. The DUT was observed to resolve a link at the highest priority possible in every case based on the technologies advertised.
b. The DUT was observed to enter the FLP LINK GOOD CHECK state and disable all Ethernet PMAs.

GROUP 3: PARALLEL DETECTION

Test # and Label	Part(s)	Result(s)
28.3.1 – Single Link Ready	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT properly monitors the status of single_link_ready during Parallel Detection.

a. The DUT is sent 'lc_max' 10BASE-T Link Test Pulses causing the device to transition to the LINK STATUS CHECK state in Figure 28-16, *Arbitration state diagram*. According to Figure 28-17, *NLP Receive Link Integrity Test state diagram*, after the link_loss_timer expires, the DUT should see link_status[NLP]=FAIL, and thus detect single_link_ready=false. Referring to Figure 28-16, this should immediately cause a transition from LINK STATUS CHECK to PARALLEL DETECTION FAULT. A conformant device should cease FLP transmission for approximately link_loss_timer when parallel detecting a 10BASE-T link.

Comments on Test Results

a. The DUT ceased FLP transmission for approximately link_loss_timer + transmit_link_burst_timer after reception of link test pulse transmission. This shows that the DUT properly transitions to the PARALLEL DETECTION FAULT state once single_link_ready=false.

Test # and Label	Part(s)	Result(s)
28.3.2 – Range of Auto-Negotiation Wait Timer	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the implemented value of autoneg_wait_timer is within the specified range of 500 to 1000ms

a. The DUT is sent NLPs continuously and the delay between the cessation of FLPs and the transmission of NLPs from the DUT is measured. The minimum observed value of this interval is taken as the upper bound of the autoneg_wait_timer. The lower bound is obtained by finding X, where X is the number of NLPs that will cause the DUT to never enter FLP LINK GOOD CHECK state. Sending X+1 NLPs will cause the DUT to enter the FLP LINK GOOD CHECK state. The value of X, along with the value of lc_max from test 28.4.1 and the link_loss_timer from test 28.4.3 are used to calculate the lower bound (see results).

   The range of the autoneg_wait_timer should lie within the range of 500 ms to 1000 ms.

Comments on Test Results

a. 512 ms ≤ autoneg_wait_timer ≤ 555.775 ms.

   When sent a stream of NLPs spaced at 7 ms, the minimum of 10 observed gaps from FLP transmission to NLP (10BASE-T link) transmission was 555.775 ms. This establishes the upper bound on autoneg_wait_timer.

   When 64 NLPs spaced at 7 ms were sent, the DUT transmitted FLPs after cessation of NLP reception. When 65 NLPs were sent, the DUT transmitted NLPs approximately link_loss_timer after the last received NLP (105 ms observed). From 10BASE-T related tests lc_max was 3, and link_loss_timer was between 85 ms and 111 ms. For the case of 64 NLPs, 63 seven ms gaps were sent, 2 seven ms gaps were consumed for lc_max, thus a time of: (63 – 2) * 7 ms + 85 ms = 512 ms. This establishes the lower bound on autoneg_wait_timer.

GROUP 4: 10BASE-T RELATED TESTS

Test # and Label	Part(s)	Result(s)
28.4.1 – Link Count Max	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT implements lc_max within 2 to 10 Link Test Pulses.

a. The DUT should cease FLP transmission for approximately link_loss_timer after receiving between 2 to 10 validly spaced Link Test Pulses.

Comments on Test Results

a. lc_max was observed to be 3.

Test # and Label	Part(s)	Result(s)
28.4.2 – Range of Link Test Timers	**a**	**PASS**
	b	**PASS**
	c	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT accepts NLPs (link test pulses) with proper spacing, and refuses those with spacing outside of the acceptable range.

a. The DUT is sent 'lc_max' Link Test Pulses. The spacing between these pulses is decreased until the DUT no longer enters the LINK STATUS CHECK state. The link_test_min_timer should lie between 2 ms and 7 ms.
b. The DUT is sent 'lc_max' Link Test Pulses. The spacing between these pulses is increased until the DUT no longer enters the LINK STATUS CHECK state. The link_test_max_timer should lie between 25 ms and 150 ms.
c. The DUT is sent a continuous stream of Link Test Pulses with the spacing that is less than link_test_min_timer. The device should never enter the LINK STATUS CHECK state.

Comments on Test Results

a. 5.6 ms ≤ link_test_min_timer ≤ 6.3 ms.
b. 67 ms ≤ link_test_max_timer ≤ 95 ms.
c. The DUT was observed to not enter the LINK STATUS CHECK state.

Test # and Label	Part(s)	Result(s)
28.4.3 – Range of Link Loss Timer	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT implements link_loss_timer within 50 ms and 150 ms.

a. The DUT is sent one second of validly spaced Link Test Pulses in order to form a valid 10BASE-T link. A gap is introduced followed by another second of validly spaced Link Test Pulses. The length of the gap is increased until the DUT is observed to drop link. The DUT should keep link with a gap ranging from 50 ms to 150 ms.

Comments on Test Results

a. 85 ms ≤ link_loss_timer ≤ 111 ms.

Test # and Label	Part(s)	Result(s)
28.4.4 – Link Integrity and RD Active	**a**	**FAIL**
	b	**Not Applicable**
	c	**PASS**
	d	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT maintains 10BASE-T link upon reception of valid 10BASE-T frames.

a. The DUT is sent 'lc_max' pulses directly followed by a continuous stream of frames. The frames should satisfy RD=active such that when autoneg_wait_timer=done the device will begin transmitting valid 10BASE-T link.
b. The DUT is sent one less than 'lc_max' pulses directly followed by a continuous stream of frames. The DUT should never establish a link, and thus, never send out NLPs and never receive the frames. Figure 28-17, *NLP Receive Link Integrity Test state diagram*, requires that the DUT receive the number of Link Test Pulses determined by lc_max before determining link_status=READY.
c. The DUT is sent a continuous stream of frames with no Link Test Pulses. The DUT should never establish a link, and thus, never send out NLPs and never receive frames.
d. The DUT is sent a continuous stream of validly spaced Link Test Pulses until a 10BASE-T link is observed. Through the use of a DPDT relay, the receive channel of the DUT is then switched to a 100BASE-TX source for several seconds, and then switched back to the 10BASE-T frames. A conformant device should drop the 10BASE-T link and reestablish a 100BASE-TX link through Parallel Detection while the device is receiving the 100BASE-TX signaling and not establish a link upon the detection of 10BASE-T frames.

Comments on Test Results

a. It was observed that the DUT failed to remain in the NLP TEST PASS state after receiving 'lc_max' Link Test Pulses followed by a constant stream of frames. The DUT was observed to transition to the NLP TEST FAIL RESET state, indicating that the RD state variable was improperly set to the value of *idle* upon the reception of 10BASE-T frames.
b. This test was not performed. As was observed in part (a), the DUT did not properly implement the RD variable, therefore a test result from part (b) would be invalid.
c. The DUT did not establish a 10BASE-T link from the reception of valid 10BASE-T frames spaced at 16 ms.
d. The DUT was observed to source 10BASE-T Link Test Pulses after receiving validly spaced Link Test Pulses. When the DUT started receiving 100BASE-TX signaling, it was observed to drop the 10BASE-T link and parallel detect to a 100BASE-TX link. Upon switching back to the10BASE-T frames, the DUT was observed to drop the 100BASE-TX link and properly send FLPs.

Figure 1: LTP Mask (Test Load 1, No Twisted Pair Model)

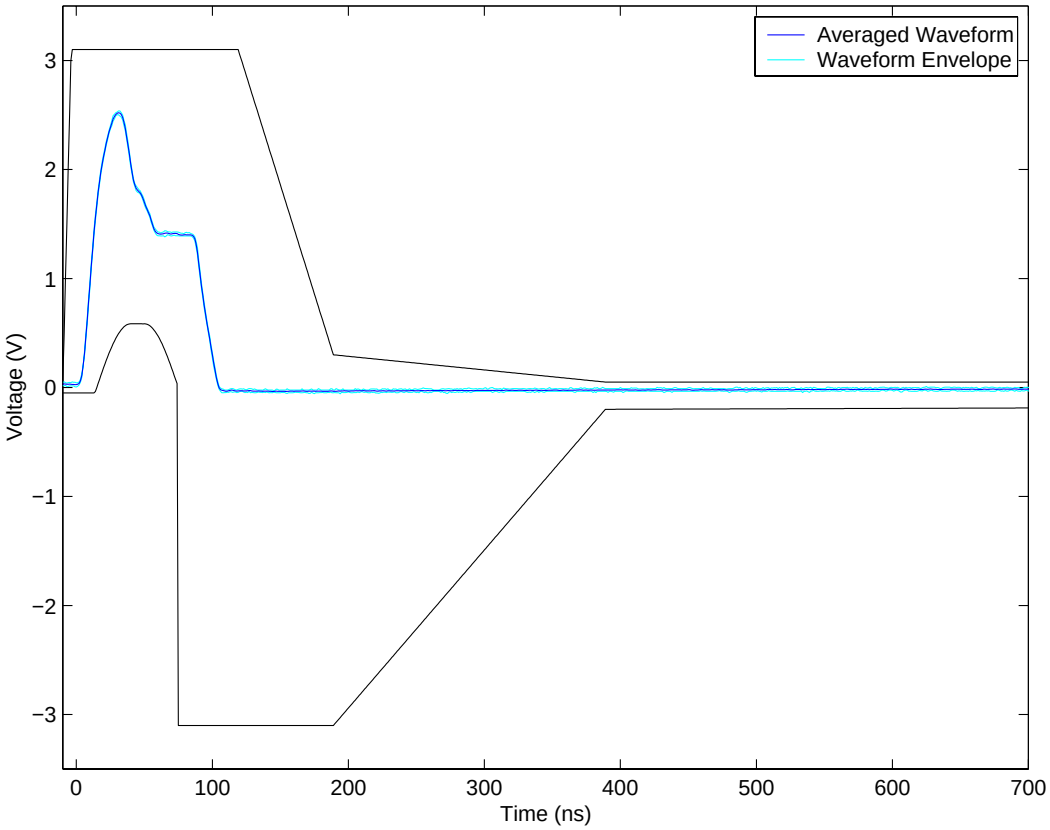

Figure 2: LTP Mask (Test Load 1, With Twisted Pair Model)

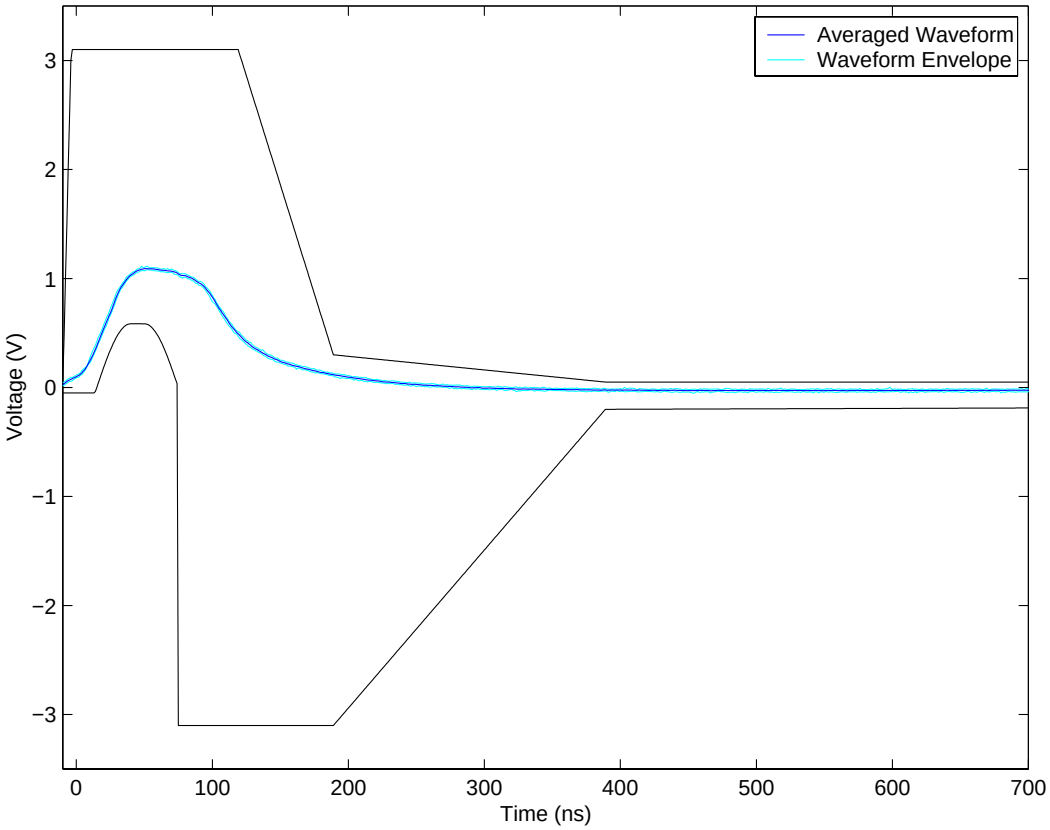

Figure 3: LTP Mask (Test Load 2, No Twisted Pair Model)

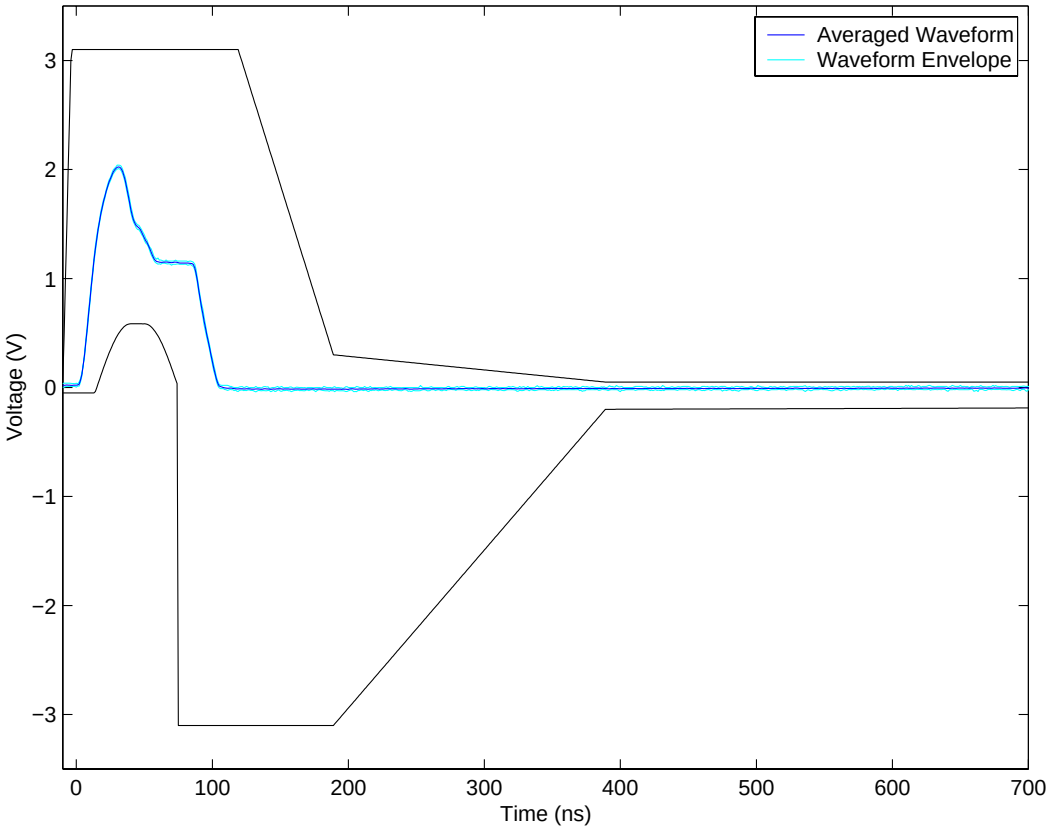

Figure 4: LTP Mask (Test Load 2, With Twisted Pair Model)