Gigabit Ethernet Consortium
Clause 22, 28 &40 Auto-Negotiation Management Registers Test Suite v2.7 Report

UNH-IOL — 121 Technology Drive, Suite 2 — Durham, NH 03824 — +1-603-862-0090
Consortium Manager: Gerard Nadeau — grn@iol.unh.edu — +1-603-862-0166

Jason Contact
Computer Inc.
1234 Fake St.
Somewhere, LL 99999

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Enclosed are the results from the Clause 22, 28 & 40 Auto-Negotiation Management Register Conformance testing performed on:

Device Under Test (DUT):	Computer HBL7845 NIC
Hardware Version:	Hardware Version
Firmware Version:	Firmware Version
Software Version:	Software Version
Miscellaneous:	PHY: AAA; MAC: BBB; Magnetics: CCC; Serial Number: DDD

The test suite referenced in this report is available at the UNH-IOL website:

ftp://ftp.iol.unh.edu/pub/ethernet/test_suites/Management_Register_Test_Suite/Management_Register_Test_Suite_v2.7.pdf

Issues Observed While Testing
28.2.3 – Remote Fault part b: The DUT was observed to improperly implement the Remote Fault bit.

For specific details regarding issues please see the corresponding test result.

Testing Completed 02/08/2006

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Review Completed 02/08/2006

John Q. Tester
jonny5@iol.unh.edu

John Q. Reviewer
johnqreviewer@iol.unh.edu

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Result Key

The following table contains possible results and their meanings:

Result	Interpretation
PASS	The Device Under Test (DUT) was observed to exhibit conformant behavior.
PASS with Comments	The DUT was observed to exhibit conformant behavior however an additional explanation of the situation is included, such as due to time limitations only a portion of the testing was performed.
FAIL	The DUT was observed to exhibit non-conformant behavior.
Warning	The DUT was observed to exhibit behavior that is not recommended.
Informative	Results are for informative purposes only and are not judged on a pass of fail basis.
Refer to Comments	From the observations, a valid pass or fail could not be determined. An additional explanation of the situation is included.
Not Applicable	The DUT does not support the technology required to perform these tests.
Not Available	Due to testing station or time limitations, the tests could not be performed.
Borderline	The observed values of the specified parameters are valid at one extreme, and invalid at the other.
Not Tested	Not tested due to the time constraints of the test period.

SampleReport

Test Setup

All tests completed were completed using the UNH-IOL created Python Board. This board allows us to view signaling transmitted and received before establishing a link, along with viewing the type of link signaling a device is transmitting. Some of our testing tools can be viewed at: http://www.iol.unh.edu/consortiums/ethernet/tools/aneg/ Some tests required the use of specific Smart Bits cards to establish a link and send packets.

Sample Report

GROUP 1: CLAUSE 22 MANAGEMENT FUNCTION REQUIREMENTS

Test # and Label	Part(s)	Result(s)
22.1.1 – Main Reset	**a**	**PASS**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that bit 0.15 controls the resetting of the PHY and Auto-Negotiation process.

a. Bit 15 of the Control Register (MII Register 0) gives management the ability to reset all of the Control and Status Registers, as well as restarting the Auto-Negotiation process. Once the DUT is transmitting FLPs, bit 15 of the Control Register is set. The DUT should stop Auto-Negotiation, wait approximately break_link_timer, and then restart Auto-Negotiation by sending FLPs.
b. Once Auto-Negotiation has resumed transmissions, the value of the Control and Status Registers are read. The Control Register is written with a value different than observed from the read. A link is established thus that the value within the Status Register is different than observed from the read. Bit 0.15 is then set to one, and the Control and Status Registers are read again. The value within the Control and Status Registers should be identical to the value of the first read.

Comments on Test Results

a. The DUT properly halted FLP transmission for approximately break_link_timer and then restarted Auto-Negotiation by sending FLPs.
b. The Control and Status Registers were observed to contain consistent values, indicating bit 0.15 properly reset the Control and Status Registers to their default value.

Test # and Label	Part(s)	Result(s)
22.1.2 – Auto-Negotiation Enable	**a**	**PASS**
	b	**PASS**
	c	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that bit 0.12 controls the enabling/disabling of the Auto-Negotiation process.

a. Bit 12 of the Control Register (MII Register 0) gives the management the ability to enable/disable Auto-Negotiation. A value of one is written to this bit. The DUT should transmit FLPs if this bit contains a value of one.
b. A value of zero is written to bit 0.12. The DUT should cease FLP transmission and proceed to transmit valid link signaling (based on the values of bits 0.6 and 0.13). The DUT may also wait approximately break_link_timer before sourcing valid link signaling.
c. A value of one is written to bit 0.12. The DUT should cease link signaling, wait approximately break_link_timer, and transmit FLPs.

Comments on Test Results

a. The DUT properly transmitted FLPs.
b. The DUT transmitted valid link signaling immediately after a value of zero was written to bit 0.12.
c. The DUT halted link signaling, waited approximately break_link_timer, and transmitted FLPs.

Sample Report

Test # and Label	Part(s)	Result(s)
22.1.3 – Auto-Negotiation Restart	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that bit 0.9 controls the restarting of Auto-Negotiation.

a. Bit 9 of the Control Register (MII Register 0) gives management the ability to restart Auto-Negotiation without resetting the PHY. Once the DUT is transmitting FLPs, bit 9 of the Control Register is set. The DUT should stop Auto-Negotiation, wait approximately break_link_timer, and then restart Auto-Negotiation by sending FLPs.

Comments on Test Results

a. The DUT properly halted FLP transmission for approximately break_link_timer and then restarted Auto-Negotiation by sending FLPs.

Test # and Label	Part(s)	Result(s)
22.1.4 – Auto-Negotiation Complete	**a**	**PASS**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that bit 1.5 is properly set upon completion of Auto-Negotiation and entrance into the FLP LINK GOOD state.

a. Auto-Negotiation is disabled by setting bit 0.12 to zero. The DUT is sent enough FLPs to put it through the COMPLETE ACKNOWLEDGE state followed by valid link signaling in order to establish a link. The status of bit 1.5 is observed.
b. The procedure for part a is repeated; however, Auto-Negotiation is enabled by setting bit 0.12 to one.

Comments on Test Results

a. The value of bit 1.5 was properly set to 0 indicating that the DUT did not enter the FLP LINK GOOD state.
b. The value of bit 1.5 was properly set to 1 indicating that the DUT was in the FLP LINK GOOD state.

Test # and Label	Part(s)	Result(s)
22.1.5 – Link Status	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that bit 1.2 of the Status Register is set when a valid link has been established and is not set if a valid link has not been established.

a. Bit 1.2 of the Status Register (MII Register 1) makes management aware that a valid link has been established. The DUT is sent a series of FLPs and link signaling to establish a link. The status of bit 1.2 is observed. Auto-Negotiation is disabled on the DUT and an Idle pattern is sent to manually force link. The status of bit 1.2 is observed.

Comments on Test Results

a. In both of the above scenarios the value of bit 1.2 was not set to a value of one until the FLP LINK GOOD state was entered.

Sample Report

Test # and Label	Part(s)	Result(s)
22.1.6 – Auto-Negotiation Ability	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT maintains the value of one in bit 1.3.

a. Bit 1.3 indicates whether a PHY supports Auto-Negotiation. Bit 0.12 is set to a value of zero in the DUT to disable Auto-Negotiation. Bit 0.12 is then set to a value of one in the DUT to enable Auto-Negotiation.

Comments on Test Results

a. The DUT maintained a value of one in bit 1.3 regardless as to whether Auto-Negotiation was enabled or disabled.

Test # and Label	Part(s)	Result(s)
22.1.7 – Report PHY Capabilities	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the PHY set bits 1.15:8 and 15.15:12 appropriately for the PHY's capabilities.

a. Bits 1.15:8 and 15.15:12 contain the PHY's signaling capabilities. These registers should be set appropriately on the DUT and bit 1.8 must contain a value of one if Register 15 is non-zero.

Comments on Test Results

a. The DUT contained valid values in bits 1.15:8. The bits advertised correspond to the following abilities:
   - 10BASE-T half duplex
   - 10BASE-T full duplex
   - 100BASE-X half duplex
   - 100BASE-X full duplex
   - Extended Status

   The DUT contained valid values in bits 15.15:12. The bits advertised correspond to the following abilities:
   - 1000BASE-T half duplex
   - 1000BASE-T full duplex

SampleReport

Test # and Label	Part(s)	Result(s)
22.1.8 – Duplex Mode	**a**	**Not Applicable**
	b	**Informative**
	c	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT will resolve a link to the highest common duplex mode according to bit 0.8.

a. The Control Register (MII Register 0) is accessed and the default value of bit 0.8 is read. If a PHY is able to operate in only one duplex mode, then the value of bit 0.8 should correspond to the mode in which the PHY can operate, and any attempt to change the setting of bit 0.8 should be ignored.
b. INFORMATIVE: Bit 12 of the Control Register gives the management the ability to enable/disable Auto-Negotiation. A value of one is written to this bit. A link is then established with the DUT by sending FLPs advertising full duplex only at one supported speed. When Auto-Negotiation has been enabled, bit 0.8 can be read or written, but its state has no effect on the link configuration.
c. When Auto-Negotiation is disabled, setting bit 0.8 configures the PHY for full duplex operation and clearing bit 0.8 configures the PHY for half duplex operation. A zero is written to bit 12 of the Control Register to disable Auto-Negotiation. Bit 0.8 is set to one and a full duplex link is established by sending the DUT appropriate link signaling at one supported speed. This procedure is then repeated when bit 0.8 is cleared and half duplex link is established.

Comments on Test Results

a. The PHY was observed to operate in both half duplex and full duplex modes of operation, therefore this test did not apply.
b. The DUT did not write bit 0.8 to reflect link configuration.
c. The DUT properly resolved a full duplex link when bit 0.8 was set and resolved a half duplex link when bit 0.8 was cleared.

SampleReport

Test # and Label	Part(s)	Result(s)
22.1.9 – Speed Selection	**a**	**PASS**
	b	**PASS**
	c	**PASS**
	d	**Informative**

Expected Results and Procedural Comments

Purpose: To verify that bits 0.6 and 0.13 of the Control Register are set appropriately once a valid link has been established manually.

a. Via management, the Control Register (MII Register 0) is accessed and bits 0.6 and 0.13 are read. The default values should reflect the highest speed capable of the PHY.
b. Auto-Negotiation is disabled by writing a value of zero to bit 0.12. A value of zero is written to bits 0.6 and 0.13. Observing transmissions from the DUT, this scenario is repeated writing a value of one to bit 0.13 and zero to 0.6, writing a value of zero to bit 0.13 and one to bit 0.6, and a value of one to bit 0.13 and one to bit 0.6. The DUT should transmit appropriate link signaling corresponding to bits 0.6 and 0.13.
c. Auto-Negotiation is enabled by writing a value of one to bit 0.12. A 100BASE-TX link is established with the DUT and Register 0 is accessed. A one is written to bit 0.6 and a zero is written to bit 0.13. This is then repeated writing a value of zero to bit 0.6 and a one to bit 0.13. Writing to these bits should have no effect on the configuration.
d. INFORMATIVE: Part c, is repeated and bits 0.6 and 0.13 are read. These bits may or may not reflect the operating speed of the link when read.

Comments on Test Results

a. The default value of bits 0.6 and 0.13 reflected the highest speed capable of the PHY.
b. The DUT properly transmitted appropriate link signaling corresponding to bits 0.6 and 0.13.
c. The writing of bits 0.6 and 0.13 did not have any effect on the link configuration.
d. When Auto-Negotiation was enabled, the DUT did not indicate the operating speed of the link through bits 0.6 and 0.13.

Sample Report

GROUP 2: CLAUSE 28 MANAGEMENT REGISTERS

Test # and Label	Part(s)	Result(s)
28.2.1 – Auto-Negotiation Advertisement Register	**a**	**PASS**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the Auto-Negotiation Advertisement Register (Register 4) is reflected in the Link Code Words transmitted by the DUT.

a. The Advertisement Register (MII Register 4) is accessed. 8001h is written to the Advertisement Register. The DUT should transmit FLPs containing the value of 8001h. This is then repeated with, but not limited to, the values E001h, 0000h, and FFFFh.
b. Register 4 and the Link Code Words transmitted by the DUT should contain the bit value of zero for 4.14.

Comments on Test Results

a. In all of the above cases, the DUT properly transmitted FLPs containing each of the bit values after they were written to MII Register 4, leaving the ACK bit (4.14) with a zero value.

   It was observed that the DUT properly transmitted the Next Page bit in its Link Code Word due to Annex 40C, in all cases:
   - When the DUT advertised 1000BASE-T speeds in Register 9, the Next Page bit in the DUT's Link Code Word was observed to be set to one regardless of the value contained in bit 4.15. When bit 4.15 was set to zero, the DUT supported a fully managed Next Page Exchange. When bit 4.15 was set to one, the DUT required Register 7 (AN Next Page Transmit Register) to be written in order to complete the Next Page Exchange. In this case however, the DUT's Next Pages did not correspond to Register 7, but contained valid 1000BASE-T Next Pages.
   - When the 1000BASE-T abilities were disabled in Register 9, the Next Page bit in the DUT's Link Code Word directly corresponded to bit 4.15. When bit 4.15 was set to one, the DUT supported a fully unmanaged Next Page Exchange.

b. The DUT properly did not allow bit 4.14 to be written.

Test # and Label	Part(s)	Result(s)
28.2.2 – Auto-Negotiation Link Partner Ability Register	**a**	**PASS**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the Auto-Negotiation Link Partner Ability Register is set according to Table 28-3 based upon the reception of Link Code Words by the DUT.

a. Enough Link Code Words are transmitted to the DUT in order to put the DUT into the COMPLETE ACKNOWLEDGE state. The AN Link Partner Ability Register (MII Register 5) is then accessed and read. This is then repeated with the values 0000h and FFFFh along with the same page with ACK. Each transmitted bit value should appear in Register 5 once it has been received.
b. FFFFh is written to Register 5. This should be rejected by the DUT.

Comments on Test Results

a. The DUT properly stored values of the received FLPs in Register 5.
b. The DUT properly rejected the write, preserving the values in Register 5.

Sample Report

Test # and Label	Part(s)	Result(s)
28.2.3 – Remote Fault	**a**	**PASS**
	b	**FAIL**
	c	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT sets bit 1.4 upon reception of a Link Code Word with the Remote Fault bit set.

a. A device that supports the Remote Fault function must indicate the reception of a Link Code Word with the Remote Fault bit set by setting bit 1.4 of the Status Register (MII Register 1). The Status Register is read twice.
b. The DUT is sent enough FLPs with the Remote Fault bit set to go through the COMPLETE ACKNOWLEDGE state. Once Auto-Negotiation has restarted, bit 1.4 is read. The DUT should set bit 1.4. The Status Register is read again. The DUT should clear bit 1.4.
c. A link is established with the DUT such that the Link Partner advertised Remote Fault. Bit 1.4 is read. The DUT should set bit 1.4. The Status Register is read again. The DUT should clear bit 1.4.

Comments on Test Results

a. Bit 1.4 was observed to properly contain a value of zero when no Remote Fault had been received.
b. Bit 1.4 was observed to improperly contain a value of zero when a Remote Fault had been received.
c. Bit 1.4 was properly observed to contain a value of one when a Remote Fault was received. It was verified that the DUT did not clear bit 1.4 until it was read. When read again, bit 1.4 properly contained a value of zero.

Test # and Label	Part(s)	Result(s)
28.2.4 – Parallel Detection Fault	**a**	**PASS**
	b	**Not Applicable**
	c	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT sets bit 6.4 upon reception of a parallel detection fault.

a. Bit 6.4 makes management aware of a parallel detection fault. The DUT is sent valid 100BASE-TX Idle signal for less than 500 ms such that FLP transmission ceases. The value of the Auto-Negotiation Expansion Register (MII Register 6) is then read twice.
b. The DUT is sent valid 100BASE-T4 Idle signal for less than 500 ms such that FLP transmission ceases. The value of the Auto-Negotiation Expansion Register is then read twice.
c. The DUT is sent valid 10BASE-T signal for less than 500 ms such that FLP transmission ceases. This may be lc_max NLPs. The value of the Auto-Negotiation Expansion Register is then read twice.

Comments on Test Results

a. Upon the first read, bit 6.4 contained a value of one. Upon the second read, bit 6.4 contained a value of zero.
b. The DUT did not support a 100BASE-T4 PMA, therefore this test could not be performed.
c. Upon the first read, bit 6.4 contained a value of one. Upon the second read, bit 6.4 contained a value of zero.

Sample Report

Test # and Label	Part(s)	Result(s)
28.2.5 – Page Received Setting/Resetting	**a**	**PASS**
	b	**PASS**
	c	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that mr_page_rx is set when a new page is received and cleared when the Auto-Negotiation Expansion Register is read.

a. Bit 6.1 indicates to the management that a page has been received. The DUT is sent a series of valid FLPs without the ACK bit set so that it would enter the ACKNOWLEDGE DETECT state. The value of the Auto-Negotiation Expansion Register (MII Register 6) should remain zero.
b. The DUT is sent a series of valid FLPs to put it through the COMPLETE ACKNOWLEDGE state. The value of the Auto-Negotiation Expansion Register (MII Register 6) should contain a one value upon the first read and a zero value upon the second read.
c. Auto-Negotiation is then restarted and the DUT is sent enough FLPs with the value of C1E1h to enter the COMPLETE ACKNOWLEDGE state. This stream of FLPs is immediately followed by FLPs encoded with E808h. The value of the Auto-Negotiation Expansion Register (MII Register 6) should contain a one value upon the first read. A desired Next Page value may be written to Register 7 and bit 6.1 should contain a one value upon the read and a zero value upon the next read.

Comments on Test Results

a. Upon entering the ACKNOWLEDGE DETECT state, bit 6.1 was observed to properly contain a value of zero.
b. Upon entering the COMPLETE ACKNOWLEDGE state, bit 6.1 was observed to properly contain a value of one for the first read followed by a value of zero for the second read.
c. Each time the DUT enters the COMPLETE ACKNOWLEDGE state, bit 6.1 was observed to contain a value of one. Bit 6.1 properly contained a value of zero for the third read.

Test # and Label	Part(s)	Result(s)
28.2.6 – Link Partner Auto-Negotiation Able	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT sets bit 6.0 upon detection of link partner which is capable of Auto-Negotiation.

a. Bit 6.0 indicates to management that the link partner is Auto-Negotiation able. The DUT is reset and bit 6.0 is read. The DUT is sent a constant stream of identical FLPs to set ability_match=true and bit 6.0 is read. Nothing is sent to the DUT and bit 6.0 is read. The DUT is sent a constant stream of FLPs alternating in content to keep it in the ABILITY DETECT state and bit 6.0 is read.

Comments on Test Results

a. When the DUT was sent a constant stream of identical FLPs, bit 6.0 properly contained a value of one. Upon all other reads, bit 6.0 contained a value of zero.

Test # and Label	Part(s)	Result(s)
28.2.7 – Auto-Negotiation Next Page Transmit Register	**a**	**PASS**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the Auto-Negotiation Next Page Transmit Register, set according to Table 28-6, is properly reflected in the Next Pages transmitted by the DUT.

a. The management uses the Auto-Negotiation Next Page Transmit Register (MII Register 7) to control the content of transmitted Next Pages. The Next Page bit (4.15) is set in the DUT. A constant stream of FLPs containing a value of C1E0h is sent to the DUT. A value of 2008h is written to Register 7 of the DUT. This scenario is repeated using the values of, but not limited to, 2808h and FFFFh. The Next Pages transmitted by the DUT should have bits 7.15, 7.13, 7.12, and 7.10:0 set to what is written in Register 7.
b. Throughout Part a, the Next Pages transmitted by the DUT should have bit 7.14 set to zero and bit 7.11 set to the opposite of the value of bit 4.11 in the initial Link Code Word sent by the DUT.

Comments on Test Results

a. The DUT properly transmitted the Next Pages containing the bit values of bits 7.15, 7.13, 7.12, and 7.10:0 after they were written to MII Register 7.
b. The DUT properly transmitted the Next Pages with bit 7.14 containing a zero value and bit 7.11 containing the opposite of the value of bit 4.11 in the initial Link Code Word sent by the DUT.

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Test # and Label	Part(s)	Result(s)
28.2.8 – Auto-Negotiation Link Partner Ability Next Page Register and Next Page Location Bits	**a**	**PASS**
	b	**Not Applicable**
	c	**PASS**
	d	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the Auto-Negotiation Link Partner Received Next Page Register is set according to Table 28-7 based upon the reception of Next Pages by the DUT and to verify that the DUT properly stores received Next Pages in the correct register based on bits 6.6:5.

a. Register 6 bits 5 and 6 are read from management. A value is then written to these bits, which differ from that previously read. The bits should reject the write, preserving the values in bits 6.6:5.
b. The management uses the Auto-Negotiation Link Partner Ability Next Page Register to control the content of received Next Pages. The Next Page bit (4.15) is set in the DUT. A constant stream of FLPs with the Next Page bit set is sent to the DUT to force it to enter the COMPLETE ACKNOWLEDGE state. This transmission is followed by FLPs containing the value 2008h. A value of 2001h is written to Register 7. The DUT should store the Auto-Negotiation Link Partner Ability Next Page Register in Register 8 if bit 6.6 is one and bit 6.5 is one, or in Register 5 if bit 6.6 is one and bit 6.5 is zero. If bit 6.6 is set to zero, the DUT is allowed to store the received Next Pages in either Register 5 or Register 8 and this test is “Informative”.
c. The value read from the Auto-Negotiation Link Partner Ability Next Page Register in part b should identically match the received Next Page from the Link Partner. This scenario is repeated transmitting the DUT Next Pages with values of and not limited to 2808h, FFFFh and 0000h.
d. Write values of FFFFh and 0000h to the Auto-Negotiation Link Partner Received Next Page Register.

Comments on Test Results

a. The DUT properly rejected the write, preserving the value in bits 6.6:5.
b. The DUT was observed to not implement bits 6.6:5. It was observed that the DUT stored the values of received Next Pages within Register 8.
c. The DUT properly stored the correct value of the received Next Pages in the Auto-Negotiation Link Partner Ability Next Page Register.
d. The DUT properly rejected the write, preserving the values in the Auto-Negotiation Link Partner Received Next Page Register.

Sample Report

Test # and Label	Part(s)	Result(s)
28.2.9 – mr_next_page_loaded	**a**	**PASS**
	b	**PASS**
	c	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that mr_next_page_loaded is set upon write to the Auto-Negotiation Next Page Transmit register and cleared in the states NEXT PAGE WAIT and TRANSMIT DISABLE.

a. A value of one is written to bit 4.15. A value of '2201h' is written to Register 7. Auto-Negotiation is restarted (a value of 1 was written to bit 0.12). A constant stream of FLPs with the Next Page bit set is sent to cause the DUT to enter the COMPLETE ACKNOWLEDGE state. The DUT should remain in the COMPLETE ACKNOWLEDGE state and continue to send its Base Page with ACK.
b. If the DUT remained in the ACKNOWLEDGE DETECT state a value of '2301h' is written to Register 7, then a value of '2401h' is written to Register 7. If the DUT remained in the COMPLETE ACKNOWLEDGE state while sending its first Next Page (2201h), a value of 2301h is written to Register 7 to trigger the 2nd Next Page transmission. After mr_next_page_loaded=true, the DUT should commence transmitting its Next Page, with the proper Toggle and ACK bit values.
c. Once rx_link_code_word[12]=1 and toggle_rx ^ the DUT should remain in COMPLETE ACKNOWLEDGE state and continue to send its first Next Page (2301h).

Comments on Test Results

a. The DUT was observed to properly remain in the COMPLETE ACKNOWLEDGE state and continue to send its Base Page with ACK.
b. The DUT properly continued the Next Page exchange, transmitting its Next Page with the proper Toggle and ACK bit values.
c. The DUT remained in the COMPLETE ACKNOWLEDGE state and continued to send its first Next Page.

Test # and Label	Part(s)	Result(s)
28.2.10 – Next Page Able	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT sets bit 6.2 if it is capable of a Next Page exchange.

a. A PHY which supports Next Page exchange must indicate this capability to management by setting bit 6.2 in the Expansion Register (MII Register 6), regardless of whether a Next Page exchange is desired. Bit 4.15 the Next Page Advertisement Register is set to zero. After bit 6.2 of the MII Expansion Register (Register 6) is read, Next Page advertised is set to one. The MII Expansion Register (Register 6) should reflect the advertised capability for a Next Page exchange.

Comments on Test Results

a. Upon the first read, bit 6.2 contained a value of one. After enabling Next Page advertisement, bit 6.2 contained a proper value of one.

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Test # and Label	Part(s)	Result(s)
28.2.11 – Link Partner Next Page Able	**a**	**PASS**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify that the DUT sets bit 6.3 upon reception of a Base Page which has bit 15 set.

a. Bit 6.3 allows the management to become aware that the Link Partner supports Next Page. A value of zero is written to bit 4.15 of the DUT. Bit 6.3 is read. A stream of identical FLPs with the ACK bit set and the NP bit not set is sent to put the DUT into the COMPLETE ACKNOWLEDGE state. Bit 6.3 is read. On both reads the DUT should have a value of zero in bit 6.3.
b. A value of zero is written to bit 4.15 of the DUT. The DUT is sent a constant stream of FLPs with the ACK bit set and the NP bit set. Once the DUT enters the COMPLETE ACKNOWLEDGE state, bit 6.3 is read. This scenario is repeated after the DUT is reset and the Next Page Advertisement is written (bit 4.15). Once the DUT enters the COMPLETE ACKONWLEDGE, a value of zero is written to bit 0.15 to reset the PHY. Bit 6.3 is read. On the first two reads, bit 6.3 should have a value of one. In the last read, bit 6.3 should contain a value of zero.

Comments on Test Results

a. In both scenarios bit 6.3 properly contained a value of zero.
b. On the first two reads, bit 6.3 properly contained a value of one. On the last read, bit 6.3 properly contained a value of zero.

Sample Report

GROUP 3: CLAUSE 40 MANAGEMENT REGISTERS

Test # and Label	Part(s)	Result(s)
40.3.1 – 1000BASE-T MASTER/SLAVE Control Register Bits 9.10:8	**a**	**PASS**

Expected Results and Procedural Comments

Purpose: To verify for 1000Base-T devices that the MASTER/SLAVE Control Register bits 9.10:8 properly control the advertised Port type and duplex.

a. Bits 9.10:8 control the 1000BASE-T advertisement of full duplex, half duplex, and single port or multiport device. Values of 010b through 111b are written to these bits. The DUT is then sent enough Base Pages and Next Pages such that it will transmit its first Unformatted Message Page. The values of bits U2, U3, and U4 should correspond to the values of bits 9.10:8.

Comments on Test Results

a. The DUT was observed to properly set bits 9.10:8 in its first Unformatted Message Page.

Test # and Label	Part(s)	Result(s)
40.3.2 – 1000BASE-T MASTER/SLAVE Control Register Bits 9.12:11	**a**	**PASS**
	b	**PASS**

Expected Results and Procedural Comments

Purpose: To verify for 1000Base-T devices that the MASTER/SLAVE Control Register bits 9.12:11 properly control MASTER/SLAVE Manual Configuration.

a. Bits 9.12:11 control the MASTER/SLAVE configuration enable, and MASTER/SLAVE configuration value abilities. Values of 11b, 10b, and 00b are written to these bits. The DUT is then sent enough Base Pages and Next Pages such that it will transmit its first Unformatted Page. The values of bits U0 and U1 should correspond to the values of bits 9.12 and 9.11.
b. Bits 9.12:11 are given a value of 01b, and the DUT is again sent enough pages such that it transmits its first Unformatted Page. The DUT may or may not set bits U0 and U1 to bits 9.12 and 9.11.

Comments on Test Results

a. The DUT was observed to properly set bits U0 and U1 to the values contained in bits 9.12:9.11.
b. The DUT was observed to properly set bits U0 and U1 to the values contained in bits 9.12:9.11.

Sample Report

Test # and Label	Part(s)	Result(s)
40.3.3 – 1000BASE-T MASTER/SLAVE Status Register	**a**	**PASS**
	b	**PASS**
	c	**PASS**
	d	**PASS**
	e	**PASS**
	f	**PASS**

Expected Results and Procedural Comments

Purpose: To verify for 1000Base-T devices that the MASTER/SLAVE Status Register conforms to the definition in Table 40-3.

a. Register 10 should be read only, and should ignore any writes to this register.
b. Bits 10.11 and 10.10 should represent the 1000Base-T duplex capability of the link partner. A valid link is established with the DUT such that all four combinations of duplex are tested (full only, half only, full/half, no duplex).
c. Bit 10.14 indicates whether the DUT has resolved to MASTER or SLAVE. A valid link is established with the DUT such that the DUT should resolve to MASTER. Then, a valid link is established with the DUT such that the DUT should resolve to SLAVE.
d. Bit 10.15 indicates whether or not a MASTER/SLAVE configuration fault has been detected by the DUT. Both the DUT and the link partner are set to advertise manual_MASTER. The two devices then attempt to establish a link. The DUT should set bit 10.15.
e. Bits 10.13 and 10.12 indicate the status of the local receiver and transmitter. The DUT is connected to a link partner, and a link is established. Once the link is established, the DUT should set bits 10.13 and 10.12.
f. Bits 10.7:0 indicate an Idle Error Count. When the quality of the link is degraded, the DUT should update these bits.

Comments on Test Results

a. The DUT was observed to ignore all attempts to write to register 10.
b. The DUT was observed to properly indicate the advertised duplex capability of its link partner.
c. The DUT was observed to properly indicate whether it had resolved to MASTER or SLAVE.
d. The DUT was observed to properly indicate that a MASTER-SLAVE configuration fault was detected.
e. The DUT was observed to properly indicate that local receiver and transmitter status was OK.
f. The DUT was observed to properly increment these bits when the quality of the link was degraded.